A $\Sigma\Delta$ CMOS ADC with 80-dB Dynamic Range and 31-MHz Signal Bandwidth

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***Abstract*—A new $\Sigma\Delta$ modulator architecture is proposed that shapes DAC mismatches in a manner similar to quantization noise shaping, allowing operation with low oversampling ratios and compact logic. The concept is demonstrated in a fourth-order cascaded system running at a clock frequency of 500 MHz and digitizing input frequencies as high as 31 MHz with 80-dB dynamic range. Fabricated in 90-nm CMOS technology, the prototype provides a peak signal-to-(noise+distortion) ratio of 70 dB at 31 MHz while consuming 140 mW from a 1.2-V supply.**

I. Introduction

The choice between Nyquist-rate and oversampling analog-to-digital converters (ADCs) for high-speed applications has been primarily based on the resolution, with the dividing line lying around 14 bits. At the 14-bit level, therefore, the two classes exhibit competitive attributes—but different trade-offs as the device dimensions and supply voltages scale. This paper demonstrates that oversampling ADCs can indeed compete with and even supersede their pipelined counterparts at the 14-bit level.

This paper proposes a low-complexity digital-to-analog (DAC) mismatch shaping technique that lends itself to low oversampling ratios (OSRs), leading to an ADC having a measured signal-to-(noise+distortion) ratio (SNDR) of 70 dB at an analog input frequency of 31 MHz, the highest combination reported in the literature in CMOS technology for a power dissipation of 140 mW. The design also achieves a dynamic range (DR) of 80 dB at 31 MHz, the highest combination reported for $\Sigma\Delta$ modulators. While applied to a discrete-time modulator here, the mismatch shaping technique can be utilized in continuous-time implementations as well.

The paper is organized as follows. Section II introduces the converter architecture, and Section III the mismatch shaping technique. Section IV describes the implementation of the building blocks, and Section V presents the experimental results.

II. System Architecture

In order to digitize signal frequencies of 30 MHz and above, the oversampling ratio is constrained to about 8. The order of the modulator and the resolution of the quantizers must therefore be sufficiently high to achieve a dynamic range of 80 dB. Figure 1 shows the high-level ADC architecture. Operating

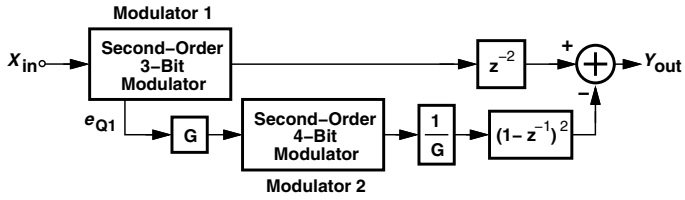

Fig. 1. High-level ADC architecture.

with an OSR of 8, the converter consists of two second-order modulators with 3-bit and 4-bit quantizers. An interstage gain of $G = 4$ increases the ADC's dynamic range proportionally [1]. It can be shown that, if $G = 2^{N_1-1}$, the dynamic range of the overall cascade is

$$DR \simeq \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot OSR^{2L+1} \cdot 2^{2(N_1+N_2-1)}, \quad (1)$$

where L_j and N_j denote, respectively, the order and quantizer resolution of modulator j and $L = L_1+L_2$. Equation (1) reveals that the cascade behaves as an L-th order modulator having an $(N_1 + N_2 - 1)$-bit quantizer.

In order to ensure small quantization noise leakage and moderate integrator swings without increasing the capacitive load of the second integrator in the first modulator, $N_1 = 3$ is chosen. N_2 can be obtained from (1) so as to achieve the required dynamic range. For $N_2 = 4$, the theoretical DR reaches 91 dB, leaving adequate margin for electronic noise, leakage, DAC mismatch noise, and other imperfections.

III. DAC Mismatch Shaping

A multitude of techniques have been reported that shape the DAC mismatches and push the energy to high frequencies [1]- [4]. Among these, the tree structure scheme described in [2] provides second-order shaping of the mismatches, but it is suited to high-OSR modulators. At $OSR = 8$, the approach suffers from low averaging of the mismatches because the oversampling is not fast enough to cycle through all possible combinations of the DAC elements over a sufficiently short time. For example, according to simulations, this technique yields a dynamic range of only 73 dB (in the absence of device noise) with $OSR = 8$ in a fourth-order modulator employing a 4-bit DAC whose capacitors have a mismatch of 0.2%.

Data-weighted averaging (DWA) [3], on the other hand, lends itself better to low-OSR systems. It must, however, deal with

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two issues. First, in-band tones arising from DAC mismatch patterns degrade the overall SNDR, and tone reduction techniques such as those in [1] and [4] and inevitably raise the noise floor. Second, more importantly, the complexity of DWA logic grows exponentially with the number of bits, thereby introducing a significant delay [5] and limiting the settling time allowed for the second integrator and the conversion time allowed for the quantizer.

Consider the modulator shown in Fig. 2(a), which is derived from the standard second-order loop by factoring out the first integration and inserting it in series with the input and with the DAC. It can be shown that the first DAC mismatch, X_{mis}, experiences first-order shaping as it appears at the output:

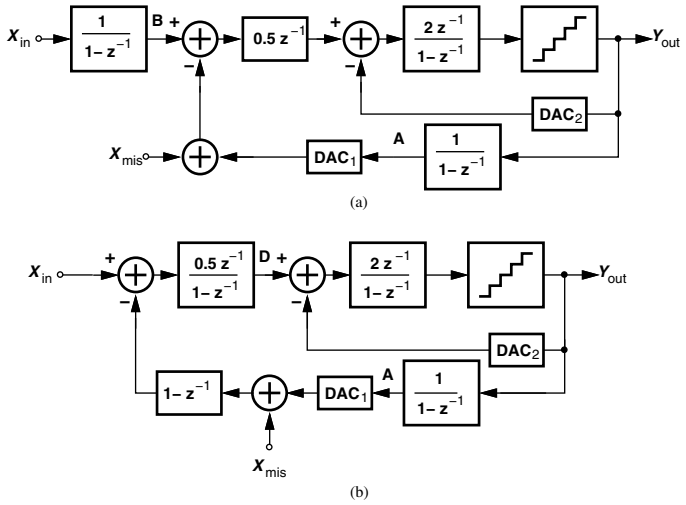

Fig. 2. (a) Factorization of $(1-z^{-1})^{-1}$ to shape X_{mis}, (b) modified structure to avoid overflow at input.

$$Y_{out} = z^{-2}X_{in} + (1 - z^{-1})X_{mis}. \tag{2}$$

Thus, the DAC mismatch is suppressed in a manner similar to the quantization noise, obviating the need for explicit randomization and shaping of the mismatches. However, due to "open-loop" integration, the signals at nodes A and B are unbounded.

In order to avoid an unbounded signal at node B, we return the input integrator to its original position while maintaining the one before DAC_1 and inserting a differentiator after DAC_1 [Fig. 2(b)]. The transfer function in (2) still applies, but the output of the digital integrator (accumulator), A, remains unbounded. That is, each time the accumulator reaches its maximum, which results in an overflow signal, DAC_1 produces a large step, which after differentiation and integration, also appears at node D and in Y_{out}.

If the carry output of the accumulator is converted to analog form through a single-bit DAC (which we call DAC_3) and summed with the differentiator output, then no overflow error occurs. In other words, the system from the output of the quantizer to the output of the summing node has a unity transfer function in the absence of DAC mismatches.

Note that DAC_1 mismatches are still shaped by $1 - z^{-1}$ even though DAC_3 is added. Owing to this factor, the DAC mismatch shaping can scale with OSR in a manner similar to quantization noise shaping. Moreover, the technique lends itself to high-speed logic because it requires no randomization.

The resulting modified architecture entails a number of issues. First, the differentiator following DAC_1 appears to amplify high-frequency noise. This issue is resolved by merging the differentiator with the front-end integrator, thus arriving at a simple amplification function. The second issue relates to mismatches between DAC_1 and DAC_3. Since the carry output occurs only occasionally, such mismatches are weighted by a small factor. It can be shown that this weighting factor is proportional to the rate of occurrence of the carry signal. Furthermore, the design is modified to obtain a signed carry, thereby reducing its rate of occurrence as well as forcing its average to zero. Since the modified carry signal can be either positive, negative or zero, a 3-level DAC must be used. DAC_3 is then a 1.5-bit DAC that is constructed using only one capacitor, hence unconditionally linear.

In Fig. 3 the DAC_1 mismatches are shaped by $1 - z^{-1}$. The mismatches between DAC_1 and DAC_3 are weighted by the rate of occurrence of the carry signal, which in turn depends on the input level, but also scaled down by the oversampling ratio in a manner similar to kT/C and op amp noise. In Fig. 3 the overall DAC of the first modulator feeding the first integrator consists of the adder/subtractor, DAC_1, the differentiator and DAC_3. The worst case linearity of this DAC happens at the maximum input level. From system level simulations, a 9-bit matching between DAC_1 and DAC_3 leads to a worst case linearity of the overall DAC of more than 80 dB.

It is worth noting that the total capacitance in the front-end integrator in the modified architecture equals that in the front-end integrator in the standard architecture. The total input-referred kT/C noise in the modified architecture is smaller than that of the standard architecture because the kT/C noise associated with the DAC_1 capacitance is first-order shaped when referred to the input. We therefore conclude that all of the capacitors in the modified architecture can be smaller than those in the standard one, saving a proportional power in the integrator. It can be shown that the power saving in the front-end integrator is 25% of its original value.

IV. Prototype ADC

The cascade ADC system of Fig. 1 has been realized as shown in Fig. 3, incorporating the proposed DAC mismatch shaping technique in the first modulator. The thermometer output is converted into binary using the thermometer to binary converter (TBC). An issue here is that bubbles in the thermometer code generated by the quantizer can create inconsistencies among four paths: the feedback path through the accumulator, the feedback path through DAC_2, the forward path through DAC_4 and the path to the output Y_{out1}. If employing different types of codes, these paths may potentially interpret bubbles differently, with the resulting (unshaped) inconsistency drastically reducing the dynamic range. To avoid this effect, the logic immediately following the quantizer simply calculates the

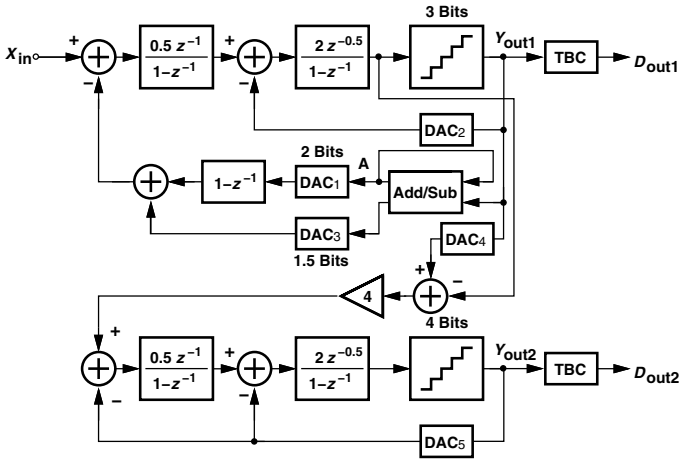

Fig. 3. Final modulator architecture.

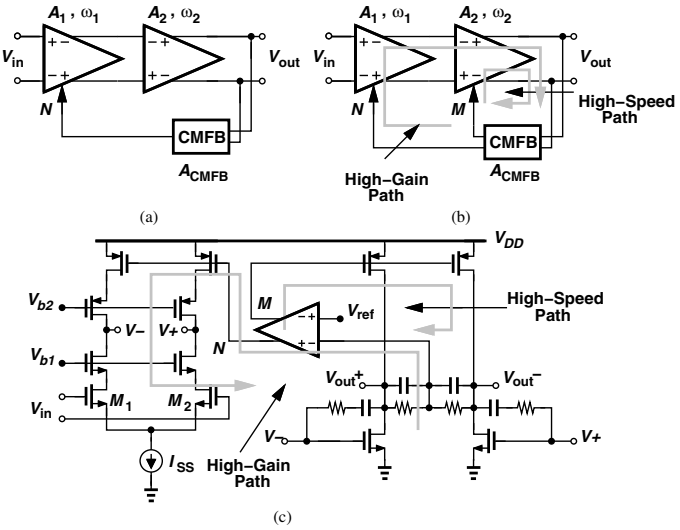

Fig. 4. Two-stage op amp with (a) single CMFB path, (b) high-gain and high-speed CMFB paths, and (c) new CMFB circuit.

number of ONEs in the thermometer code. Merging this thermometer/binary implementation with the accumulator results in a total delay that is linearly proportional to the number of bits in the quantizer rather than growing exponentially in most known DEM techniques. Using system level simulations, it can be shown that the DR is greater than 80 dB for 9-bit matching.

The ADC is implemented in 90-nm digital CMOS technology. In order to minimize quantization leakage, all of the DAC and integrator capacitors are formed as integer multiples of a unit. The unit itself is configured as a multi-finger structure. The circuit details of some building blocks are now described.

a) Op Amp: The large integrator output swings call for a two-stage op amp topology, and small leakage demands an open-loop gain of higher than 500. In addition to the need for frequency compensation for differential signals, two-stage op amps face stability issues with respect to their common-mode feedback (CMFB) loop. The poles in the differential signal path manifest themselves in the CMFB loop as well, but differential compensation may not stabilize the CMFB loop because of its additional poles or a different feedback factor.

In order to stabilize the CMFB loop, one of two measures can be taken: (1) reduce the loop gain, e.g., by reducing A_{CMFB} in Fig. 4(a), but at the cost of slower CM settling, which may also contain differential settling tails; (2) apply "feedforward" to the CMFB path. Illustrated in Fig. 4(b), the latter technique adds a high-speed, low-gain path, thereby creating a zero in the equivalent loop transmission and improving the stability.

Figure 4(c) depicts the op amp implementation with dual-loop CM feedback. The high-gain path contains the dominant pole (at the output of the first stage), the second pole (at the main output), and the pole at node N. The high-speed path bypasses the dominant pole. Figure 5 shows the CMFB loop response with and without the high-speed path. The unity-gain bandwidth is almost unchanged while the phase margin improves from 25° to 58° in the presence of the high-speed path. Designed for a large-signal settling of 700 ps to 14-bit linearity level, the op amp draws a supply current of 33 mA and contributes a total input-referred noise of 58 μV_{rms} (before reduction by a factor of OSR).

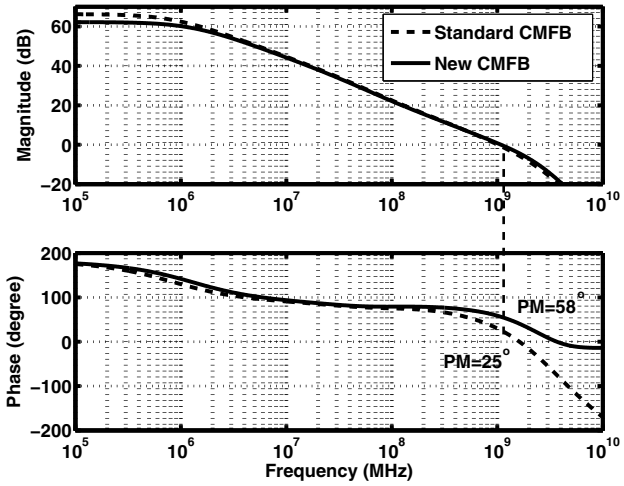

Fig. 5. CMFB loop response with high-speed path disabled and enabled.

b) Quantizer: The 3-bit quantizer in the first modulator employs seven comparators. The circuit consists of a differential difference amplifier and a low-power latch. The 4-bit quantizer in the second modulator incorporates a similar comparator but with 2x interpolation to reduce the capacitive loading seen by the second integrator. The first and second quantizers consume 3.5 mW and 4 mW, respectively.

V. Experimental Results

The ADC prototype has been fabricated in 90-nm CMOS technology and tested while operating from a 1.2-V supply. Figure 6 shows a photograph of the die, whose active area is 850 $\mu m \times$ 1350 μm. Running with a clock frequency of 500 MHz, the circuit has been tested in a chip-on-board

assembly, and the digital outputs (D_{out1} and D_{out2} in Fig. 3) are combined off-chip. The total power consumption (excluding that of the output buffers) is 140 mW.

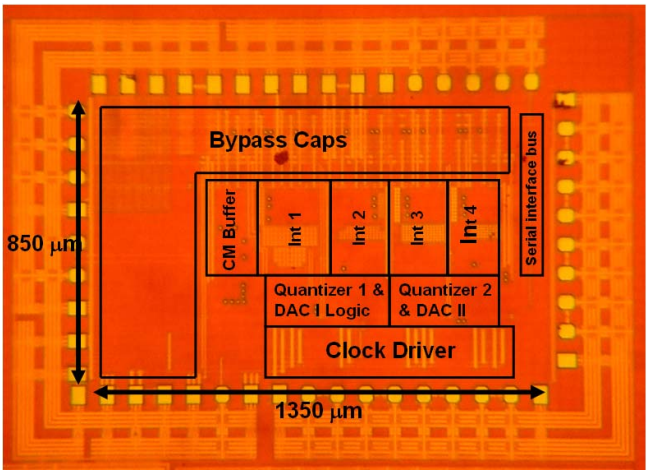

Fig. 6. Chip photograph.

Figure 7 plots the measured output spectrum for a 2.65-MHz full-scale input. The peak SNDR and SNR are 70 dB and 72 dB, respectively. Superimposed on this plot is the measured spectrum for a full-scale 31-MHz input, which still yields an SNDR of 70 dB.

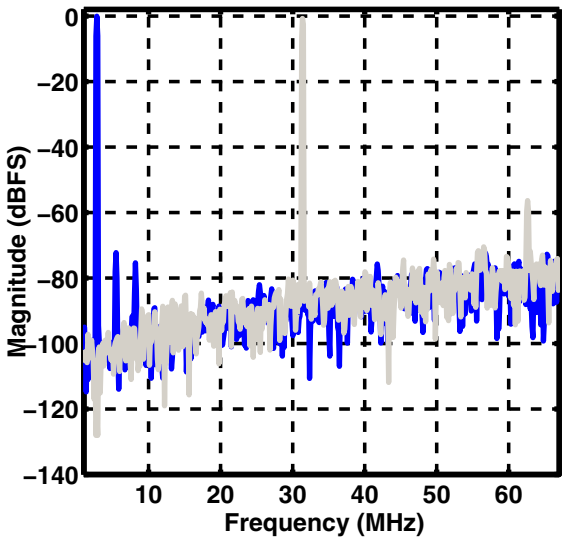

Fig. 7. Output spectra for $f_{CK} = 500$ MHz and $f_{in} = 2.65$ and 31 MHz.

Running the test at a sampling frequency of 200 MHz, Fig. 8 plots the measured output spectrum for a 1.06-MHz full-scale input. The peak SNDR and SNR are 73 dB and 74 dB, respectively. Superimposed on this plot is the measured spectrum for a full-scale 12.8-MHz input, which yields an SNDR of 74 dB. The second and third order harmonics are significantly lower than in the 500-MHz test.

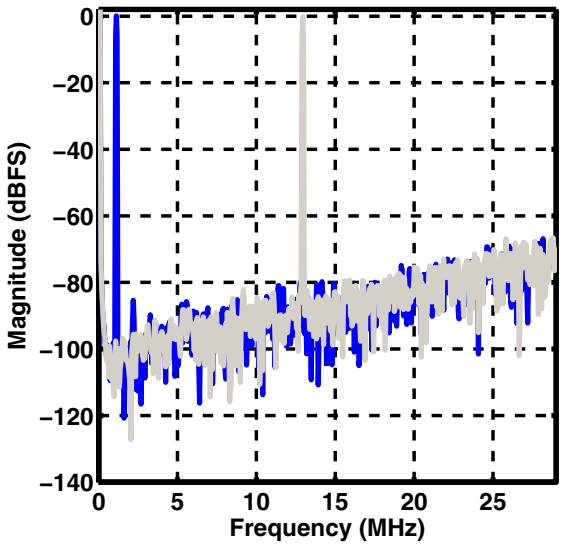

Fig. 8. Output spectra for $f_{CK} = 200$ MHz and $f_{in} = 1.06$ and 12.8 MHz.

Figure 9 plots the measured SNR and SNDR as a function of the input level, displaying a dynamic range of 80 dB for a clock frequency of 500 MHz and an input bandwidth of 31 MHz.

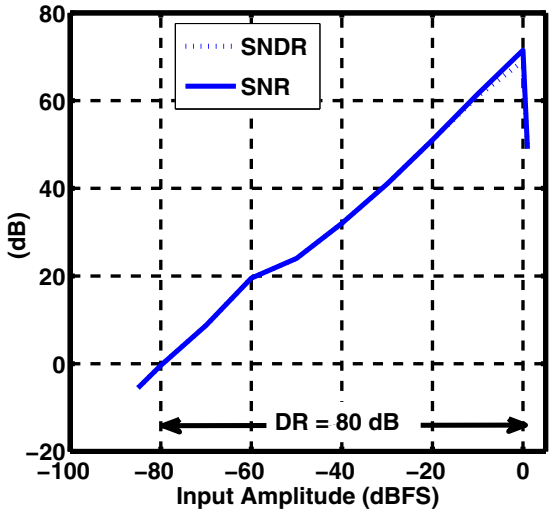

Fig. 9. SNR and SNDR vs. input level.

A slight adjustment of biases allows the prototype to operate at a clock frequency of 630 MHz while digitizing input frequencies as high as 35 MHz and consuming 160 mW. The peak SNDR and SNR are 65 dB and 69 dB, respectively, and the DR is 79 dB. Figure 10 plots the measured SNDR and DR as a function of the input frequency for a constant OSR of 8 (OSR=9 at the 35-MHz data point). Table I summarizes the measured performance of the prototype and Table II compares this performance with that of pipelined and oversampling converters in the same resolution range.

TABLE II
COMPARISON WITH PREVIOUS WORK

	f_s	f_M	DR	SNDR	Power	Technology	Comments
[6]	200M	11M	84 dB	72 dB	200 mW	0.18 μm	Discrete-time $\Sigma\Delta$
[7]	640M	20M	80 dB	76 dB	20 mW	0.13 μm	Continuous-time $\Sigma\Delta$
[8]	100M	39M	N/A	66 dB	300 mW	0.13 μm	Pipelined ADC
[9]	100M	50M	N/A	72 dB *	250 mW	0.13 μm	Pipelined ADC
This work	500M	31M	80 dB	70 dB	140 mW	90 nm	Discrete-time $\Sigma\Delta$
This work	630M	35M	79 dB	70 dB	160 mW	90 nm	Discrete-time $\Sigma\Delta$

* This work relies on uncalibrated matching for 14-bit resolution [10].

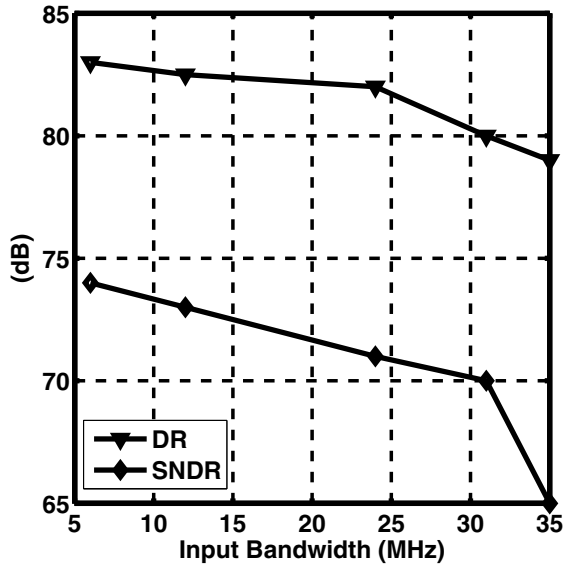

Fig. 10. SNDR and DR versus the input bandwidth.

TABLE I
PERFORMANCE SUMMARY

Max. Sampling Frequency		500 MHz
Max. Input Frequency		31 MHz
Max. Input Voltage Range		1.8 V_{pp}
Clock Freq. 500 MHz	DR	80 dB
	peak SNDR (@ 31 MHz)	70 dB
	peak SNR	72 dB
Clock Freq. 630 MHz	DR	79 dB
	peak SNDR (@ 35 MHz)	65 dB
	peak SNR	69 dB
Technology		90-nm 1P8M CMOS
Chip Area		850 $\mu m\times$ 1350 μm
Power Consumption		140 mW @ 500 MHz 160 mW @ 630 MHz

VI. CONCLUSION

This paper has introduced a DAC mismatch shaping technique that lends itself to both low oversampling ratios and compact, high-speed logic. Unlike prior approaches, the proposed method simply shapes the mismatches by the $\Sigma\Delta$ modulator loop—in a manner similar to the shaping of the quantization noise. The efficacy of the technique is demonstrated in a fourth-order cascaded system operating with an OSR of 8 and a clock frequency of 500 MHz. Designed in 90-nm CMOS technology, the prototype yields an SNDR of 70 dB with an analog input frequency of 31 MHz—the highest combination reported in the literature with a power consumption of 140 mW. The proposed mismatch shaping technique can also be combined with other schemes to create higher-order shaping and achieve greater accuracies.

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