14.2 A 2.75Gb/s CMOS Clock Recovery Circuit with Broad Capture Range

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Use of CMOS technology for optical fiber communications creates challenges in circuit design. In particular, multi-gigahertz clock recovery circuits require techniques coping with speed, power, and noise trade-offs. A critical issue in these circuits is the conflict between a narrow loop bandwidth imposed by optical standard jitter specifications and a broad capture range required by CMOS technology to encompass oscillator frequency variations with process and temperature. This dual-loop phase-locked architecture incorporates a digital frequency search algorithm, thereby extending the capture range by more than one order of magnitude without external references.

Figure 14.2.1 shows the architecture of the clock recovery circuit. In addition to the phase-locked loop (PLL), a frequency-locked loop (FLL) consisting of a quadrature frequency detector, a digital search algorithm, a counter, and a capacitor array controls the frequency of the voltage-controlled oscillator (VCO). The circuit begins by disabling the PLL and allowing the FLL to drive the VCO frequency within about 1.4MHz of the input data rate. The results are stored digitally and the PLL is subsequently enabled to perform phase locking. All building blocks are fully differential.

An important drawback of typical PLLs is their limited capture range. Behavioral simulations of PLLs reported in References 1 and 2 indicate a capture range of 10%-15%, a value perhaps adequate for bipolar technology but insufficient to accommodate VCO frequency variations in CMOS implementations. The PLL presented in this work overcomes this drawback. To arrive at the PLL design, first consider the average output voltage of a binary quadrature frequency detector [2] as a function of the difference between the data and clock rates, depicted in Figure 14.2.2a. In the near-lock region, where the clock frequency is within the capture range of the FD, the dc content is large enough to reliably signal the polarity of the frequency difference. However, in the far-from-lock region, the output carries little information. In this work, the VCO frequency is set to its minimum value and stepped up with adequate resolution until Δf enters the near-lock region and subsequently changes polarity.

The PLL operation is illustrated conceptually in Figure 14.2.2. A counter controlling the capacitor array sets the VCO frequency to the lowest value. Under this condition, Δf is negative and VCP is close to zero. Thus the two comparators generate logical zeros, the signal Δf_top remains low, and the counter continues to count up (with the aid of a slow external clock) until VCP drops below VLO. This is an indication that VCP has reached a reliable level. Now the two flipflops begin to save state before the next state is carried out. The counter continues to count until Δf crosses zero and VCP jumps from negative to positive. The two flipflops then record this change, disabling the counter and enabling the PLL.

The frequency resolution provided by the FLL is primarily determined by the capacitor array. With a tuning range of 350MHz and 45b resolution, the minimum frequency step is about 1.37MHz, accommodating a PLL capture range of a few megahertz. The PLL also allows a small VCO gain, K_vco, thus minimizing the jitter resulting from ripple on the control voltage.

This is particularly important at low supply voltages because, to obtain a given relative tuning range, K_vco must increase as the supply decreases. In this design, K_vco is 50MHz/V.

The VCO core consists of two LC oscillators coupled to operate in quadrature [Figure 14.2.3a]. The continuous frequency tuning is by varying the tail current in the coupling differential pairs [3]. To maintain relatively constant VCO gain across the tuning range, input voltage-to-current converter, M1-M2, incorporates linearization devices M3 and M4 [4]. An important advantage of this tuning technique over a varactor-based method is that the control voltage is fully differential.

The capacitor arrays added to the tanks in each VCO [Figure 14.2.3b] entail several design issues. First, the resolution of the array determines how close the frequency can come to the desired value. The resolution is limited by capacitor mismatch, parasitic capacitance in routing, and bottom-plate capacitance. In this work, a resolution of 0.6 is chosen, comprising a 4b segmented section containing 16 equal capacitors and a 4b binary-weighted section. This combination generates monotonicity even in the presence of 12.5% capacitor mismatch. The second issue relates to the on-resistance of the switches in series with the capacitors. This resistance is chosen to yield a capacitor Q of ten at the oscillation frequency.

The phase detector is similar to that in Reference 5, modified to equalize delays in the inputs of the two exclusive-OR gates. The charge pump implementation is shown in Figure 14.2.4. Since the circuit must provide a differential control for the VCO, it is important that the outputs not drop in the absence of up and down pulses. For this reason, the charge pump turns off all the devices connected to the output nodes when both up and down pulses are low. The common-mode feedback (CMFB) network senses the average differential output, adjusting the on-resistance of M1 and M2. Since this approach results in substantial process and temperature variability, transistor M3, sensing the desired voltage VCM, and the diode-connected device M4 control the gate of M1 [6]. With reasonable matching, the output CM level remains close to VCM.

The clock recovery circuit in digital 0.25um CMOS is shown in Figure 14.2.7. The die has 0.8x0.6m2 active area. Figures 14.2.5 and 14.2.6 show the recovered clock and the jitter histogram in response to a 2.75Gb/s PRBS of length 2^31-1. The rms and peak-to-peak jitter is 0.1ps and 35.8ps, respectively. The output spectrum of the recovered clock depicts -89.2dBc phase noise at 1MHz offset. The capture range is 50MHz and the tracking range, determined by the fine-tuning range, is 45MHz. The circuit operates reliably at data rates to 3Gb/s. Total power dissipation is 50mW from 2.7V power supply.

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References:
Figure 14.2.1: Clock recovery architecture.

Figure 14.2.3: (a) Quadrature coupled LC oscillator; (b) capacitor array for LC tank.

Figure 14.2.5: Recovered clock at 2.756Hz.

Figure 14.2.6: Jitter histogram for PRBS of 2^11.
PLL with
Lock Time
< 120µs

Frequency Range
2.4-2.5GHz

Limited Sensitivity Dynamic Range of RSSI
> 40dB

Demodulator Input Frequency Range
> 400kHz

PLL Feedback Ratio@1MHz offset
24dB

LPF Feedback Ratio@1MHz offset
27dB

PLL with
Freq. Doubler and VCO

Current in Transmit Mode
34.4mA

Current in Recieve Mode
44.0mA

Current in Sleep Mode
< 1µA

Supply Voltage
2.7-3.3V

Table 14.1.1: Performance characteristics of prototype chip.

Figure 13.6.6: Measured output frequency of all TX blocks operation for 00001111 pattern.

Figure 13.6.7: Measurement results for the transceiver.

Figure 13.7.7: Die micrograph of the receiver.

Figure 14.1.6: Chip micrograph.

Figure 14.2.7: Die micrograph.