CMOS Transceivers at 60 GHz and Beyond [1]

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Abstract

The integration of millimeter-wave transceivers in CMOS technology can benefit from sophisticated signal processing and calibration techniques already is use at lower frequencies. This paper describes a CMOS heterodyne receiver with on-chip LO and frequency divider that achieves a noise figure of 6.9-8.3 dB while consuming 80 mW. A frequency divider is also presented that operates from 64 to 70 GHz in 0.13-μm CMOS technology with a power dissipation of 6 mW.

I. Introduction

The convergence of computing and communications demands increasingly higher data rates in both wireline and wireless media. While wireless systems in the 2-10 GHz band have demonstrated data rates approaching 1 Gb/s, it appears that multi-gigabit-per-second communications would require greater channel bandwidths than presently available below 10 GHz. For example, the 7-GHz unlicensed band around 60 GHz proves attractive for this purpose. Another important motivation for moving up to such frequencies relates to the small size and hence integrability of the antenna. Also, automotive radar applications operating at 75 GHz dictate highly-integrated, low-cost solutions.

This paper presents circuit and architecture techniques that enable millimeter-wave design in CMOS technology. Section II reviews some properties of communication at 60 GHz. Section III deals with receiver design, and Section IV describes an architecture for high-speed frequency dividers.

II. Communication at 60 GHz

While line-of-sight communication may appear to limit the utility of the 60-GHz band, we note that, if transceivers with low power dissipation and small form factor can be designed, then many of them can be distributed in an indoor environment to reestablish communication when a link fails due to obstruction. Such transceivers would also require small antennas, which are readily afforded by the choice of millimeter wavelengths.

The integration of small antennas on-chip further reduces the form factor of transceivers. While somewhat lossy, on-chip antennas offer many other significant benefits: (1) they obviate the need for expensive and lossy millimeter-wave packaging; (2) they lend themselves to differential operation, transmitting a greater power for a given voltage swing; (3) the receive and transmit paths can incorporate separate antennas to avoid the use of lossy transmit/receiver switches; (4) the transmitter need not be ac-coupled to the antenna; (5) the high-frequency pads need no ESD protection; (6) the antennas can serve in a beamforming array, raising the output power. The last property is particularly important because, with the low supply voltage of deep submicron devices, it is much simpler to construct a multitude of low-power transmitters than one high-power counterpart.

III. Receiver Design

Recent work has demonstrated millimeter-wave CMOS building blocks such as low-noise amplifiers (LNAs) and mixers [1, 2] and oscillators [3]. However, the integration of these building blocks to form transceivers poses additional constraints on the design of the circuits. For example, a direct-conversion receiver would require at least two inductors for the LNA, one inductor for each quadrature mixer, at least two inductors for the quadrature oscillator, and at least one inductor for the first divider in the synthesizer loop. With the large foot print of the inductors, the 60-GHz quadrature phases of the LO must travel a long distance before reaching the mixers (or, if the mixer transistors are placed next to the LO transistors, the RF signal must travel a long distance to reach the mixers.) Under these conditions, both the loss and the mismatches contributed by the long interconnects degrade the performance of the LO and the receiver considerably. Insertion of buffers between the LO and the mixers does not resolve the mismatch issues as the buffers themselves must incorporate inductors.

This section presents a heterodyne receiver [4] that avoids quadrature separation at millimeter-wave frequencies, minimizing the length of critical interconnects and allowing the integration of all high-frequency building blocks.

A. Architecture

Figure 1 shows the receiver architecture, where the RF mixer is directly driven by the LO, and the IF mixers by half of the LO frequency. Several aspects of the architecture merit consideration. First, in contrast to a 60-GHz quadrature LO required in direct conversion, the oscillator used here must operate at 40

[1] This work was supported by Realtek Semiconductor, Skyworks, Inc., and DARPA.

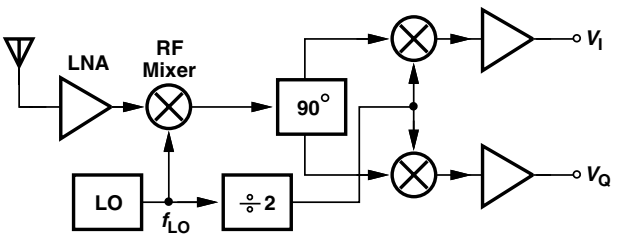

Fig. 1. Receiver architecture.

GHz and provide only differential outputs, potentially achieving a lower phase noise especially because the Q of varactors appears to fall below that of inductors at high frequencies. Second, the choice of $\div 2$ over $\div 4$ is governed by the level of image rejection that can be achieved by the selectivity of the front end. Third, even though directly tied to the RF mixer, the LO is not pulled by in-band interferers because they bear a frequency difference as high as $f_{RF}/3$ with respect to f_{LO}. Fourth, the $\div 2$ circuit must operate at a nominal frequency of 40 GHz, dictating either an injection-locked topology, which suffers from a narrow lock range and hence poses risks on the overall design, or a Miller regenerative topology, which does not readily produce quadrature phases. In this work, a Miller divider is chosen and the quadrature phase shift is performed in the IF signal path. As explained below, I/Q separation in the current domain negligibly affects the noise figure and gain of the receiver.

B. Building Blocks

Figure 2 shows the implementation of the front end. A cascode LNA is followed by a transconductance stage and a single-balanced mixer. The capacitances introduced by M_1 and M_2 at node X severely limit the bandwidth and raise the

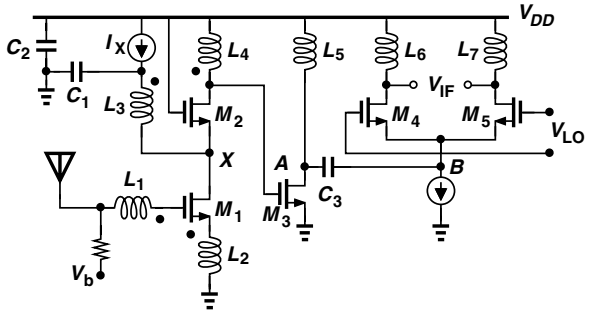

Fig. 2. Implementation of front end.

contribution of M_2 to the output noise. Thus, in a manner similar to the mixer design in [1], an inductor is added to X to resonate with the total capacitance at this node. Current source $I_X (\approx 0.25 I_{D1})$ provides flexibility in the noise and gain optimization of the stage.

The magnetic coupling factors indicated between $L_1 (= 180$ pH) and $L_2 (= 60$ pH) and between $L_3 (= 192$ pH) and $L_4 (= 287$ pH) result from "nesting" these inductors. For example, L_2 is enclosed by L_1 so as to minimize the length of high-frequency interconnects.

The return paths of the signal currents carried by L_3, L_4, and $L_5 (= 192$ pH) must be chosen carefully so that parasitic inductances do not degrade the Q or raise the value of these components. This is accomplished by means of metal sandwich capacitors C_1 and C_2, which are tied to a wide ground plane that travels 100 μm and connects to the input ground pads.

In order to accommodate a nominal center frequency of 60 GHz, the mixer may employ an inductor tied to the common-source node of the switching pair while carrying some of the bias current of the input transconductance device [1]. However, in the presence of mismatches between current sources, it becomes difficult to guarantee a well-defined current through the switching pair. To resolve this issue, the front end of Fig. 2 capacitively couples the signal current of M_3 to the mixer core while L_5 resonates with the capacitances at nodes A and B. Thus, the noise and nonlinearity performance of M_3 is decoupled from the switching efficiency of M_4 and M_5. The load inductors L_6 and L_7 (realized as one symmetric structure) provide both conversion gain and suppression of the LO (which would otherwise desensitize the IF mixers.)

Figure 3 depicts the IF mixers. As with the RF mixer, this

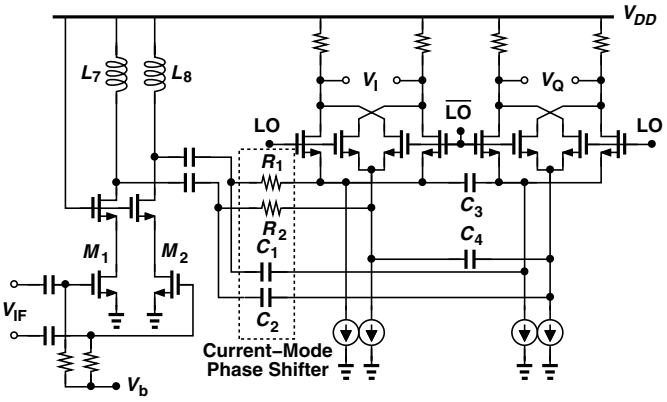

Fig. 3. IF mixer.

circuit isolates the bias of the switching transistors from that of the input transconductance stage. The IF current generated by this stage is applied to a current-mode quadrature phase separation network R_1-R_2 and C_1-C_2, with the resulting outputs commutated by the switching quads. Since the finite impedance seen at the common source nodes of the switching quads introduces a small error in the phase separation, capacitors C_3 and C_4 are added to provide partial correction.

While splitting the IF current between the two switching quads, the phase shift network does not degrade the overall gain or noise figure significantly. This can be seen by viewing M_1 or M_2 in Fig. 3 as equivalent to two transistors in parallel, which would be required in typical quadrature down conversion mixers driven by quadrature LO phases. In other words, it is as if the input transconductance stages of two mixers are merged into one.

The receiver has been fabricated in 90-nm digital CMOS technology and tested on a high-frequency probe station. Figure 4 shows the die, whose active area measures approximately 400 μm $\times$ 300 μm. Figure 5 plots the measured noise figure,

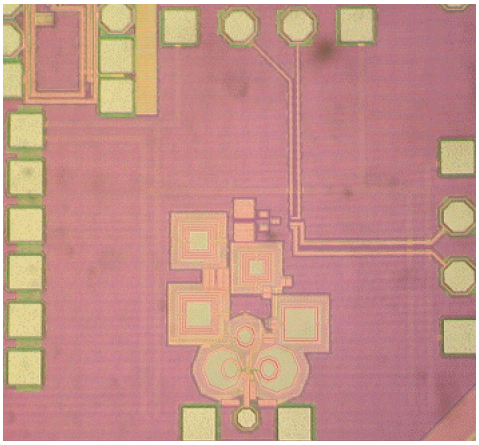

Fig. 4. Receiver die photograph.

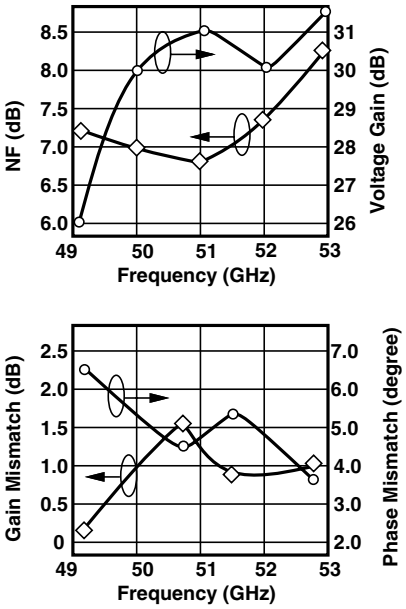

Fig. 5. Measured receiver performance.

voltage gain, and gain and phase mismatch as a function of the input frequency. The receiver consumes 80 mW, a factor of 5.6 lower than that of the 60-GHz BiCMOS receiver reported in [5] for the same functionality and roughly the same performance.

IV. Frequency Division

While the receiver architecture described above employs a 40-GHz LO and divider chain, other architectures or future applications may require frequency division at higher speeds. This task faces serious challenges as flip-flop-based topologies fail and only narrow-band alternatives emerge as a viable solution. These alternatives include the Miller regenerative topology and injection-locked oscillators, both of which suffer from a narrow lock range at very high frequencies. For example, the injection-locked divider in [6] achieves a lock range of about 1.5% if no external tuning is applied. Furthermore, these topologies do not readily lend themselves to divide ratios greater than 2 [7].

A. Heterodyne Phase-Locking

This section presents the concept of "heterodyne phase-locking," a technique that can be used to construct high-speed dividers with arbitrary integer or fractional divide ratios [8]. Consider the phase-locked loop (PLL) shown in Fig. 6, where

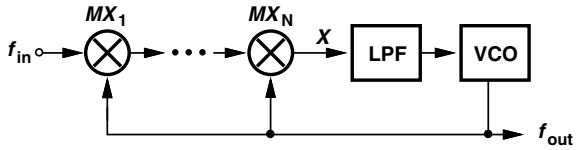

Fig. 6. Heterodyne phase-locked loop.

the phase detector (e.g., a single mixer) is replaced with a cascade of N mixers that are driven by the voltage-controlled oscillator (VCO) output. It is assumed that each mixer is followed by mild filtering to remove the sum frequency generated by that mixer. In a manner similar to a heterodyne receiver, this cascade downconverts the input N times, producing a dc component at node X if $f_{in} = N f_{out}$. In other words, if the loop locks, then $f_{out} = f_{in}/N$.

Heterodyne phase-locking offers a number of advantages over other frequency division techniques. First, a divide ratio of, say, 3 is as easily afforded as a divide ratio of 2 - a sharp contrast to flip-flop-based and injection-locked topologies. In fact, as N increases, the only trade-offs arise from the necessary reduction of the loop bandwidth, which is tolerable so long as the settling of the PLL is much faster than that of the synthesizer in which it is embedded, and the higher loading imposed on the oscillator, which can be accommodated because the oscillator operates at a proportionally lower frequency.

The second advantage is associated with the lock range. Using a relatively high loop gain (while maintaining a reasonable phase margin), the PLL can achieve a lock range almost equal to the tuning range of the oscillator, which is typically 5 to 10 times the lock range of an injection-locked divider. Note that external (discrete or continuous) tuning techniques applied to injection-locked dividers [1, 2] can be used here as well to further widen the lock range.

The third advantage relates to the output phase noise. While injection-locked dividers suffer from a trade-off between the tank Q and the lock range and produce greater phase noise as the circuit approaches the edge of the lock range, heterodyne PLLs entail no such trade-offs if their loop gain remains high.

Heterodyne phase-locking can also provide fractional divide ratios. If a $\div M$ circuit is inserted in the feedback path of Fig. 6, then $f_{out} = M f_{in}/N$. In a more general topology, the LO and RF ports of some of the mixers can be preceded with dividers to realize various fractional divide ratios.

B. Divide-by-Two Example

To demonstrate the potential of heterodyne phase-locking, a divide-by-two circuit has been designed in 0.13-μm CMOS technology. Figure 7 shows the first mixer circuit diagram.

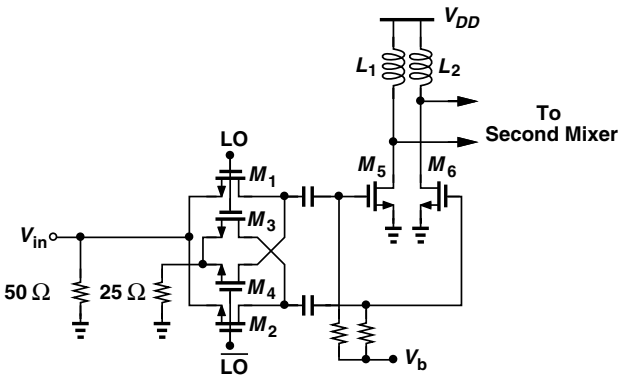

Fig. 7. First mixer.

Early simulations indicated that, for a given input capacitance and input voltage swing, passive mixers followed by amplifiers provide a greater gain across a wider frequency range than do active mixers. This is partly due to the nearly rail-to-rail swings provided by the VCO. Thus, M_1-M_4 downconvert f_{in} to $f_{in}/2$, applying the result to the tuned stage consisting of M_5-M_6 and L_1-L_2. A double-balanced mixer is chosen as it would receive differential inputs when following an on-chip oscillator, but for test purposes, one input is tied to ground through a 25-Ω resistor. With their small dimensions ($W/L = 2.5\mu$m/0.13 μm), M_1-M_4 present little capacitance at the input or to the VCO.

Shown in Fig. 8, the second mixer incorporates PMOS

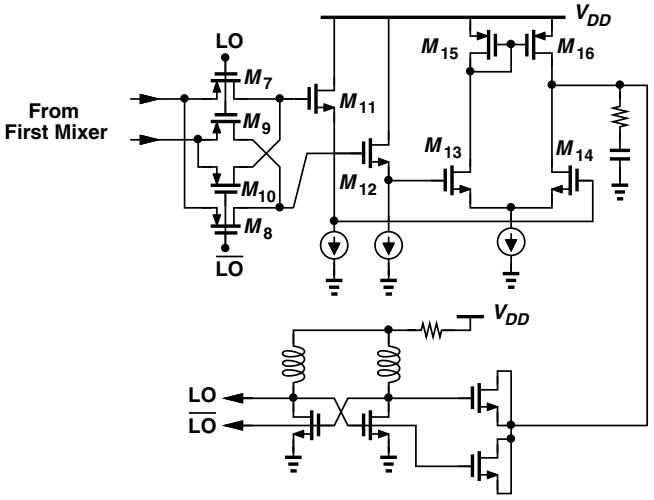

Fig. 8. Second mixer and VCO.

devices M_7-M_{10} to both avoid capacitive coupling and bias the gates of the source followers M_{11}-M_{12} at V_{DD}. The level shift provided by the followers allows the amplifier M_{13}-M_{16} to sustain large output swings, thus maximizing the tuning range of the VCO.

Simulations reveal a lock time of 40 ns for the divider, suggesting that it would negligibly affect the stability of typical synthesizer loops.

The circuit has been fabricated in 0.13-μm CMOS technology and tested with a 1.2-V supply and an input swing of -2 dBm. Figure 9 shows the die, which occupies an active area

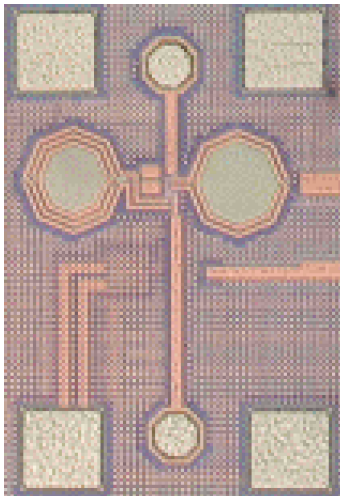

Fig. 9. Divider die photograph.

of 200 μm $\times$ 100 μm. The circuit achieves a lock range of 64 GHz to 70 GHz with the -2-dBm input swing.

Figure 10 plots the signal source phase noise and the output

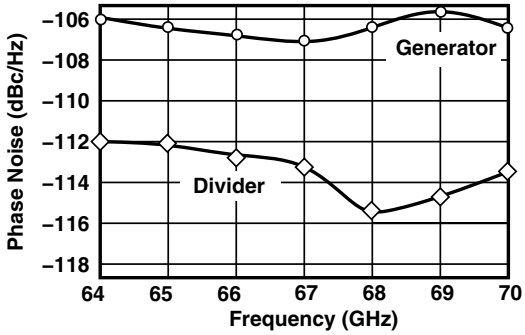

Fig. 10. Measured phase noise of divider.

phase noise across the lock range, indicating little change in the phase noise suppression provided by the PLL.

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