Multi-Decade Carrier Generation for Cognitive Radios[1]

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Abstract—A bimodal quadrature oscillator and three divider chains produce carrier frequencies in the range of 1 GHz to 10 GHz in quadarature form and can also be used to cover lower decades. Fabricated in 90-nm CMOS technology, a prototype consumes 31 mW and exhibits a phase noise of −120 dBc/Hz at 1.75 GHz and −93 dBc/Hz at 8.75 GHz at 1-MHz offset.

Future cognitive radios are expected to perform spectrum sensing, transmission, and reception across two to three decades of frequencies. As such, these radios will require both a broadband signal path and a multi-decade frequency synthesizer. While considerable effort has been expended on enlarging the signal path bandwidth, the problem of wideband synthesis has persisted. This issue proves particularly difficult in cognitive radios as spurious components accompanying the carrier can lead to false detection in spectrum sensing.

This paper describes a carrier generation architecture that covers one decade of frequencies and can be readily extended to produce lower decades as well.

Wideband carrier synthesis for cognitive radios must deal with three issues: (1) each frequency component must be produced in quadrature form while avoiding lossy, power-hungry polyphase filters; (2) due to its large spurious content, single-sideband (SSB) mixing must be avoided; (3) to achieve a reasonable phase noise, the tuning range of the oscillator(s) must remain below approximately $\pm 15\%$.

Based on these observations, the architecture shown in Fig. 1(a) is proposed. It consists of a "bimodal" quadrature local oscillator (LO) and four divider paths generating f_{LO}/N, where $N = 2, 3, 4, 5, 6, 7, 8, 10$. Note that all outputs are in quadrature form. As explained below, the bimodal LO generates one of two discrete values, $f_{LO1} = 17.5$ GHz and $f_{LO2} = 14$ GHz in the prototype, and can also be tuned by varactors around each of these values.

Figure 1(b) depicts all of the center frequencies generated in this design. We note that the frequency range of 1 GHz to 10 GHz can be covered with a worst-case tuning range of $(10\text{ GHz} - 8.75\text{ GHz})/8.75\text{ GHz} = 14\%$. Under this condition, the lower center frequencies require a tuning range of no more than $\pm 11\%$ to maintain continuity across the decade. To fill the gaps between 1 GHz and 1.4 GHz and between 1.4 GHz and 1.75 GHz, the available components in the range of 2 GHz to 3.5 GHz can be simply divided by 2. Also, as shown in Fig. 1(a), lower decades can be generated by repeating this architecture with $f_{LO}/8$ and $f_{LO}/10$ as its inputs.

The proposed architecture derives its simplicity from both the bimodal operation of the LO and the ability of each divider to generate quadrature outputs. Figure 2(a) shows the bimodal oscillator introduced in this work. (The quadrature LO employs two instances of this circuit with unilateral coupling between them.) The oscillator consists of a cross-coupled pair, M_1-M_2, and buffer pairs, M_3-M_4 and M_5-M_6. In a given mode, only one buffer is enabled by the mode select command. In contrast to the topologies in [1, 2], the two discrete modes are created by means of mutual coupling between the load inductors of the core and the buffer and changing the *polarity* of this coupling by enabling either buffers. It can be shown that, for a given choice of L_1, L_2, the capacitances at nodes A-D, I_{SS}, and I_{buf}, there exists a range of the coupling factor that guarantees stable oscillation in both modes.

The mutual coupling between L_1 and L_2 is established by "nesting" them [3]. Illustrated in Fig. 2(b) for the overall quadarature LO, this approach also substantially shortens the high-frequency interconnects between the LO and the dividers.

In order to generate divided outputs with quadrature phases, this work utilizes the Miller divider proposed in [4]. Shown in Fig. 3 is the $\div 5$ loop, which employs an SSB mixer and a $\div 4$ chain, reaching stable operation if $(f_{LO} - f_{out})/4 = f_{out}$ and hence $f_{out} = f_{LO}/5$. It can be shown that the SSB mixer spurs appearing at node A are translated to zero or $f_{LO}/5$ as they travel to the output.

It is tempting to utilize the intermediate frequencies available at the internal nodes of the $\div 3$ and $\div 5$ circuits—as the topology in [4] does to obtain a ratio of 2.5. Unfortunately, however, these nodes exhibit significant sidebands arising from the LO feedthrough of the mixers. For example, as illustrated in Fig. 4, the LO feedthrough in the $\div 5$ circuit can be considered the sum of FM and AM components, the latter of which is removed by the limiting action of the first $\div 2$ stage, thereby yielding another spur at $3f_{LO}/5$. Upon division by 2, the two spurs emerge around $2f_{LO}/5$.

The architecture of Fig. 1(a) has been realized in 90-nm CMOS technology. Figure 5 shows the active area of the die, which measures 530 μm×550 μm. The highest power consumed by the circuit occurs when $f_{LO}/8$ is produced (i.e., the topmost divider chain is enabled) and is equal to 31 mW. As an example, Fig. 6 shows the output spectrum of the $\div 5$ circuit in the high mode, revealing a phase noise of −102 dBc/Hz at 1-MHz offset. Figure 7 plots the measured phase noise of each output component at 1-MHz offset.

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References

[1] Bevilacqua et al, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE TCAS II*, pp. 293-297, Apr. 2007.

[2] J. Borremans et al, "A compact wideband front end using a single-inductor dual-band VCO in 90-nm digital CMOS," *IEEE JSSC*, pp. 2693-2705, Dec. 2008.

[3] B. Razavi, "CMOS transceivers for the 60-GHz band," *IEEE RFIC*

Symp., pp. 231-234, June 2006.
[4] C.-C. Lin and C.-K. Wang, "A regenerative semi-dynamic frequency divider for mode-1 MB-OFDM UWB hopping carrier generation," *ISSCC Dig. Tech. Papers,* pp. 206-207, Feb. 2005.

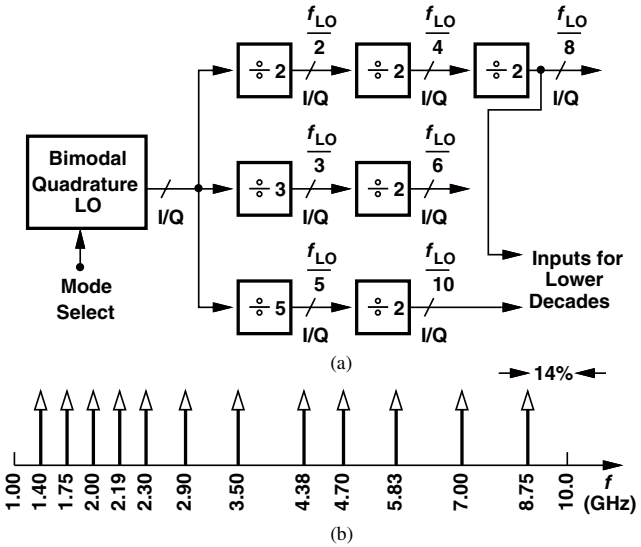

Fig. 1. (a) Architecture of carrier generator, (b) output frequencies.

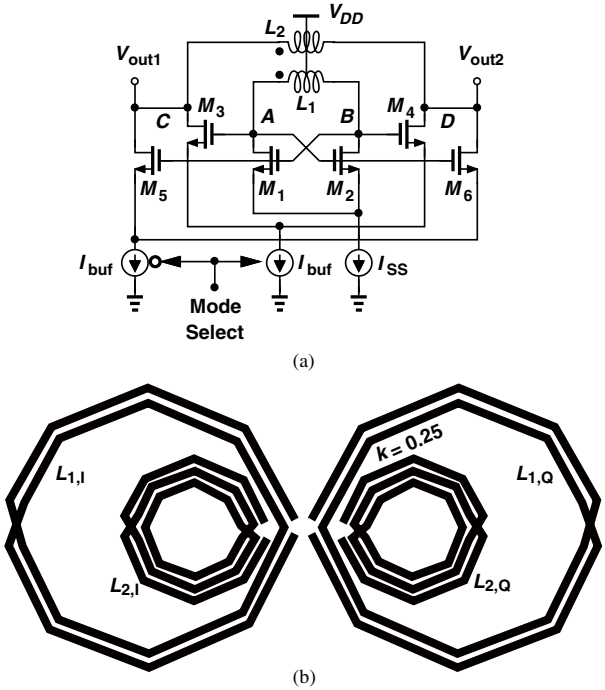

Fig. 2. (a) Bimodal oscillator, (b) layout of inductors.

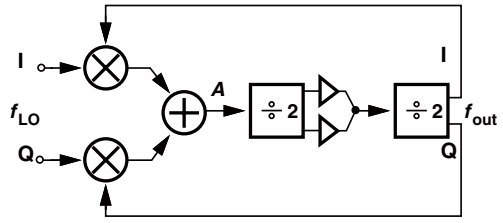

Fig. 3. Divide-by-5 realization.

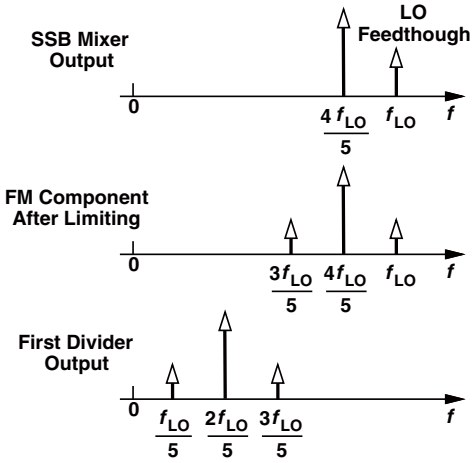

Fig. 4. Spurs at internal nodes of ÷5 circuit.

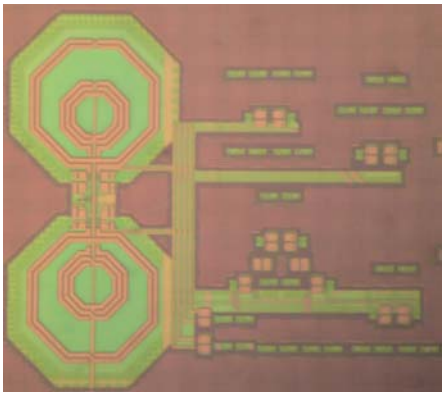

Fig. 5. Die photograph.

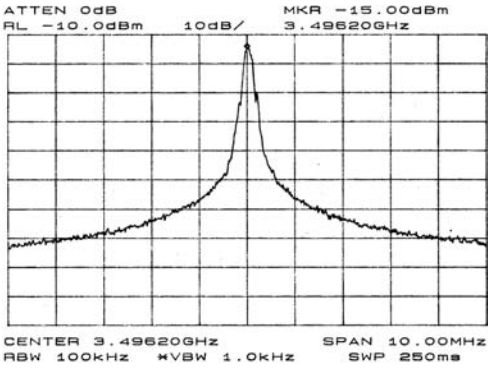

Fig. 6. Output spectrum of ÷5 circuit.

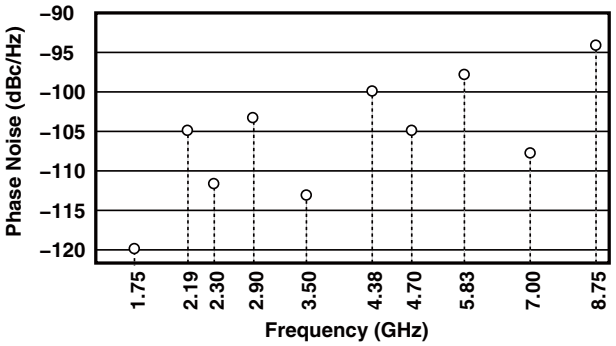

Fig. 7. Phase noise of each output at 1-MHz offset. (Both LO modes generate 3.5 GHz; phase noise of $f_{LO2}/4$ is shown.)