

# Lower Bounds on Power Consumption of Clock Generators for ADCs

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## Abstract

**This paper formulates the jitter-power trade-offs in the design of phase-locked loops that provide the sampling clock for ADCs. We obtain lower bounds for the oscillator power consumption in terms of the performance penalty allowed for the ADC. We show that the oscillator power grows with the square of the target signal-to-noise ratio and the square of the clock frequency and is expected to exceed that of the ADC in future designs.**

## I. INTRODUCTION

Nyquist-rate analog-to-digital converters (ADCs) continue to achieve higher speeds and resolutions [1]-[4], intensifying the problem of clock jitter. A 10-bit 10-GHz ADC incurs a 1-dB penalty in its signal-to-noise ratio (SNR) if its clock contains 12.9 fs of rms jitter. How much power will a 10-GHz phase-locked loop draw to meet this jitter requirement? This paper analyzes a “best-case” scenario to derive lower bounds for this power consumption, demonstrating that the PLL can in fact burn more power than the ADC.

Section II formulates the ADC SNR penalty in terms of the clock jitter, and Section III describes our analysis framework. Section IV derives the lower bound if only oscillator phase noise is taken into account. Section V repeats the analysis while including the reference phase noise as well. Section VI examines the results and Section VII presents numerical calculations, predicting alarming trends. Sections VIII and IX provide additional insights into the trade-offs.

## II. ADC SNR PENALTY DUE TO JITTER

For an analog input of the form  $A_{in} \cos \omega_{in} t$  sampled at  $f_{CK} = 2f_{in} = 2(\omega_{in}/2\pi)$ , the jitter-induced noise power,  $P_j$ , is given by

$$P_j = 2\pi^2 A_{in}^2 f_{in}^2 \sigma_j^2, \quad (1)$$

where  $\sigma_j$  denotes the rms clock jitter [5]. Suppose  $P_j$  is so chosen as to yield an  $m$ -dB SNR penalty for the ADC. Denoting the quantization noise power by  $P_q$ , we have

$$\frac{P_q + P_j}{P_q} = 10^{m/10}, \quad (2)$$

and hence  $P_j/P_q = 10^{m/10} - 1$ . We also define a jitter-less ADC SNR as

$$\text{SNR}_0 = 6.021M + 1.761 \text{ dB}, \quad (3)$$

where  $M$  denotes the resolution. The sampler SNR is given by  $(4\pi^2 f_{in}^2 \sigma_j^2)^{-1}$ . The latter must be sufficiently higher than the former to allow the tolerable penalty. In fact, we must have

$$\frac{1}{4\pi^2 f_{in}^2 \sigma_j^2} = \frac{\text{SNR}_0}{10^{m/10} - 1}. \quad (4)$$

Since  $f_{in} \approx f_{CK}/2 = (1/T_{CK})/2$ , we obtain

$$\frac{1}{\pi^2} \left( \frac{T_{CK}}{\sigma_j} \right)^2 = \frac{\text{SNR}_0}{10^{m/10} - 1}. \quad (5)$$

For example, a 10-bit 10-GHz ADC with  $\text{SNR}_0 = 61.967 \text{ dB} \equiv 1.574 \times 10^6$  experiences a penalty of  $m = 1 \text{ dB}$  if  $\sigma_j = 1.29 \times 10^{-4} T_{CK} = 12.9 \text{ fs}$ .

We should point out that  $\text{SNR}_0$  does not account for other ADC imperfections, such as nonlinearity and thermal noise. In practice, we can simply use the actual jitter-free SNR of a given ADC in the derivations that follow.

## III. ANALYSIS FRAMEWORK

We consider a simple integer- $N$  PLL that multiplies a crystal oscillator’s frequency,  $f_{REF}$ , by  $N$  to produce  $f_{CK}$  (Fig. 1). As a best-case scenario, we neglect all noise sources except for the reference and the voltage-controlled oscillator (VCO). The reference spurs are also neglected. The output thus contains two phase noise profiles:  $S_{REF}$  multiplied by  $N^2$  and low-pass filtered by the PLL, and the shaped VCO phase noise.

We make the following approximations: (1) flicker noise is negligible, (2) the PLL acts as a first-order filter on  $S_{REF}$  with a  $-3$ -dB bandwidth of  $f_1$ , (3) the shaped VCO phase noise exhibits a plateau up to  $\pm f_2$  with a spectral density of  $S_1$ , where  $S_1$  is equal to the free-running VCO phase noise evaluated at an offset frequency of  $f_2$ , and (4)  $f_1 \approx f_2$ , a good approximation if the PLL damping factor,  $\zeta$ , exceeds approximately 2. The same condition also allows approximating the VCO shaped phase noise by a plateau for  $|f| < f_2$ .

Our goal is to compute the VCO power consumption in two cases:  $S_{REF}$  is negligible or significant. The resulting values constitute lower bounds because the other building blocks’ noise and power consumption are neglected.

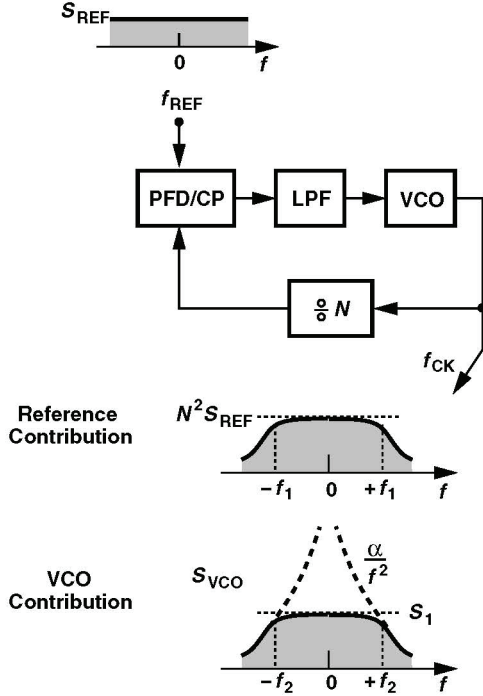


Fig. 1. Integer-N PLL showing output phase noise due to reference and VCO.

## IV. LOWER BOUND DUE TO VCO PHASE NOISE

### A. PLL Jitter Due to VCO

Returning to Fig. 1, we note the area under  $S_{VCO}$  is given by  $2S_1 f_2$  from  $-f_2$  to  $+f_2$ . In addition, if the VCO phase noise arises from only thermal noise and hence falls in proportion to  $f^2$ , the areas under the tails also add up to  $2S_1 f_2$ . To express the total area,  $4S_1 f_2$ , in seconds squared, we multiply it by  $T_{CK}^2/(4\pi^2)$ :

$$\sigma_j^2 = 4S_1 f_2 \left( \frac{T_{CK}}{2\pi} \right)^2. \quad (6)$$

### B. VCO Phase Noise

As a representative topology, we consider the LC VCO shown in Fig. 2, where  $R_p$  models the finite quality factor,  $Q$ ,

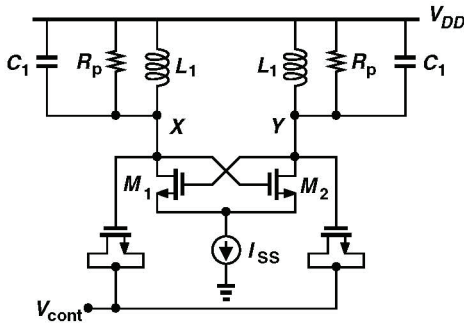


Fig. 2. Simple cross-coupled VCO.

of the tanks. We neglect the noise in  $I_{SS}$  and the flicker noise

of  $M_1$  and  $M_2$ . The free-running phase noise is given by [6]:

$$S(f) = \frac{\pi^2 kT(1+\gamma)}{2R_p I_{SS}^2} \left( \frac{f_{CK}}{2Qf} \right)^2, \quad (7)$$

where  $\gamma$  denotes the MOS excess noise coefficient and  $f$  is the offset frequency. Let us assume that the single-ended peak-to-peak voltage swing,  $(4/\pi)I_{SS}R_p$ , is approximately equal to  $V_{DD}/2$ . Denoting the VCO power consumption,  $I_{SS}V_{DD}$ , by  $P_{VCO}$ , we have

$$S(f) = \frac{4\pi kT(1+\gamma)}{P_{VCO}} \left( \frac{f_{CK}}{2Qf} \right)^2. \quad (8)$$

We now evaluate  $S(f)$  at  $f_2$  to obtain  $S_1$  in Fig. 1 and substitute the result in Eq. (6):

$$\sigma_j^2 = \frac{kT(1+\gamma)}{\pi P_{VCO} Q^2} \frac{1}{f_2}. \quad (9)$$

As expected, a greater  $f_2$  (a wider PLL bandwidth) translates to a lower jitter or a lower VCO power consumption.

### C. Lower Power Bound

The jitter expressed by (9) must meet the constraint stipulated by (5) for the ADC to incur  $m$  dB of SNR penalty. Substituting the former in the latter yields

$$P_{VCO} = \frac{\text{SNR}_0}{10^{m/10} - 1} \frac{\pi kT(1+\gamma)}{Q^2} \frac{f_{CK}^2}{f_2}. \quad (10)$$

For example, a 1-dB penalty in a 10-bit 10-GHz ADC demands a VCO power consumption of 15.8 mW if  $\gamma = 1$ ,  $Q = 10$ , and  $f_2 = 10$  MHz. To compare with the 12-bit 5-GHz 159-mW ADC in [4], we have  $\text{SNR}_0 = 74$  dB,  $f_{CK} = 5$  GHz, and hence  $P_{VCO} = 63$  mW with  $Q = 10$  and  $f_2 = 10$  MHz. We observe that  $P_{VCO}$  is no longer negligible with respect to the ADC power. As explained below, the situation is much more severe when the reference phase noise is also taken into account.

## V. EFFECT OF REFERENCE PHASE NOISE

### A. Optimum Loop Bandwidth

The choice of  $f_2 = 10$  MHz in the previous section appears somewhat arbitrary. In a typical PLL,  $f_2$  is around  $f_{REF}/10$  or less. In low-jitter PLL design, on the other hand,  $f_1$  and  $f_2$  in Fig. 1 must be so selected as to minimize the sum of the reference and VCO phase noise contributions. We now derive a simple expression for the optimum PLL bandwidth.

With the one-pole PLL approximation stipulated in Section III, we can express the output phase noise profile due to the reference as

$$S_{out,REF}(f) = \frac{N^2 S_{REF}}{1 + \frac{f^2}{f_1^2}}. \quad (11)$$

Integrating this function from  $-\infty$  to  $+\infty$  yields a value of  $\pi N^2 S_{REF} f_1$ . We must minimize the sum of this value and that due to the VCO:

$$S_{tot} = \pi N^2 S_{REF} f_1 + 4S_1 f_2. \quad (12)$$

Recall from Eq. (7) that the free-running VCO phase noise is of the form  $\alpha/f^2$ . If  $f_1 \approx f_2$ , the VCO contribution amounts to  $4(\alpha/f_2^2)f_2 = 4\alpha/f_2$ , and

$$S_{tot} \approx \pi N^2 S_{REF} f_2 + 4\frac{\alpha}{f_2}. \quad (13)$$

This total is minimized if

$$f_2 = \sqrt{\frac{4\alpha}{\pi N^2 S_{REF}}}. \quad (14)$$

We can consider this value the optimum “loop bandwidth.” Note that this choice makes the reference and VCO contributions equal, i.e., the two profiles in Fig. 1 coincide, yielding

$$S_{tot,min} = 4\sqrt{\alpha\pi N^2 S_{REF}}. \quad (15)$$

It is important to note that this result equally applies to subsampling PLLs as they too multiply the reference phase noise by  $N^2$ .

### B. Lower Power Bound

We expect that including the reference noise places stricter demands on the VCO phase noise. We must substitute for  $\alpha$  in (15), convert the result to jitter, and apply (5) to determine the SNR-power trade-off. Equation (8) yields

$$\alpha = \frac{\pi kT(1+\gamma)f_{CK}^2}{P_{VCO}Q^2}, \quad (16)$$

and hence

$$S_{tot,min} = 4\sqrt{\frac{\pi^2 kT(1+\gamma)}{P_{VCO}Q^2} N^2 f_{CK}^2 S_{REF}}. \quad (17)$$

Multiplying this result by  $(T_{CK}/2\pi)^2$  and substituting for  $\sigma_j^2$  in (5), we have

$$P_{VCO} = kT(1+\gamma)S_{REF} \left( \frac{\text{SNR}_0}{10^{m/10} - 1} \frac{\pi N f_{CK}}{Q} \right)^2. \quad (18)$$

For example, consider a 10-bit 10-GHz ADC with  $f_{REF} = 100$  MHz and hence  $N = 100$  and  $S_{REF} = -170$  dBc/Hz. For an SNR penalty of  $m = 1$  dB, we require  $P_{VCO} = 300$  mW! This is not surprising as  $f_2$  in Eq. (10) is now reduced from 10 MHz to to 1.05 MHz, necessitating a tenfold increase in the VCO power, and the equal reference and VCO contributions also demand another twofold rise. For the 12-bit 5-GHz 159-mW ADC in [4] to incur 1 dB of SNR penalty due to clock jitter, we have  $P_{VCO} = 19.3$  W!

As mentioned in Section II,  $\text{SNR}_0$  can be replaced with the actual jitter-free SNR if other ADC imperfections are significant.

## VI. DISCUSSION

We can predict that, in the near future, the VCO power consumption will prove a formidable issue because Eq. (18) implies that

$$P_{VCO} \propto f_{CK}^2, \quad (19)$$

whereas for ADC design, we typically have

$$P_{ADC} \propto f_{CK}. \quad (20)$$

Similarly, (18) suggests that

$$P_{VCO} \propto \text{SNR}_0^2, \quad (21)$$

whereas for ADCs,

$$P_{ADC} \propto \text{SNR}_0. \quad (22)$$

Equation (18) also reveals the severity of the reference phase noise problem—even for an optimistic, flat value of  $-170$  dBc/Hz. Moreover,  $f_2 \approx 1$  MHz suggests that the effect of flicker noise may not be negligible.

The dependence of  $P_{VCO}$  upon  $\text{SNR}_0^2$  can be explained intuitively. Suppose we wish to increase the resolution of an ADC by 1 bit, i.e.,  $\text{SNR}_0$  is to rise by a factor of 4. This means that the reference jitter contribution,  $\pi N^2 S_{REF} f_2$ , must fall by this factor, and, therefore, so must  $f_2$ . The VCO must now be redesigned such that its contribution also drops by a factor of 4:

$$\frac{4\alpha}{f_2} \times \frac{1}{4} = \frac{\alpha'}{f_2/4}, \quad (23)$$

where  $\alpha'$  corresponds to the new VCO. It follows that  $\alpha' = \alpha/16$ , requiring from Eq. (16) that

$$P_{VCO} \rightarrow 16P_{VCO}. \quad (24)$$

## VII. NUMERICAL CALCULATIONS

Figure 3 plots the maximum tolerable jitter for a 10-GHz ADC as a function of the resolution for SNR penalties equal to 1, 2, and 3 dB. Even for  $m = 3$  dB, a 12-bit converter can at most tolerate an rms jitter of 6.3 fs.

From the results in Fig. 3, we can determine the optimum PLL bandwidth by simply equating the reference contribution,  $\pi N^2 S_{REF} f_1 T_{CK}^2 / (4\pi^2)$ , to half of the allowable jitter squared. We assume  $N = 100$ ,  $f_{REF} = 100$  MHz,  $Q = 10$ , and  $S_{REF} = -170$  dBc/Hz. The results are plotted in Fig. 4, where the bandwidth is deliberately limited to  $f_{REF}/10 = 10$  MHz if the relaxed jitter allows a greater value.

With the optimum PLL bandwidth known, we can compute the VCO power consumption, as plotted in Fig. 5. We note the enormous increase in  $P_{VCO}$ , especially for resolutions of 10 bits and above.

The following assumptions made in this paper can be revisited: (1) the VCO single-ended swing is  $V_{DD}/2$  but can be raised to  $V_{DD}$  or even greater, possibly at the cost of flicker noise upconversion; (2) tank  $Q$ 's greater than 10 can be sought, and (3)  $f_{REF}$  can be chosen greater than 100 MHz so as to reduce  $N$  in (18), but only if  $S_{REF}$  does not increase. These remedies, however, only postpone the inevitable  $P_{VCO} \propto \text{SNR}_0^2 f_{CK}^2$  trend.

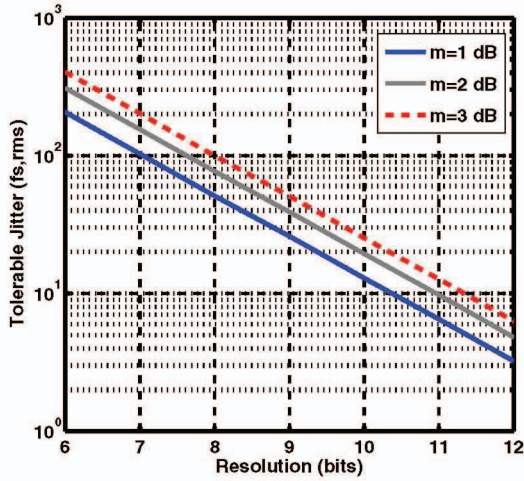


Fig. 3. Tolerable jitter for a 10-GHz ADC for SNR penalties of 1, 2, and 3 dB.

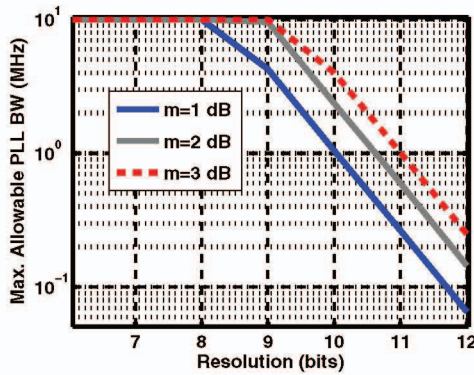


Fig. 4. Optimum PLL bandwidth for obtaining the jitter values shown in Fig. 3.

### VIII. $P_{VCO}$ CALCULATION PROCEDURE

The foregoing developments prescribe a three-step procedure for estimating the necessary  $P_{VCO}$  for a given resolution,

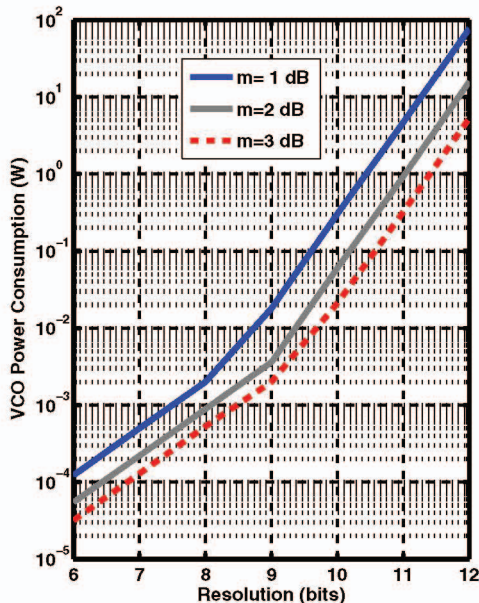


Fig. 5. VCO power consumption for a 10-GHz ADC for SNR penalties of 1, 2, and 3 dB.

sampling rate, and tolerable SNR penalty. First, we obtain the total tolerable jitter from Eq. (5) (Fig. 3), call it  $\sigma_{tot}$ , and allocate half of  $\sigma_{tot}^2$  to the reference and the other half to the VCO. Second, with  $S_{REF}$  known, we obtain the maximum PLL bandwidth by writing

$$\pi N^2 S_{REF} f_2 \frac{T_{CK}^2}{4\pi^2} = \frac{\sigma_{tot}^2}{2}, \quad (25)$$

and hence

$$f_2 = \frac{2\pi\sigma_{tot}^2}{N^2 S_{REF} T_{CK}^2}. \quad (26)$$

This led to Fig. 4. Third, we equate the VCO contribution to  $\sigma_{tot}^2/2$  for a PLL bandwidth equal to  $f_2$ :  $4\alpha/f_2 = \sigma_{tot}^2/2$ , which, for the VCO in Fig. 2, amounts to

$$P_{VCO} = \frac{kT(1+\gamma)}{\pi Q^2} \frac{1}{f_2} \frac{2}{\sigma_{tot}^2}, \quad (27)$$

which led to Fig. 5. Alternatively, we can obtain  $P_{VCO}$  from (18).

### IX. MITIGATING FACTORS

The lower power consumption bounds expressed by (10) and (18) can be relaxed by two factors. First, the jitter-induced noise power given by (1) is in fact pessimistic as it assumes an analog sinusoidal input at Nyquist rate. In practice, a random signal having a flat spectrum from 0 to  $f_{CK}/2$  incurs half of this noise power [8]. Second, the representative VCO in Fig. 2 can be replaced with lower-noise designs. We note that Eq. (8) yields an oscillator figure of merit (FoM) of about 186 dB with  $Q = 10$ , whereas, for example, the class-C topology in [7] achieves an FoM of 196 dB with  $Q \approx 16$ .

### X. CONCLUSION

This paper proposes lower bounds for the VCO power consumption in PLLs that provide the sampling clocks of ADCs. It is shown that this power rapidly rises with the resolution and the sampling rate, posing daunting challenges in the future.

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