U-PAS : A User-Friendly ADC Simulator for Courses on Analog Design

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***Abstract*—A simulator with a graphical user interface has been developed for the analysis and design of pipelined analog-to-digital converters. The user can enter parameters such as resolution per stage, number of pipelined stages, input and clock frequencies, input amplitude, op amp nonlinearity, capacitor mismatch, and comparator offset. The simulator then computes various static and dynamic properties of the system such as residue plots, differential and integral nonlinearity profiles, output spectrum, and input-referred noise. Available as an executable code, the simulator can run on various platforms.**

I. INTRODUCTION

Most advanced courses on analog design include a detailed treatment of pipelined analog-to-digital converters (ADCs). The analysis of this class of ADCs becomes increasingly difficult as various imperfections must be taken into account and their effect must be traced through the stages. Similarly, the design of pipelined ADCs presents tough challenges as the device and supply scaling exacerbates these imperfections, requiring "analog" simulations that may take hours each time.

This paper introduces the **U**CLA **P**ipelined **A**DC **S**imulator (U-PAS), a tool developed in MATLAB during our research on ADCs and subsequently used in our graduate course on the design of data converters. Aiming to expand and enhance the students' understanding of pipelined ADCs, U-PAS runs orders of magnitude faster than circuit simulators. It can therefore readily reveal and quantify the effect of each imperfection in each stage of the pipeline. Operating through a simple and efficient graphical user interface (GUI), the tool performs a comprehensive analysis based on user-specified parameters and produces various types of output characteristics.

Section II of the paper presents the modeling of pipelined ADCs using an approach that lends itself to efficient simulations. Section III presents the simulator interface and Section IV provides examples of simulation results.

II. PIPELINED ADC MODELING ISSUES

Shown in Fig. 1(a), a pipelined ADC consists of N stages that concurrently operate on N consecutive samples of the analog input signal. Each stage digitizes its input, V_{in}, by means of a sub-ADC with a resolution of M bits, thereby producing a digital estimate of V_{in}. This estimate is then returned to the analog domain by a sub-digital-to-analog converter (sub-DAC), and subtracted from V_{in}. Called the "residue", the resulting difference is amplified by a factor of 2^M and applied to the next stage in the pipeline for finer digitization.

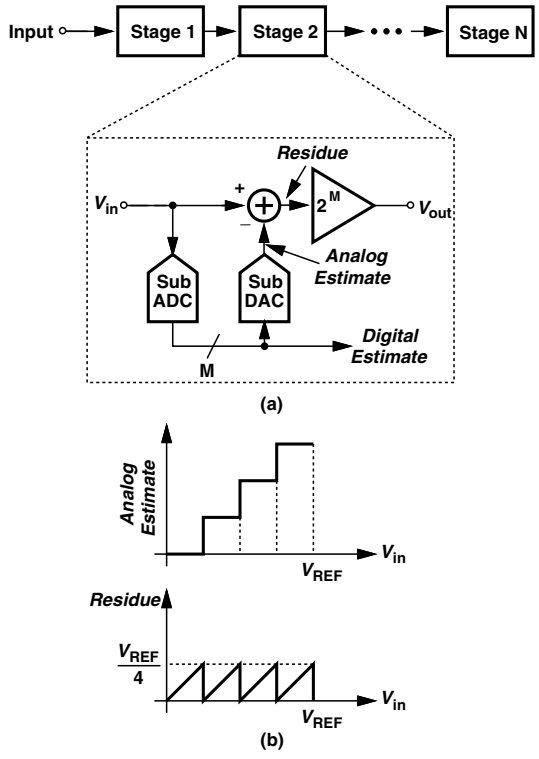

Fig. 1. Pipelined ADC architecture.

Figure 1(b) plots the analog estimate and the residue as a function of V_{in}. In this example, the residue ideally

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begins from zero at integer multiples of $V_{REF}/4$ and linearly rises to a maximum value of $V_{REF}/4$. With device and circuit imperfections, on the other hand, the residue plot experiences various distortions. The principal difficulty in the analysis is that the residue plot becomes increasingly complex for stages farther in the pipeline. As an example, Figure 2 shows a residue plot including the effect of capacitor mismatch and comparator offset in the third stage of an ADC.

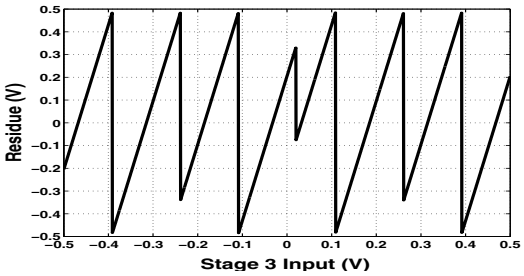

Fig. 2. Residue of third stage of a pipelined ADC.

A common type of pipelined ADCs employs a resolution of 1.5 bits per stage because this choice lends itself to a compact, efficient implementation. Figure 3 depicts a 1.5-bit stage consisting of two comparators (hence the term "1.5 bits") and a switched-capacitor multiply-by-2 circuit called a multiplying DAC (MDAC) [1].

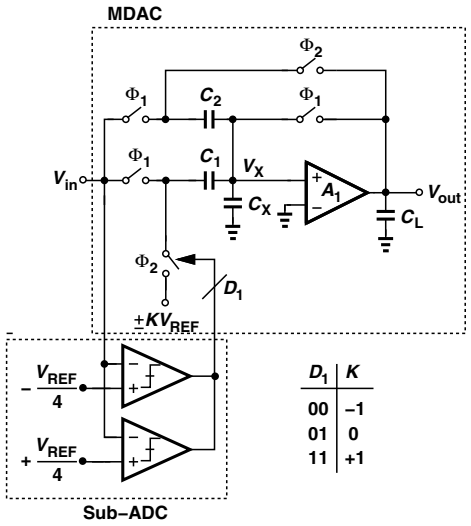

Fig. 3. Pipelined stage with 1.5-bit resolution.

The comparators make a coarse decision, placing V_{in} in one of the three voltage ranges: below $-V_{REF}/4$, between $-V_{REF}/4$ and $V_{REF}/4$, or above $V_{REF}/4$. The MDAC subtracts the sub-ADC output from the input by means of C_1 and produces the amplified residue.

Since op amps realized in deep-submicron CMOS technology suffer from significant nonlinearity, we model the static input-output characteristic of A_1 in Fig. 3 as

$$V_{out} \approx \alpha_1 V_x + \alpha_2 V_x^2 + \alpha_3 V_x^3. \quad (1)$$

It can be shown that the total charge on C_1 and C_2 in the sampling mode is given by

$$Q_{samp} = (C_1 + C_2)V_{in} - (C_1 + C_2 + C_x)V_{x1}, \quad (2)$$

and in amplification mode by

$$Q_{amp} = C_1 K V_{ref} + C_2 V_{out} - (C_1 + C_2 + C_x)V_{x2}. \quad (3)$$

These equations can be readily solved in Matlab to yield the output of each stage in the pipeline.

In addition to static characteristics, U-PAS also models the dynamic behavior of each stage in terms of both linear and nonlinear settling. The linear settling component is based on the small signal model of the MDAC and represented by a single time constant [2]:

$$\tau_{amp} = \frac{C_L(C_1 + C_x) + C_L C_2 + (C_1 + C_x)C_2}{G_m}. \quad (4)$$

The nonlinear settling is modeled by the op amp slew rate, which is calculated from the op amp characteristics provided by the user.

In high-resolution pipelined ADCs, the kT/C noise and the op amp noise must be calculated accurately for all of the stages and summed properly to yield the total input-referred noise and its effect on the signal-to-(noise+distortion) ratio (SNDR). U-PAS incorporates a state-space methodology [3] to determine the noise contributed by each stage and hence the overall SNDR.

III. Simulator Interface

The U-PAS GUI is shown in Fig. 4. The interface accepts the following parameters:

(1) ADC Parameters

– The type of architecture and MDAC (1-bit or 1.5-bit stages; "flip-around" or "non-flip-around" MDAC topologies).

– The overall resolution.

– The input signal amplitude and frequency.

(2) Stage Parameters

– The gain (a) and second-order and third-order nonlinearity coefficients (b and c respectively) of the op amp in each stage.

– The op amp transconductance.

– The capacitors in the MDAC.

– The offsets of the comparators.

– The parasitic input capacitance of the op amp.

– The input-referred offset voltage of the op amp.

Upon entering the parameters (or leaving them at their default values), the user can perform the following analyses:

(1) Static Characteristics

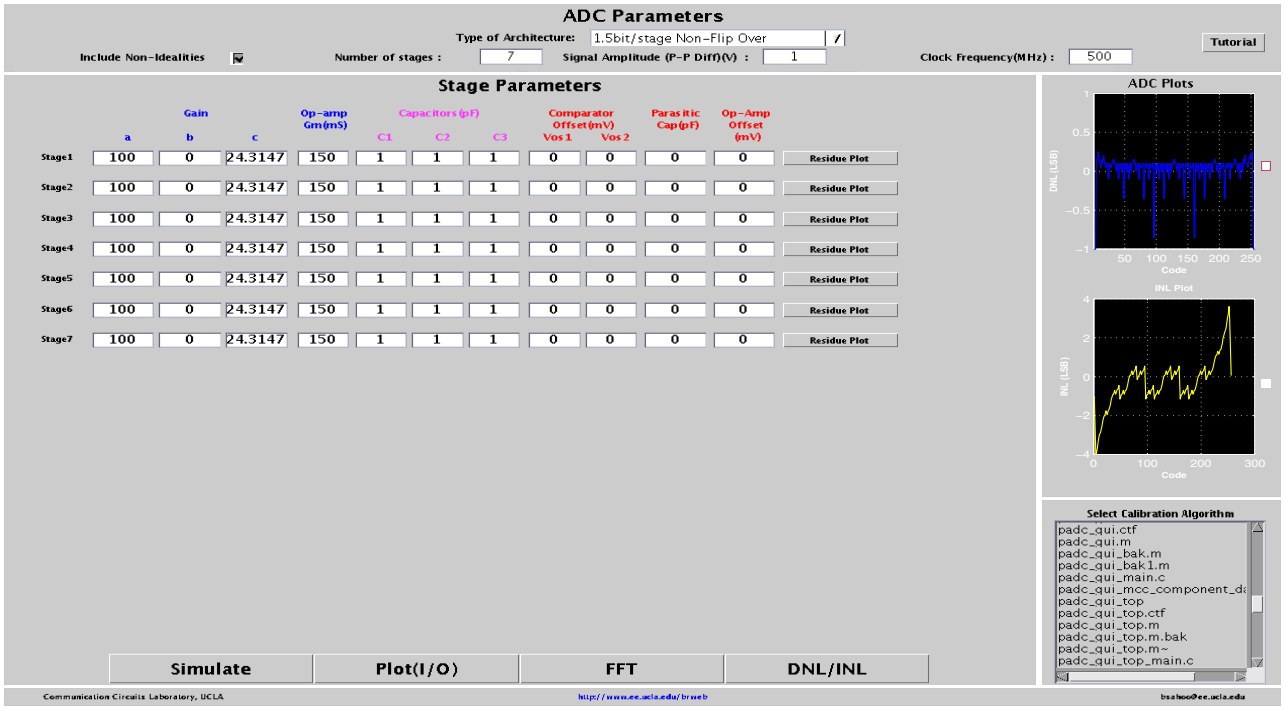

Fig. 4. U-PAS GUI Interface.

– The residue plot at the output of each stage.
– The input-output characteristic of the entire ADC.
– The differential nonlinearity (DNL) and integral nonlinearity (INL) profiles.
(2) Dynamic Characteristics
– FFT of the output in response to a sinusoidal input.
– SNDR and SNR computations.
Additionally, the GUI provides a number of calibration techniques that the user can select and apply so as to determine their effect on the static and dynamic performance. A brief tutorial can also be opened to familiarize the user with the tool's functions.

IV. Simulation Examples

U-PAS runs orders of magnitude faster than circuit simulators while negligibly sacrificing accuracy. For example, the computation of the output FFT of a 10-bit ADC takes more than 20 hours in Cadence's Spectre, 2.5 hours in Ultrasim, and 1.63 seconds in U-PAS.

Figure 5 shows the simulated DNL and INL profiles of an 8-bit ADC including various nonidealities such as capacitor mismatch, comparator offset, and op amp nonlinearity. The DNL and INL plots clearly show missing codes at the comparator thresholds of each stage.

Figure 6 reveals the dynamic behavior of the ADC by plotting the output spectrum for the following cases: (1)$f_{in} = 50$ MHz, $f_{CK} = 500$ MHz; (2)$f_{in} = 245$ MHz, $f_{CK} = 500$ MHz; (3)$f_{in} = 50$ MHz, $f_{CK} = 2$ GHz; (4)$f_{in} = 980$ MHz, $f_{CK} = 2$ GHz. The SNDR degradation in the second case arises from the high analog input slew rate, whereas that in the third case is due to incomplete op amp settling. Since each simulation takes a few seconds, the effect of each parameter in the design can be accurately and effectively quantified.

V. Conclusion

A pipelined ADC simulator greatly enhances the learning experience in advanced analog design courses. Developed as a comprehensive analysis tool, U-PAS also simplifies the design of ADCs by evaluating the static and dynamic performance that can be achieved for a given choice of parameters. The simulator has been successfully used in our graduate course on data converter design.

References

[1] S. H. Lewis and P. R. Gray, "A Pipeline 5 Msamples/s 9-bit Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 22, pp. 954–961, Dec 1987.
[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw Hill, 2001.
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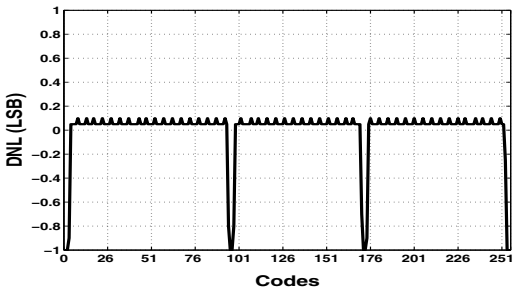
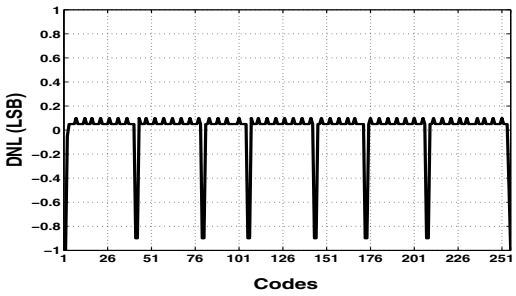


(a)



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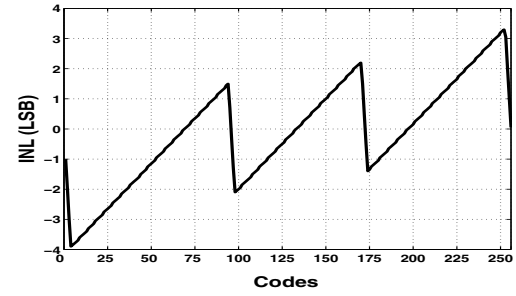

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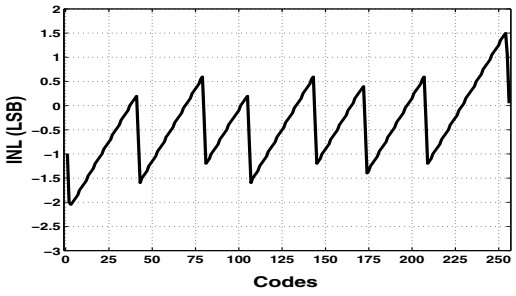
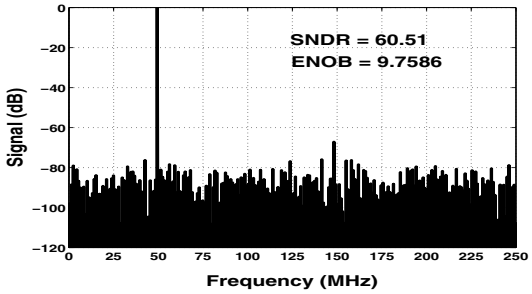


(d)

Fig. 5. DNL and INL for an 8-bit ADC: (a) DNL with non-ideal Stage 1, (b) DNL with non-ideal Stage 2, (c) INL with non-ideal Stage 1, and (d) INL with non-ideal Stage 2.



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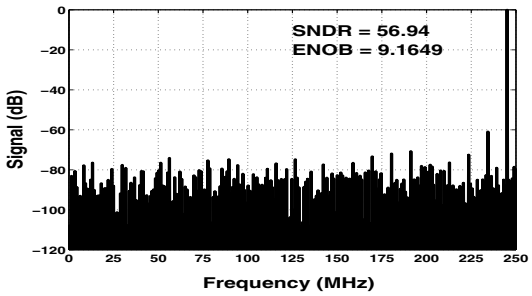

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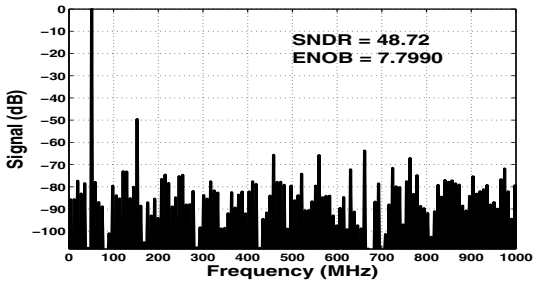

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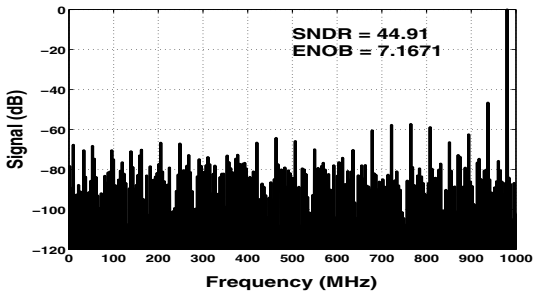

(d)

Fig. 6. FFT spectrum for a 10-bit ADC: (a) $f_{in} = 50$ MHz, $f_{CK} = 500$ MHz , (b) $f_{in} = 245$ MHz, $f_{CK} = 500$ MHz, (c) $f_{in} = 50$ MHz, $f_{CK} = 2$ GHz, and (d) $f_{in} = 980$ MHz, $f_{CK} = 2$ GHz.