18.6 A 2GHz CMOS Image-Reject Receiver with Sign-Sign LMS Calibration

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The trade-off between image rejection and channel selection in heterodyne receivers often restricts the frequency planning and requires external image-reject filters. Hartley and Weaver image-reject architectures partially resolve this issue at the cost of requiring precise phase and gain matching in both the signal path and the local oscillator (LO) path. The use of polyphase filters to improve the matching [1] typically leads to a high power dissipation whereas analog calibration [2] mandates periodic refreshing, a difficult issue in CDMA systems that must receive continuously. In this Weaver receiver, gain and phase mismatches are calibrated simultaneously by a least-mean-square (LMS) algorithm. The receiver targets a sensitivity and blocking performance commensurate with wideband CDMA (WCDMA) systems.

Figure 18.6.1 shows the receiver architecture, where the blocks denoted by Δ are variable-delay stages. An LMS adaptation circuit adjusts the phase and gain of the second downconversion stage without disturbing the RF section. In calibration mode, an image tone is applied at the RF input, the output y(t) is measured, and the coefficients w_1 and w_2 are updated according to the LMS algorithm, in discrete steps, until y(t) approaches zero. The LMS algorithm is given by $w_{1,2}[(m+1)T] = w_{1,2}[mT]+2\mu\varepsilon[mT]x_{1,2}[mT]$ where $w_{1,2}[(m+1)T]$ denotes the values of w_1 and w_2 at discrete-time point $(m+1)T$, μ is the step size, $\varepsilon[mT]$ is the error, and $x_{1,2}[mT]$ represents the values of two input "regressors", i.e., two inputs with which the error must be correlated to determine the change in the coefficients.

Five observations can be made from the receiver architecture shown in Figure 18.6.1. First, two additional mixers, MX_1 and MX_2, multiply the signals at points A and B by one phase of LO_2, thereby generating $x_1(t)$ and $x_2(t)$, respectively. It is important to note that the noise and nonlinearity of MX_1 and MX_2 are unimportant, allowing minimal power dissipation penalty (2.5mW each). Second, the receiver is fully differential, except for the LNA and RF mixers. Moreover, the phase and gain mismatches are controlled differentially to avoid systematic errors. Third, the delay stage Δ_3 duplicates the role of Δ_2, enabling delay lines Δ_1 and Δ_2 to see equal loads. Furthermore, since the delay lines only control the phase of LO_2, whose frequency is about one-tenth of LO_1, they introduce negligible phase noise. Fourth, the LMS algorithm is replaced by the sign-sign (SS) LMS algorithm to reduce hardware complexity. Using the SS-LMS approach, only the signs of the error and the input regressors are multiplied, allowing complicated digital multipliers to be replaced by XOR gates. Finally, the accuracy of calibration or the amount of image suppression is limited by the offset voltage of the comparator used to generate the error signal. Fortunately, the LMS algorithm enables offset cancellation by adding a third coefficient with an input regressor $x_{DC} = 1$. This coefficient (not shown in Figure 18.6.1 but implemented in the prototype) adds or subtracts a differential current in the input stage of the comparator.

The receiver is for the 2.11 to 2.17 GHz WCDMA band. The LNA and RF mixers illustrated in Figure 18.6.2 use a current re-use technique similar to [3] except that two single-balanced quadrature RF mixers are stacked on top of the LNA. With an IF of 200MHz, inductive loads are used for the RF mixers to increase voltage headroom. These 260nH inductors are implemented as stacked spirals [4].

The gain control and phase control in the second downconversion stage must be realized so one does not affect the other as such an interaction may prohibit convergence in the LMS loop. For this reason, the gain control adjusts only a fraction of the gain of the second downconversion mixers. As illustrated in Figure 18.6.3, each mixer is decomposed into a main path and a variable-gain path, the latter scaled-down in both device size and bias current by a factor of 5. Thus, the gain is varied by ±1.5 dB from a nominal main-mixer gain of 8dB. The outputs of the two paths are added in the current domain. The variable-delay stages are similar to those in [2] with ±25° phase adjustment for a 200MHz LO frequency. This wide range accommodates large phase mismatches in the RF and LO paths.

The SS-LMS machine lends itself to a compact mixed-signal implementation (Figure 18.6.4a). To achieve high calibration accuracy, each digital-to-analog converter (DAC) has 11b resolution, providing 0.0017dB gain step, 0.0244° phase step, and a 48.8μV offset step.

In this design, the DACs must provide 11b monotonicity with low complexity. Since speed and integral nonlinearity of the DACs are not critical, a compact, low-power topology is possible. As shown in Figure 18.6.4b, the binary input is decomposed and converted into a 6b coarse 1-of-n code and a 5b fine 1-of-n code. The former selects two consecutive tap voltages of the resistor ladder, whose voltage difference is then subdivided by a string of 32 MOSFETs operating in the triode region. The fine code subsequently selects one of the subdivided values, generating the proper V_{out}. A key property of the above DAC topology is its guaranteed monotonicity for arbitrarily high resolutions, a critical aspect for use in feedback systems.

The receiver along with the LMS calibration uses a digital 0.25μm CMOS technology. The circuit has been tested with a 2.5V supply and achieves 5.2dB measured noise figure, 41dB voltage gain, −17dBm input IP3, and −33dBm blocking level. The linearity of the receiver is limited by that of the second downconversion mixers.

Large mismatches in the setup limit the image-rejection ratio to 25dB before calibration. After calibration, the image rejection is measured by applying a desired tone and an image tone of equal power and measuring the difference between their amplitudes as they appear in the baseband. As shown in Figure 18.6.5, the SS-LMS calibration improves the IRR from 25dB to 57dB. The IRR is also measured across the WCDMA frequency range by maintaining a constant baseband frequency. Figure 18.6.6 plots the IRR, indicating only 1dB of degradation as the input frequency deviates from the calibration point. The circuit consumes 55mW during calibration mode and 50mW during normal reception. Figure 18.6.7 shows a micrograph of the1.23x1.84 mm² die.

Acknowledgment:
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References:
[1] F. Behbahani, et al., "An Adaptive 2.4GHz Low-IF Receiver in 0.6μm CMOS for Wideband Wireless LAN," ISSCC Digest of Technical Papers, pp. 146-147, Feb. 2000.
[2] R. Montemayor and B. Razavi, "A Self-Calibrating 900MHz CMOS Image-Reject Receiver," Proc. of ESSCIRC, pp. 292-295, 2000.
[3] A. Zolfaghari, A. Chan, B. Razavi, "A 2.4GHz 34mW CMOS Receiver for Frequency-Hopping and Direct-Sequence Applications," ISSCC Digest of Technical Papers, Feb. 2001.
[4] A. Zolfaghari, A. Chan, B. Razavi, "Stacked Inductors and 1-to-2 Transformers in CMOS Technology," Proc. of CICC, 2000.

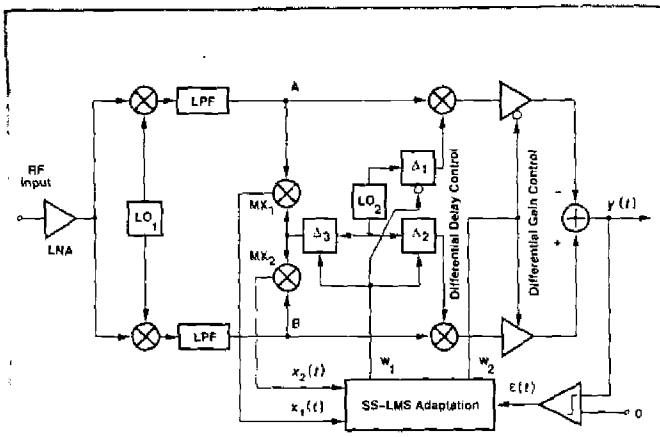

Figure 18.6.1: Receiver architecture.

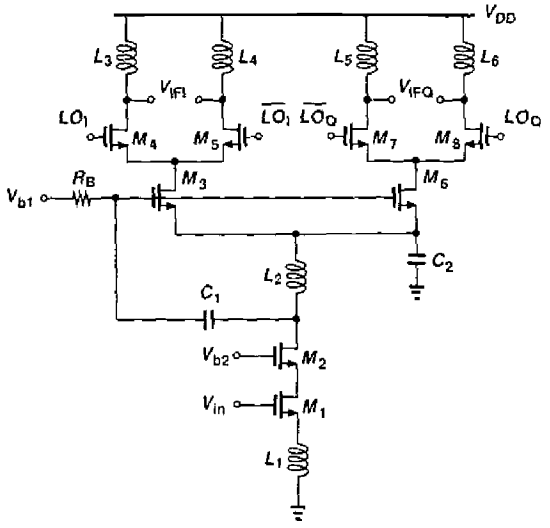

Figure 18.6.2: LNA and RF Mixers.

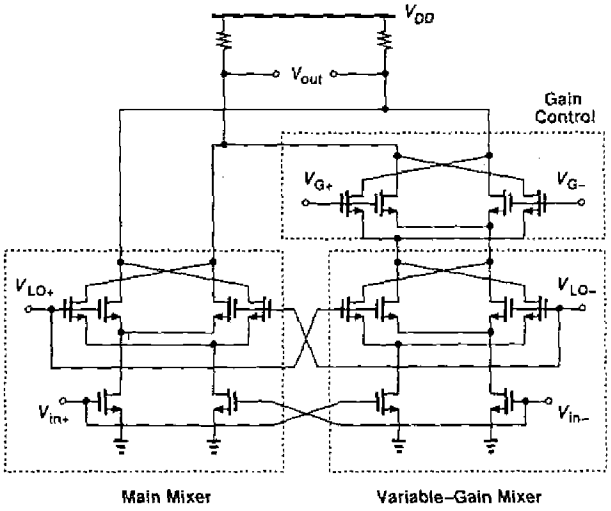

Figure 18.6.3: Simplified Circuit of second mixer.

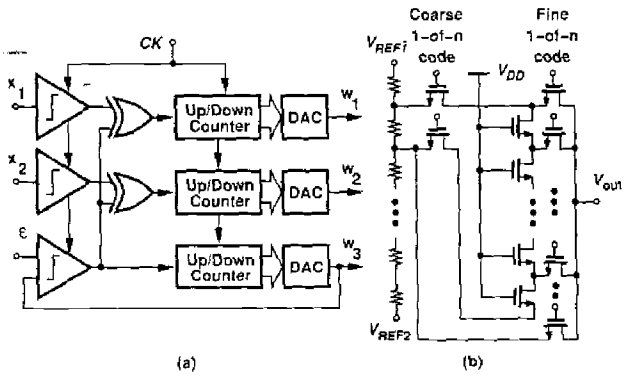

Figure 18.6.4: (a) SS-LMS adaptation circuit, (b) 1 slice of DAC.

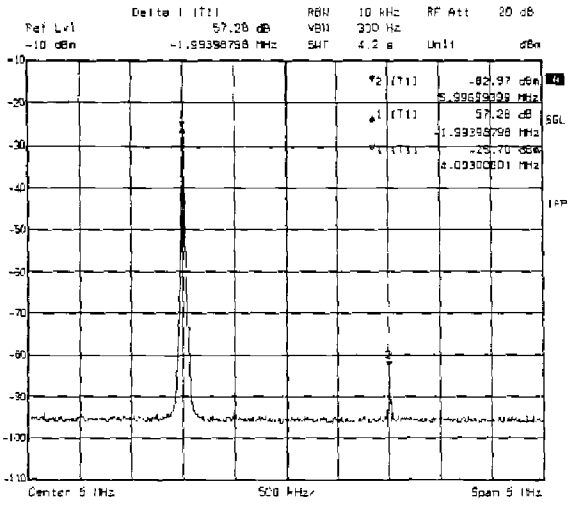

Figure 18.6.5: Output spectrum with desired tone at 4 MHz and image at 6 MHz.

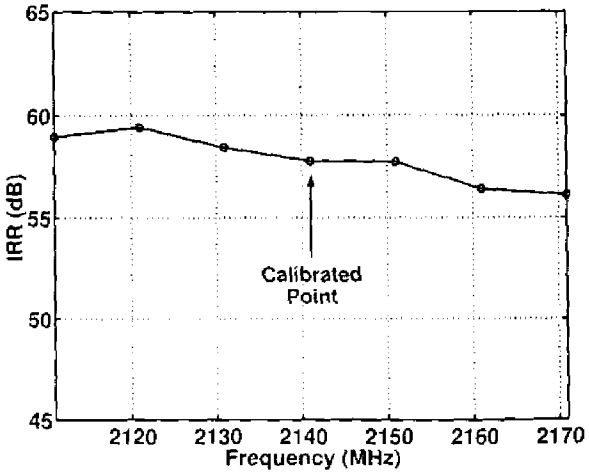

Figure 18.6.6: Measured IRR vs. Input frequency.

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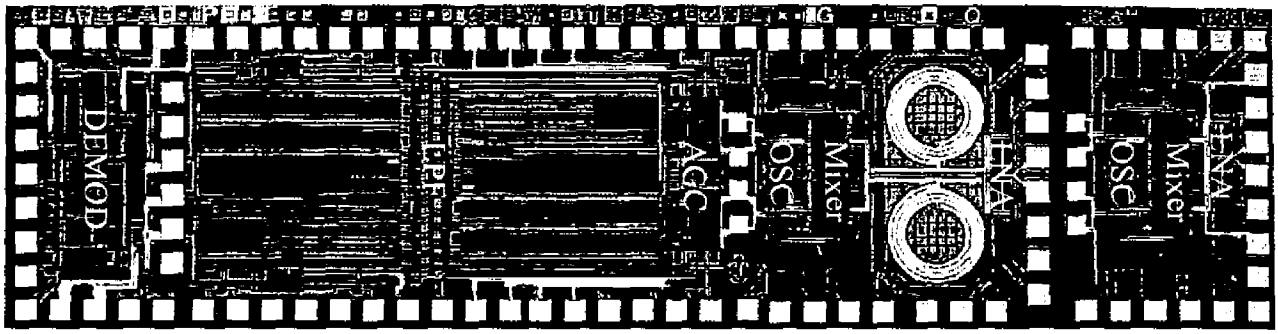

Figure 18.4.7: 4-FSK receiver die micrograph.

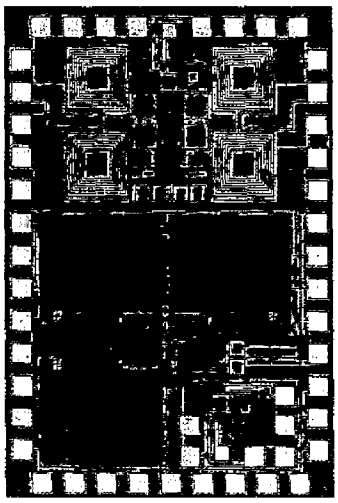

Figure 18.6.7: Die micrograph.

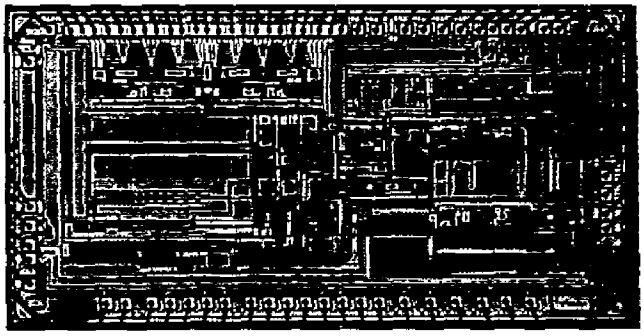

Figure 19.1.7: Analog front end micograph.

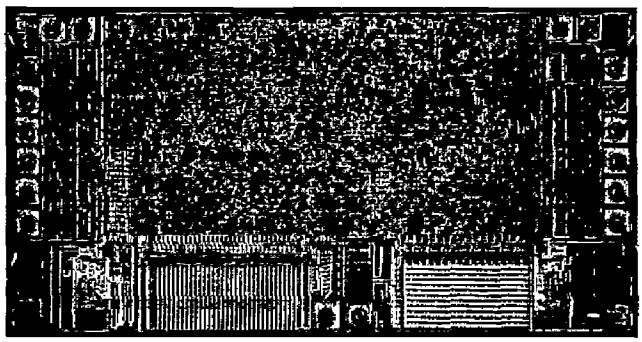

Figure 19.2.7: System-side chip micrograph.

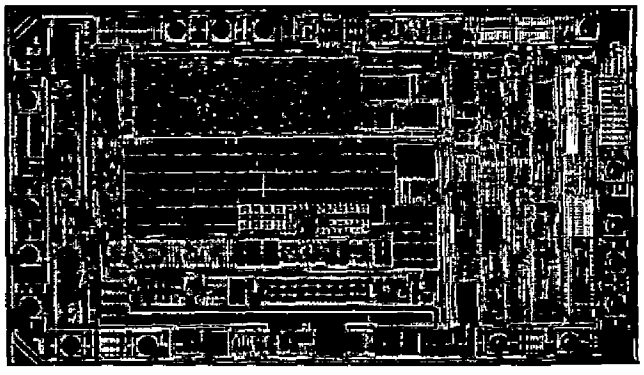

Figure 19.2.8: Isolated-side chip micrograph.

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