## 10.5 Broadband ESD Protection Circuits in CMOS Technology

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As device dimensions scale down and the operating speed of integrated circuits scales up, electrostatic discharge (ESD) proves an increasingly more critical issue. With hundreds of gigahertz I/O pads in typical data communication circuits, microprocessors, and memories, both the voltage tolerance and the area of ESD protection devices become important design parameters. It is possible to use inductive peaking to improve the bandwidth, but, with an ESD capacitance of 1.2pF, the impedance mismatch at the input or output results in $S_{11}$ or $S_{22}$ of only -4dB at 5GHz, corrupting broadband data considerably. Also, distributed ESD structures [1] suffer from the loss-capacitance trade-off of on-chip transmission lines and require a large area. For example, a metal6-metal1 microstrip designed to absorb an ESD capacitance of 1.2pF must be 8mm long and 14μm wide while introducing 1.5dB of midband loss. The distribution of the ESD capacitance over a resistive line may also compromise the voltage tolerance because an ESD event injects a large current into the line, creating a potential gradient from one end to the other.

The use of T-coil networks in ESD circuits can overcome the above difficulties. Shown in Fig. 10.5.1, such a network consists of inductors $L_1$ and $L_2$ with a coupling factor of $k$ [2] and a bridge capacitor $C_B$. An important attribute of this network that has not been exploited is that proper choice of the T-coil parameters can yield $Z_{in} = R_T$ *independent* of $C_L$ and the frequency. At low frequencies, $L_1$ and $L_2$ short $R_T$ to the input, and at high frequencies, $L_1$ and $L_2$ are open and the bridge capacitor $C_B$ plays the same role. For $Z_{in}$ to remain constant and equal to $R_T$ with frequency, the equations in Fig. 10.5.1 must hold. Moreover, for a well-behaved transfer function (uniform group delay), $\zeta = \sqrt{3}/2$, reducing these expressions to: $L_1 = L_2 = C_L R_T^2/3$, $C_B = C_L/12$, $k = 1/2$.

In addition to a constant input resistance, T-coils also increase the transfer bandwidth to a much greater extent than inductive peaking does [2]. In the ideal case, the bandwidth improvement factor reaches 2.72 for T-coils with $k = 1/2$ and only 1.6 for inductive peaking having the same type of response. These observations suggest that capacitor $C_L$ in Fig. 10.5.1 can be replaced by a standard ESD structure. The principal challenge therefore lies in the design of the T-coil itself for low loss and proper mutual coupling.

The fortunate coincidence $L_1 = L_2$ points to the use of a symmetric spiral realization of the T-coil, Fig. 10.5.2a, with the center tap representing the output terminal. The total inductance between nodes $A$ and $B$ is equal to $2L(k+1) = 3L = C_L R_T^2$. ASITIC simulations indicate that the coupling coefficient between the two halves in Fig. 10.5.2a is a strong function of the line spacing. Thus, with an initial guess for the number of turns and the outer dimension, the line width is chosen to minimize the loss, and the line spacing to obtain $k$=1/2. Next, the outer dimension is adjusted to achieve $L_{AB}=C_L R_T^2$.

If used in broadband circuits, T-coils must be modeled such that their response remains accurate for approximately the last decade of the band of interest. Figure 10.5.2b shows the distributed model used here. The spiral is decomposed into eight sections, and each section is represented by an inductance, series and parallel resistances, and parasitic capacitance to the substrate. The fringe capacitance between adjacent turns is also included. Since this capacitance appears between nodes $A$ and $B$ in a distributed form, the bridge capacitance, $C_B$, is chosen equal to the required value minus the total interwinding capacitance.

Another attribute of T-coils proves particularly important in input ESD design. To the first order, the series resistance of $L_1$ and $L_2$ does not affect the midband gain. It is readily seen in Fig. 10.5.1 that equal resistors placed in series with $L_1$ and $L_2$ leave $V_X$ unchanged if the circuit is driven by a source impedance equal to $R_T$. This is in sharp contrast to the behavior of ESD structures distributed over transmission lines, where the low-frequency metal resistance forms a voltage divider with the termination resistor.

The utility of T-coils is limited to low-impedance interfaces. Since $L_1$ and $L_2$ are proportional to $R_T^2$, large inductance values may be necessary if $R_T$ reaches several hundred ohms. For I/O interfaces, on the other hand, $L_{AB}$ falls in the range of a few nanohenries, lending itself to a compact symmetric implementation.

Figure 10.5.3 illustrates the overall input protection circuit. Devices $M_3$-$M_6$ and $M_7$-$M_{10}$ are standard ESD structures provided by the foundry. Driving 75Ω on-chip and 50Ω off-chip loads, differential pair $M_1$-$M_2$ represents a typical input stage and allows measurement of the broadband performance. Each T-coil occupies an area of 85μmx85μm, a factor of 15 lower than that in the distributed ESD example.

For output protection, the two ports of the T-coil are swapped, with the output current injected into the center tap. Figure 10.5.4 shows the resulting circuit. The dynamics are identical to those of the input structure. This topology, too, is free from midband loss.

The input and output protection circuits shown in Figs. 10.5.3 and 10.5.4 are fabricated in 0.18μm CMOS technology. The die photograph of both circuits is shown in Fig. 10.5.5. The ESD tolerance is tested according to the *JEDEC* standards, *JESD22-A114-B* for the human body model (HBM) [3] and *JESD22-A115A* for the machine model (MM) [4]. The zapping voltage is varied from 200V to 2000V in steps of 200V for HBM and from 50V to 200V in steps of 50V for MM. The measured HBM tolerance is 1000V for the input structure and 800V for the output structure. For MM, both circuits exhibit a tolerance of 100V.

The ESD circuits have also been tested for high-frequency characteristics. Figure 10.5.6 plots $S_{11}$ and $S_{22}$ for the input and output topologies, respectively, as a function of frequency. The measured $S_{11}$ remains below -24dB and $S_{22}$ below -20dB for frequencies as high as 10GHz. These quantities fall below -30dB at a few gigahertz, suggesting that the low-frequency resistance of the symmetric inductor does not degrade the matching significantly. Figure 10.5.7 shows the measured eye diagrams for both structures with an input pattern of $2^{23}$-1 at 10Gb/s.

*References*

[1] B. Kleveland, et al., "Distributed ESD Protection for High-Speed Integrated Circuits," *IEEE Electron Device Letters*, vol. 21, pp. 390-392, Aug. 2000.

[2] Dennis L. Feucht, Handbook of Analog Circuit Design, San Diego: Academic Press, 1990.

[3] JEDEC Standard JESD22-A114-B, "Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model," *JEDEC*, 2000.

[4] EIA/JEDEC Standard Test Method A115-A, "Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)," *EIA/JEDEC*, 1997.

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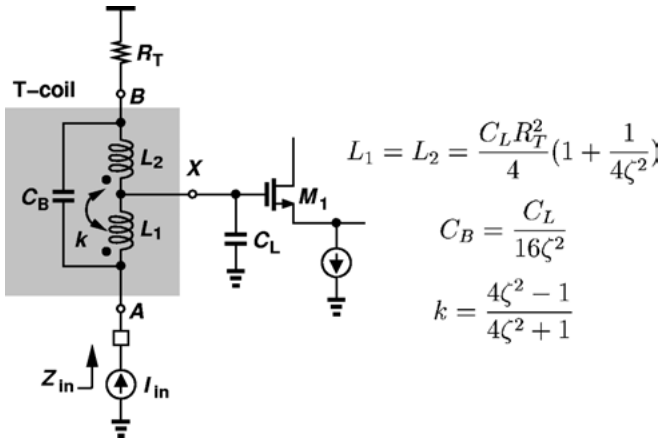


Figure 10.5.1: T-coil network.

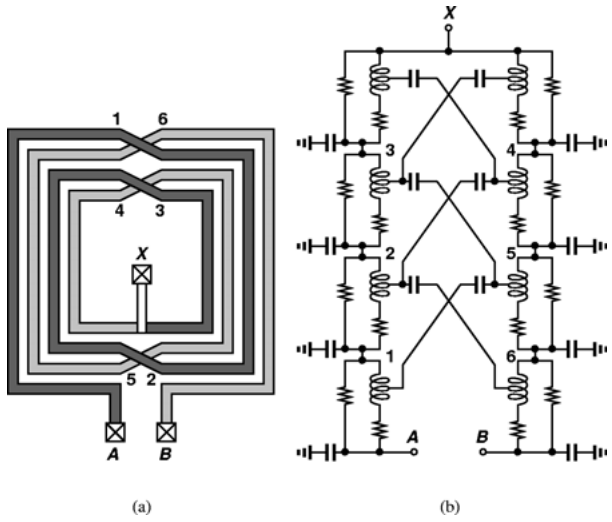


Figure 10.5.2: T-coil network (a) implementation, (b) distributed model.

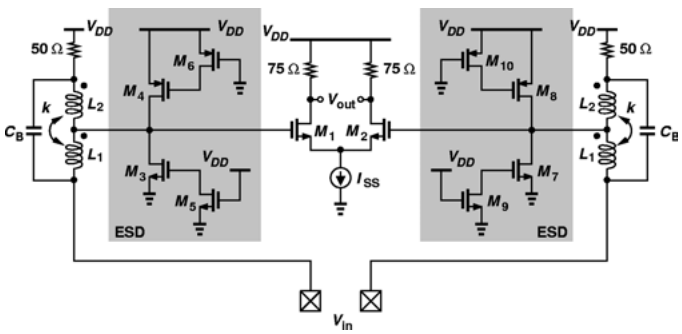


Figure 10.5.3: Input ESC protection circuit.

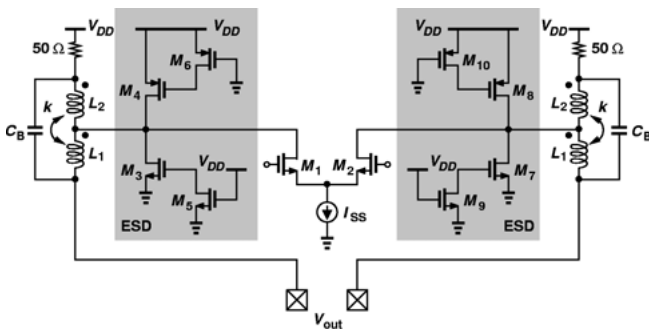


Figure 10.5.4: Output ESD protection circuit.

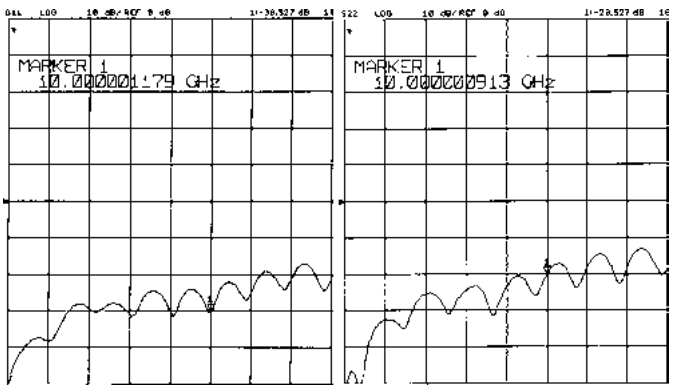


Figure 10.5.6: Measured return loss: (a) input ESD, (b) output ESD (Horizontal scale: -2GHz/div., vertical scale: 10dB/div.).

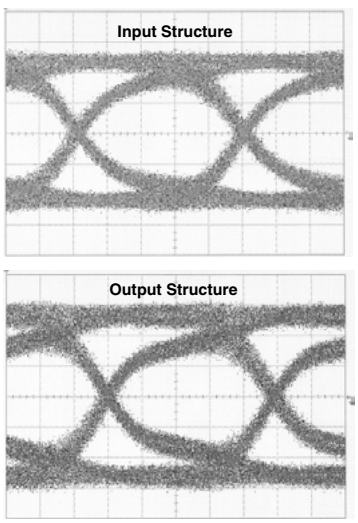


Figure 10.5.7: 10Gb/s eye diagrams for input and output ESD structures (Horizontal scale: 20ps/div., vertical scale: 50 mV/div.).

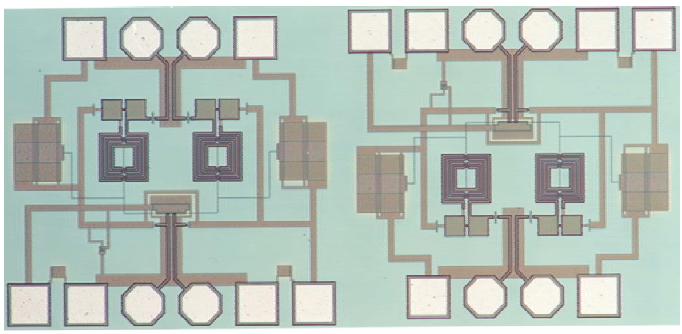

**Figure 10.5.5: die micrograph of ESD circuits.**




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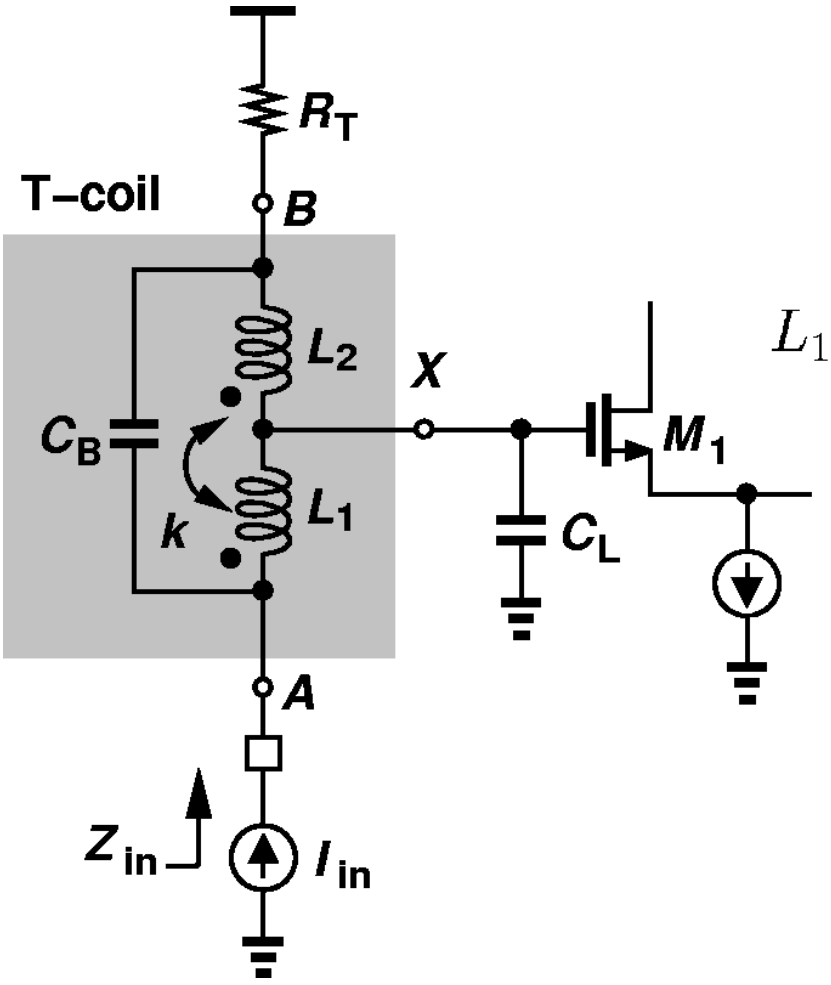


$$L_1 = L_2 = \frac{C_L R_T^2}{4}\left(1 + \frac{1}{4\zeta^2}\right)$$

$$C_B = \frac{C_L}{16\zeta^2}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1}$$

**Figure 10.5.1: T-coil network.**


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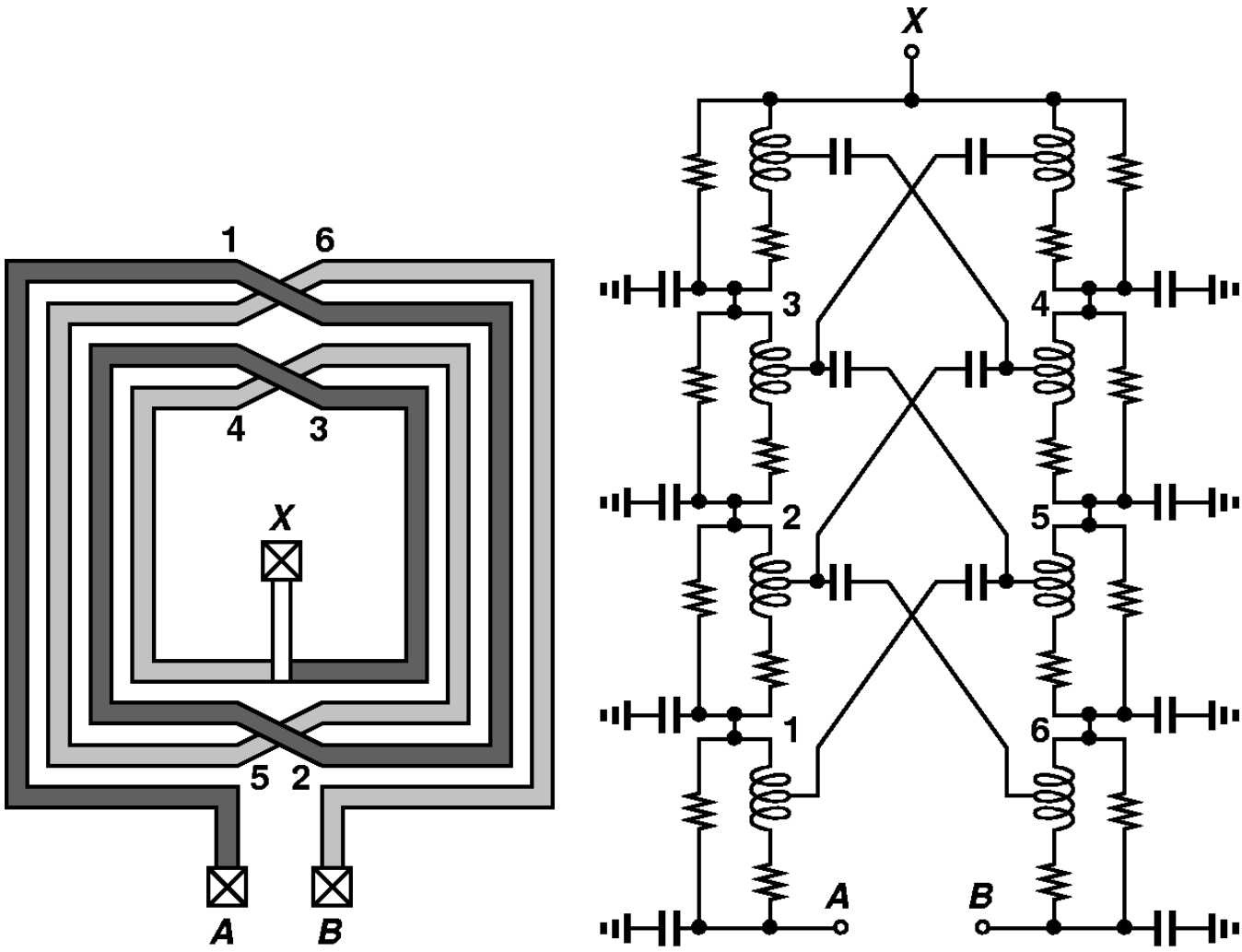


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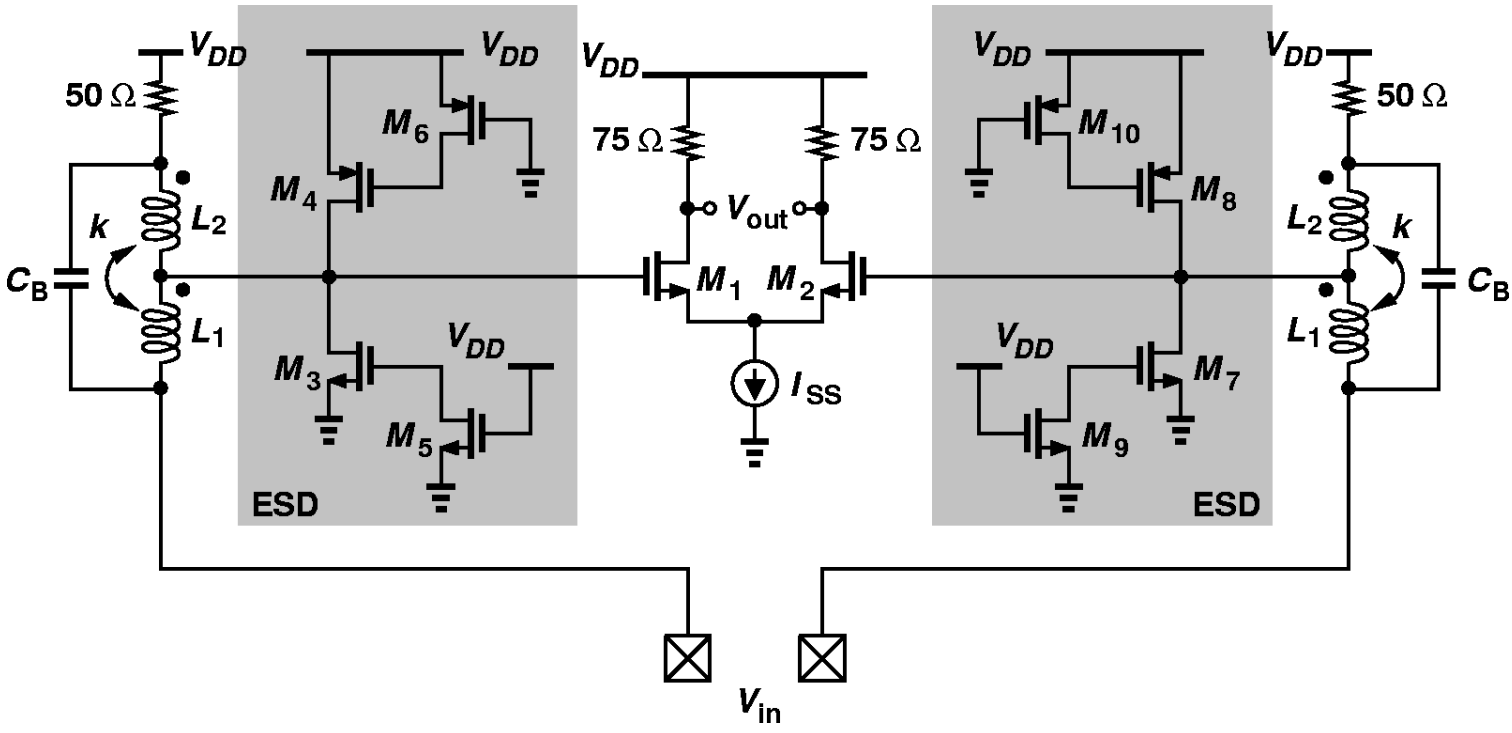



**Figure 10.5.3: Input ESC protection circuit.**

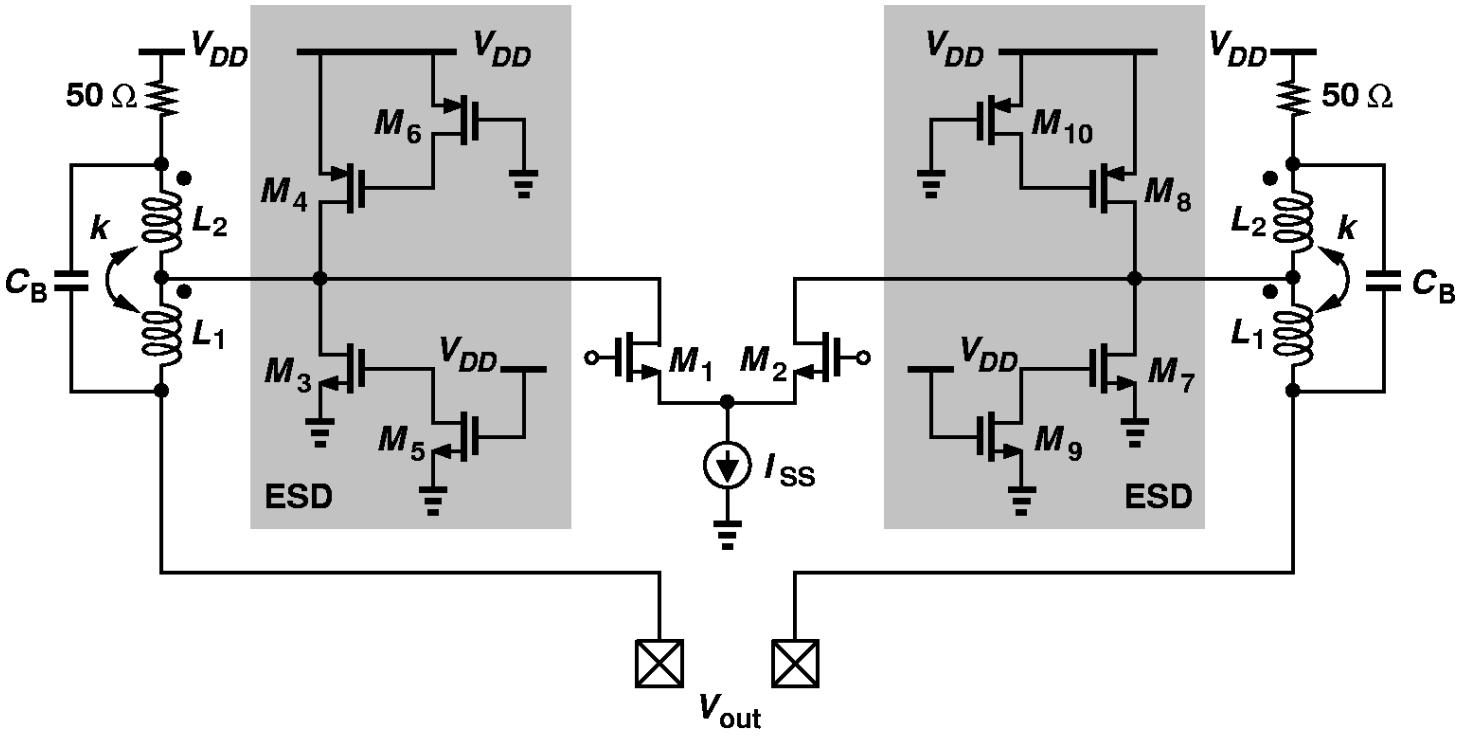
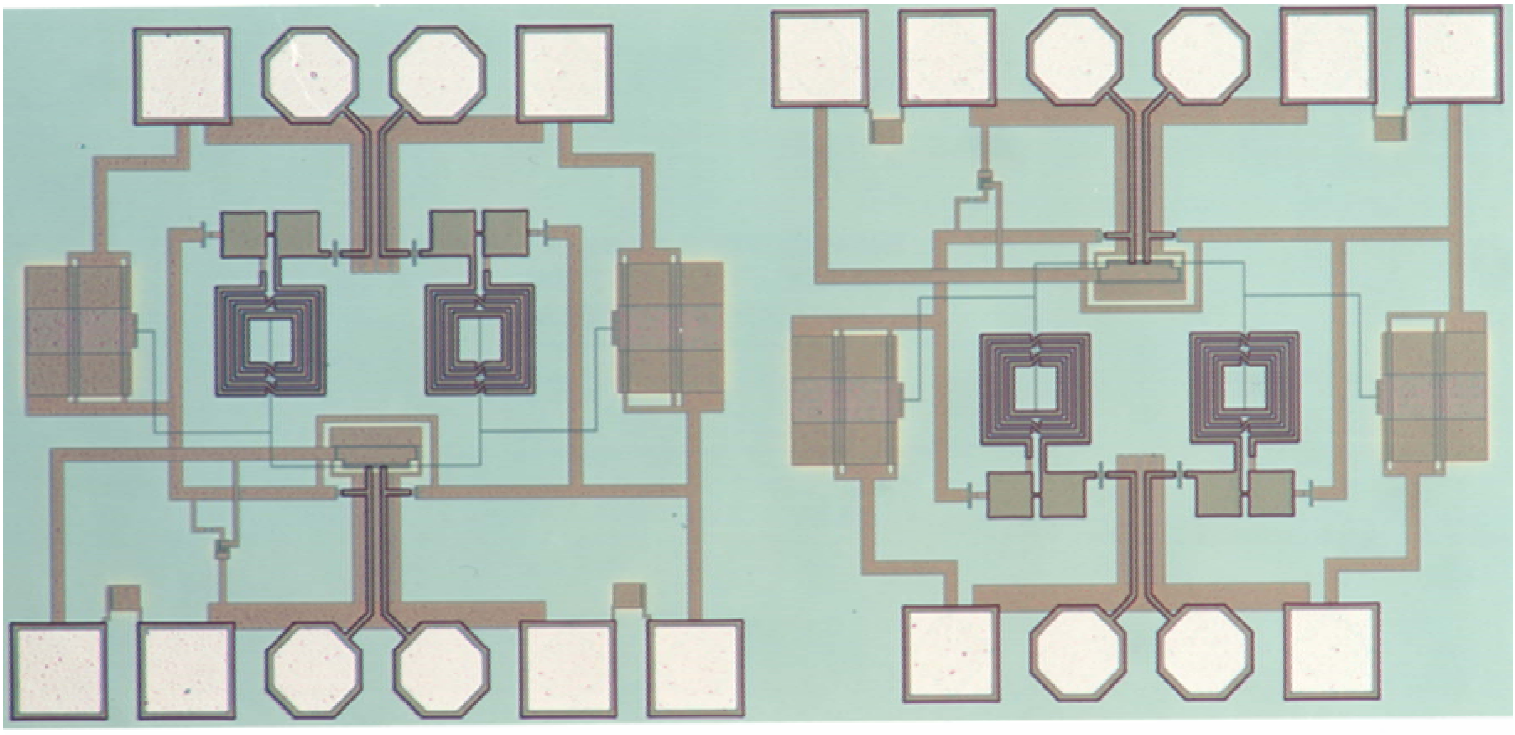



**Figure 10.5.4: Output ESD protection circuit.**



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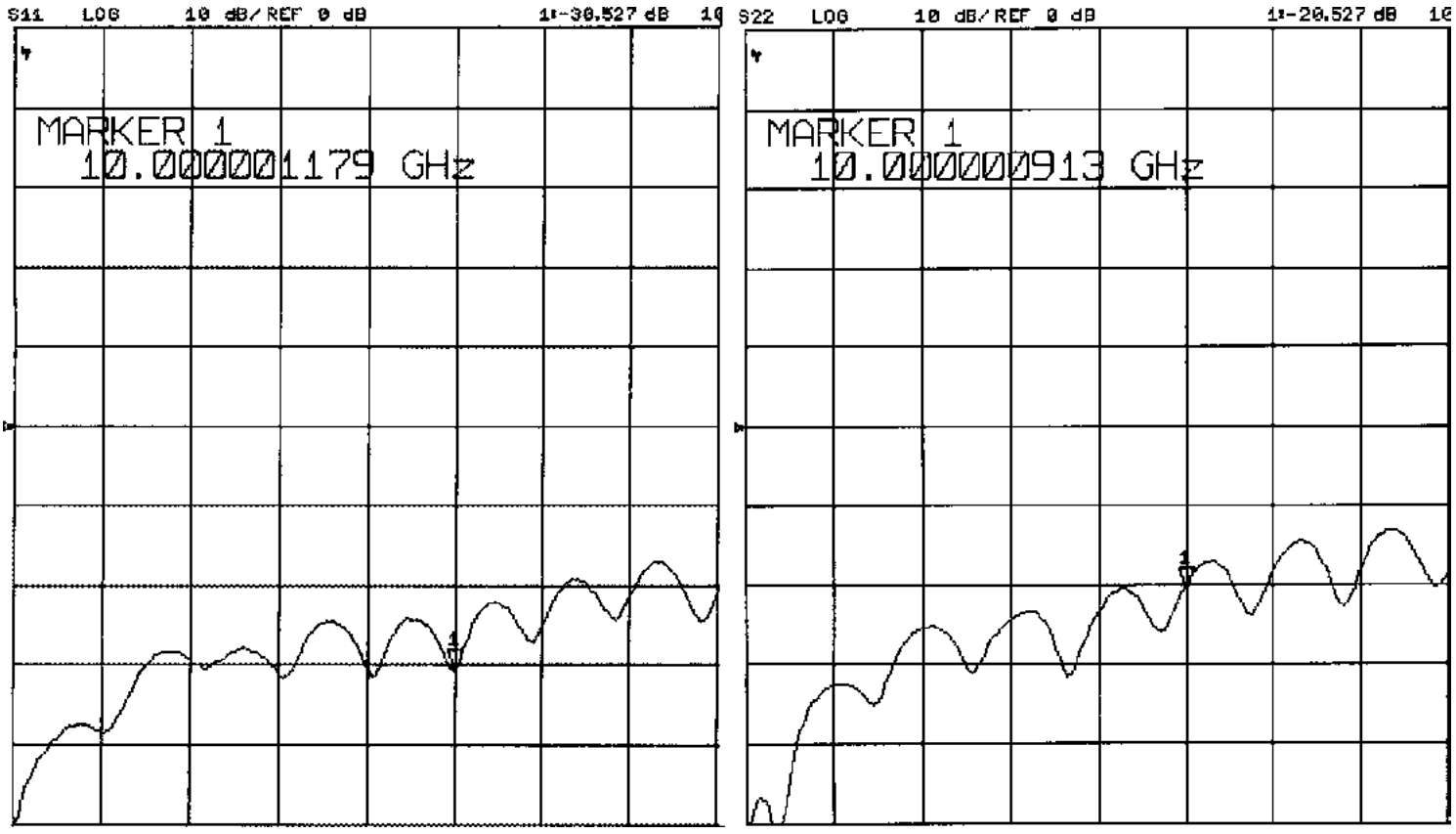


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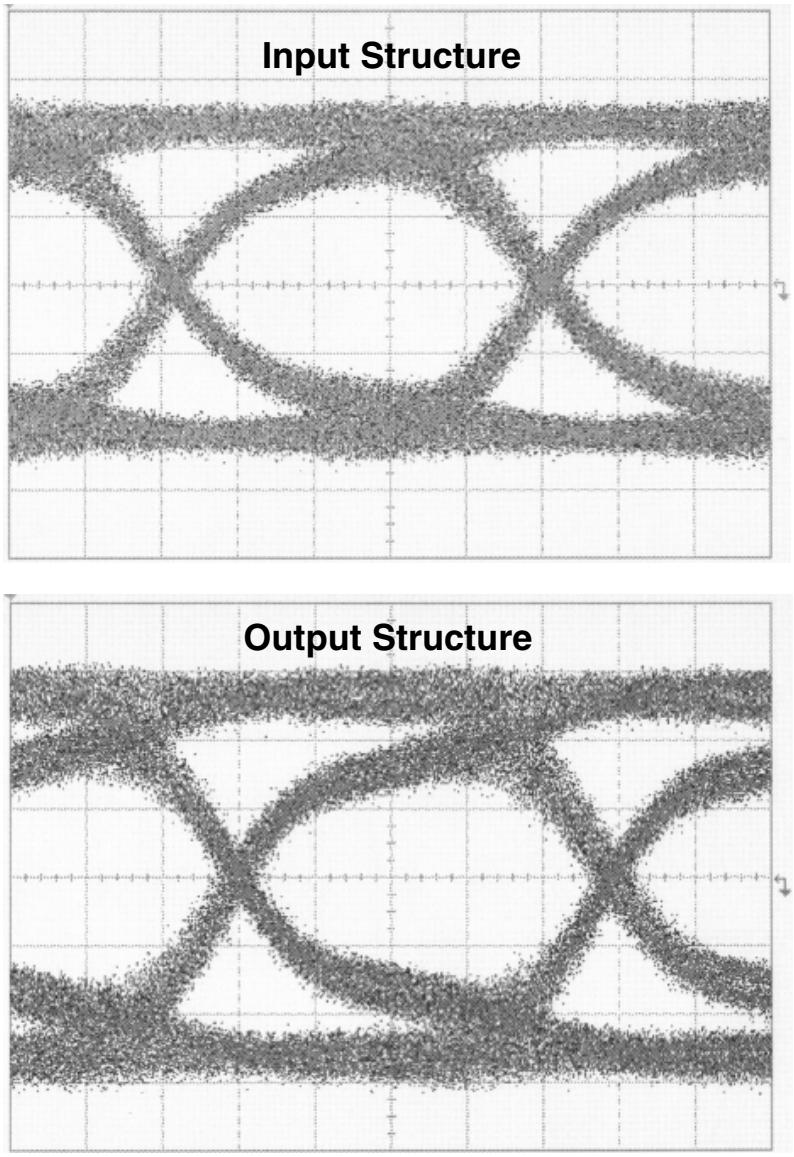


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