10.8 10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18μm CMOS Technology

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The trend towards full integration of broadband transceivers [1,2] makes it desirable to realize front-end circuits such as limiting amplifiers (LAs) and laser/modulator drivers (LMDs) in CMOS technology. These amplifiers and drivers may serve as stand-alone functions in optical modules or coexist with serializers and deserializers on the same chip.

The low transconductance of MOS devices, the limited voltage headroom, and the large voltage swings necessary for CMOS CDR circuits create a tight performance envelope that severely constrains the speed of CMOS LAs. Furthermore, unlike their bipolar counterparts, the first few gain stages in a CMOS LA operate linearly, exhibiting a small-signal behavior and hence a smaller bandwidth. Figure 10.8.1 shows the LA architecture. The core consists of five identical stages each having a voltage gain of 10dB and a bandwidth of 16GHz. While inverse scaling eases the design [3], it is avoided here to allow 50Ω driving capability. The core is followed by a buffer that delivers 1-V_{pp} differential output swings to a 75Ω on-chip and a 50Ω off-chip termination resistor. An on-chip low-pass filter and a feedback amplifier remove the dc offset of the chain and provide a low-end corner frequency of 25kHz.

To achieve the required bandwidth, each gain stage incorporates three high-speed techniques: negative Miller capacitance, inductive peaking, and active negative feedback [Fig. 10.8.2]. Commonly used in broadband design, the first two increase the bandwidth to only 4 GHz, and it is the third that enables 10-Gb/s operation. In conventional resistive feedback techniques, e.g., the Cherry-Hooper amplifier [4], the strength of the feedback (i.e., the value of the feedback resistor) directly trades with the open-loop gain. Alternatively, the unilateral feedback in an active stage avoids this trade-off. In Fig. 10.8.2, the differential pair M_5-M_6 provides active feedback. It can be proved that active feedback results in a gain-bandwidth product of roughly f_T^2/BW. With $f_T \approx 45$GHz for 0.18μm NFETs and $BW \approx 16$GHz, each stage yields a maximum gain of 18dB.

Transistors M_7 and M_8 in Fig. 10.8.2 introduce a negative capacitance at the input, lowering the load on the preceding stage. With a gate-source voltage near zero, these devices are realized as accumulation-mode MOS varactors to obtain a larger fraction of the gate oxide capacitance and better tracking. The buffer in Fig. 10.8.1 must incorporate wide transistors, potentially presenting a large load capacitance to the core. This buffer is configured as an f_T doubler along with inductive peaking [5] to provide a large output current while exhibiting a moderate input capacitance.

Depending on the application, a driver may deliver a current of 100mA to a 25Ω laser (direct modulation) or 2V_{pp} across a 50Ω Mach-Zehnder modulator (external modulation). The output swing required of both drivers is therefore around 2Vp-p. The very large currents that must be switched by the driver's output stage demand very wide transistors, making the design of the predriver stage difficult. Even with inductive peaking, the bandwidth of the driver falls below 5GHz.

The LMD circuit consists of three identical slices in parallel, each capable of delivering approximately 40mA to an external 50Ω load. For direct modulation, all three slices are enabled, providing more than 100mA to a 25Ω laser. For external modulation, only one slice is enabled. Simulations and measurements indicate that the input and output capacitances of the disabled slices do not degrade the speed in this mode.

This design introduces two techniques that substantially increase the bandwidth at the interface between the predriver and the output stage. Illustrated in Fig. 10.8.3, each slice employs T-coil peaking using on-chip coupled inductors. The driver also employs negative capacitance cancellation at nodes X and Y by the cross-coupled pair M_5-M_6 and compensation capacitors M_7-M_8 implemented using accumulation-mode MOS varactors. This pair presents a negative resistance, but the low values of R_L and the T-coil inductors prohibit underdamped response. The differential pair M_1-M_2 is designed to amplify a 400mV_{pp} single-ended input swing to the level necessary for the output stage. Inductors L_S create series peaking at the drains of the M_1 and M_2, partially canceling the effect of their drain junction capacitances.

The LA and the LMD have been fabricated in 0.18μm CMOS technology and measured in chip-on-board assemblies. Figure 10.8.4 shows the die photographs. The small-signal single-ended frequency response (S_{21}) of the LA is plotted in Fig. 10.8.5a, revealing a -3dB bandwidth of 9.4GHz. The total differential gain is 50dB. Figure 10.8.5b shows the measured bit error rate (BER) as a function of the differential input for a 2^{23}-1 random sequence. Figure 10.8.6 depicts the single-ended eye diagrams for two input levels, indicating the circuit limits even for a 5mV_{pp} input signal.

Figure 10.8.7(a) shows the setup used to measure the laser driver. A bias T follows the LMD to establish a common-mode level of 1.8 V at the drains of the output transistors. Thus, for a peak-to-peak swing of 2.5 V, each drain voltage exceeds V_{DD} by 1.25 V while the corresponding gate voltage falls below V_{DD} by about 0.6 V. That is, the maximum drain-gate voltage is around 1.85 V. Two 35Ω resistors are added in parallel with the circuit's output and in series with the transmission line, creating an equivalent source impedance Z_1 of 50Ω. Presenting an equivalent load, Z_2, of 25Ω to the LMD, this network also attenuates the voltage swing delivered to the oscilloscope by a factor of 1.7. The measured output is shown in Fig. 10.8.7(b), indicating that the driver delivers a current of approximately 100mA.

References

[1] M. M. Green, et al., "OC-192 Transmitter in Standard 0.18μm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 248 -464, Feb. 2002.

[2] J. Cao, et al., "OC-192 Receiver in Standard 0.18μm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 250 -464, Feb. 2002.

[3] E. Sackinger, et al., "A 3GHz 32dB CMOS Limiting Amplifier for SONET OC-48 Receivers," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1884-1888, Dec. 2000.

[4] E. M. Cherry, D. E. Hooper, "The Design of Wide-Band Transistor Feedback Amplifier," *Inst. Elec. Eng. Proc.*, vol. 110, no. 2, pp. 375-389, Feb. 1963.

[5] B. Razavi, "Prospects of CMOS Technology for High-Speed Optical Communication Circuits," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1135-1145, Sept. 2002.

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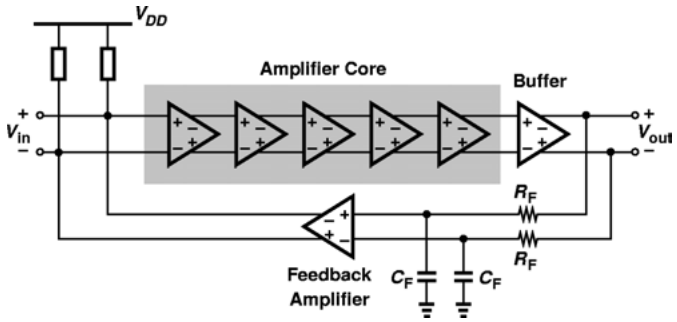


Figure 10.8.1: Limiting amplifier architecture.

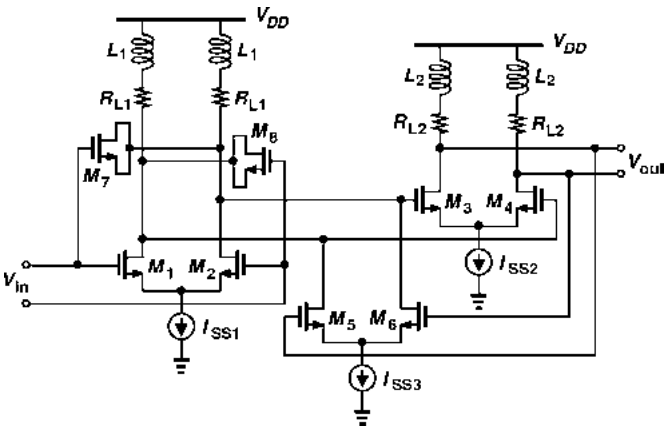


Figure 10.8.2: Gain cell used in LA core.

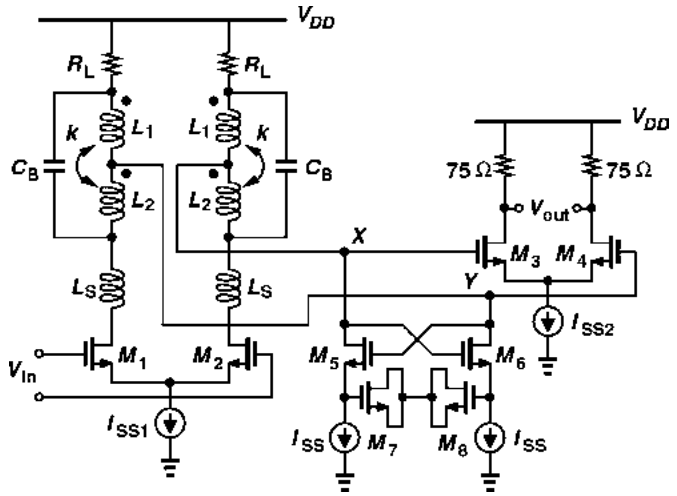


Figure 10.8.3: Circuit implementation of one slice of LMD.

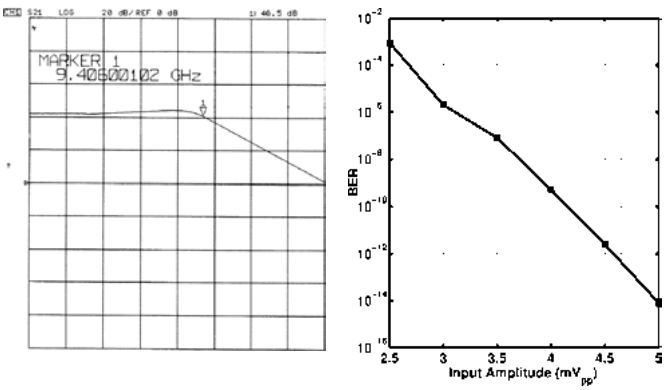


Figure 10.8.5: LA measured performance (a) S21 (Horizontal scale: ~ 2GHz/div. vertical scale: 20dB/div.), (b) BER.

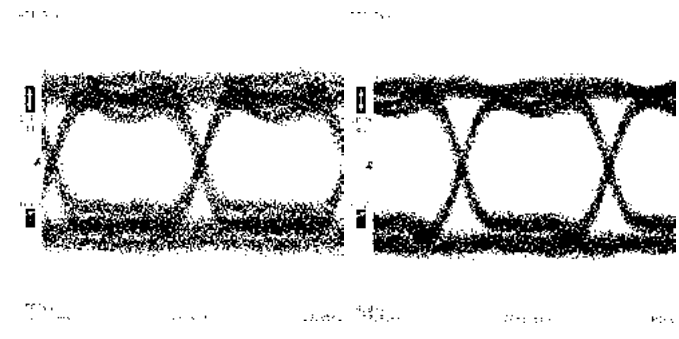


Figure 10.8.6: Measured LA output for input level of: (a) 5mVpp, (b) 20mVpp (Horizontal scale: 20ps/div., vertical scale: 100mV/div.).

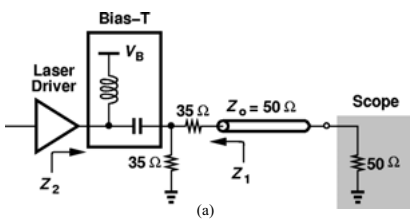
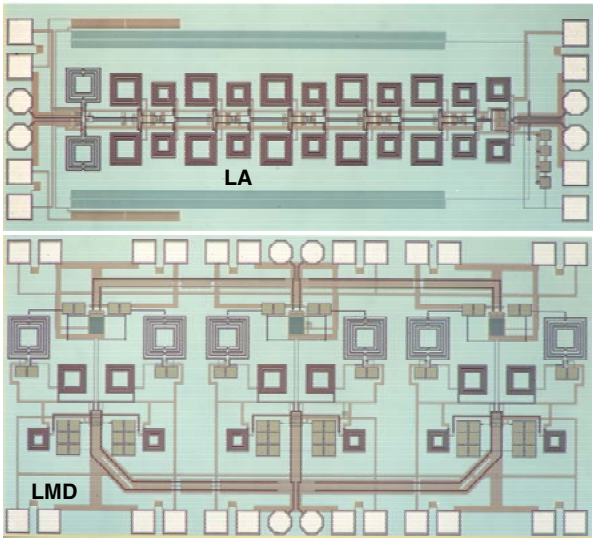


Figure 10.8.7: (a) Laser test setup, (b) measured laser driver output (Horizontal scale: 20ps/div., vertical scale: 200mV/div.).



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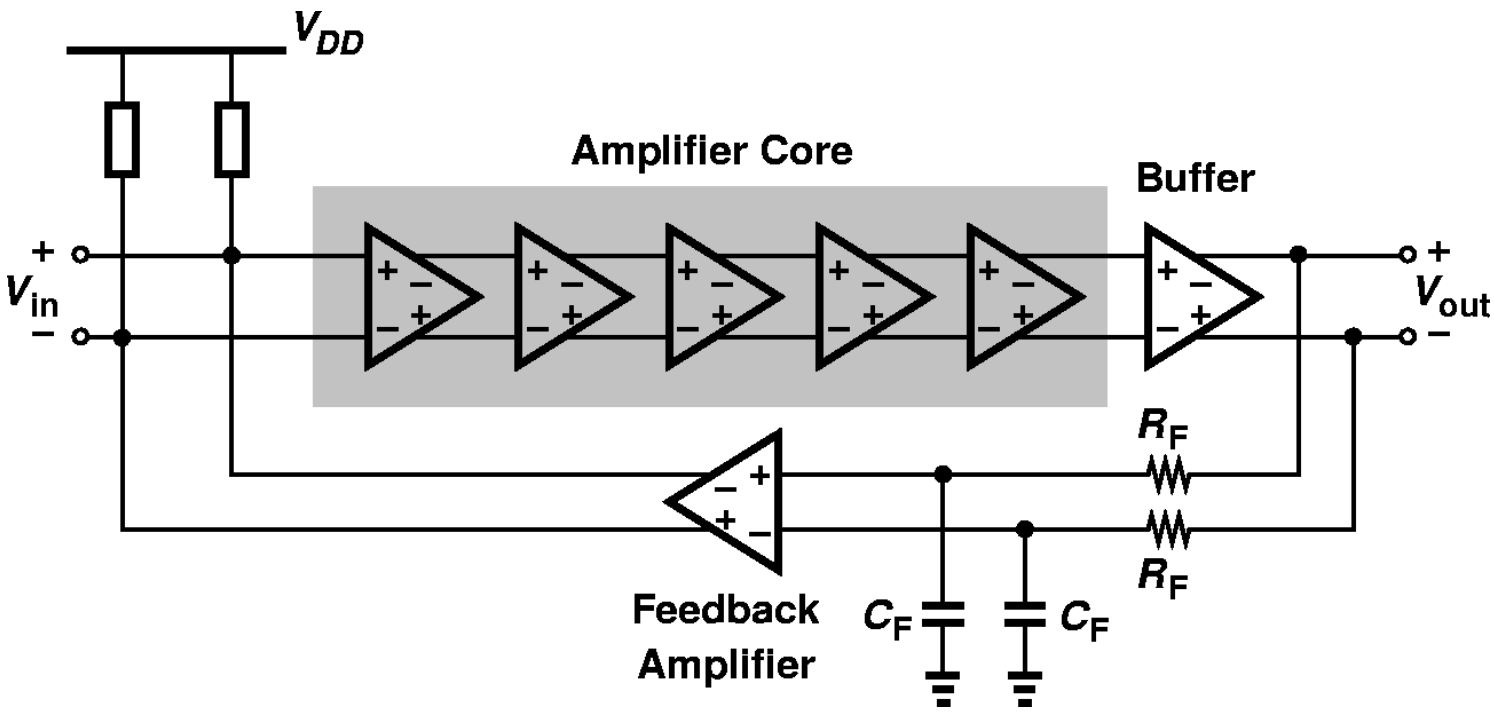

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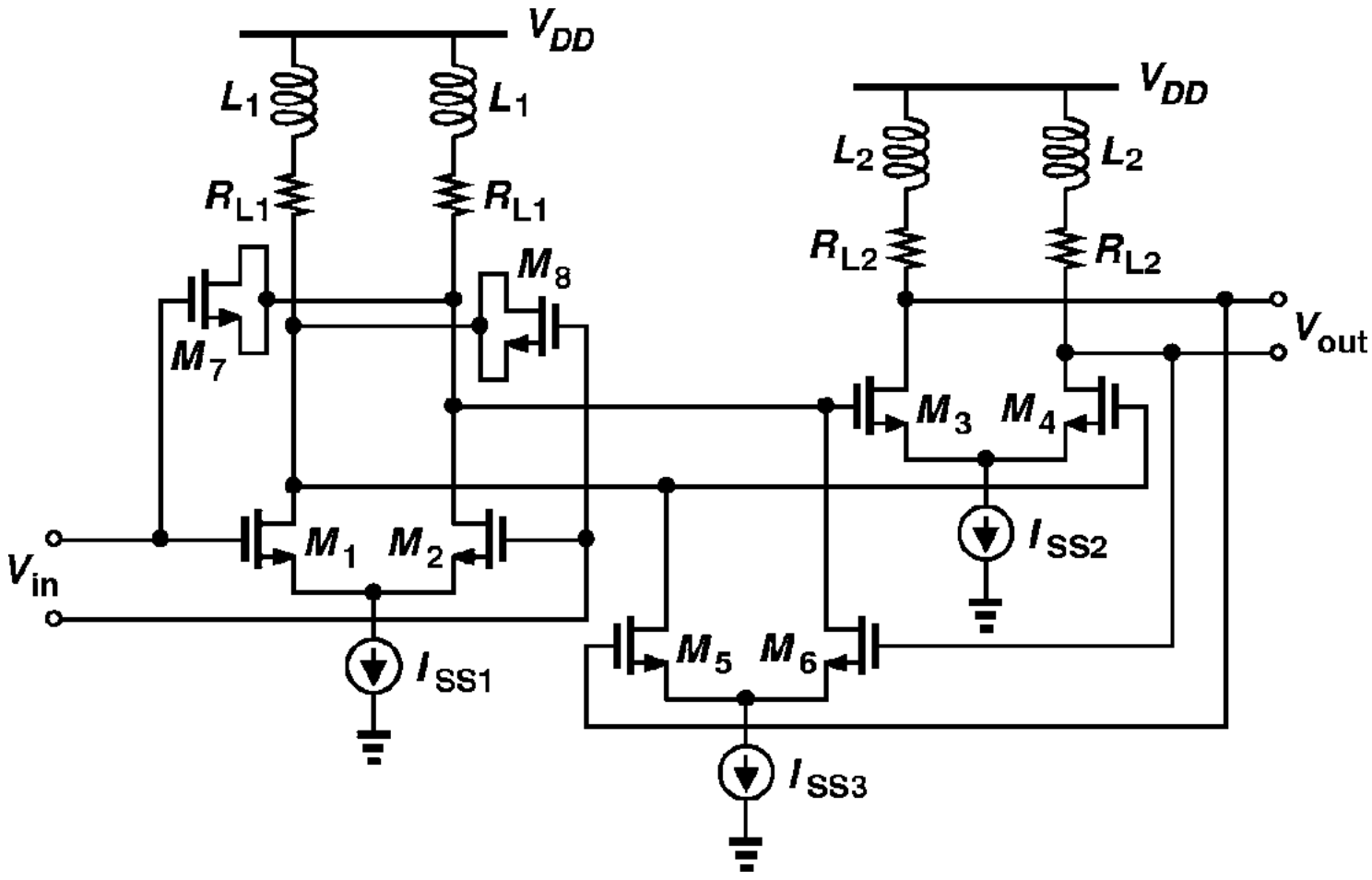

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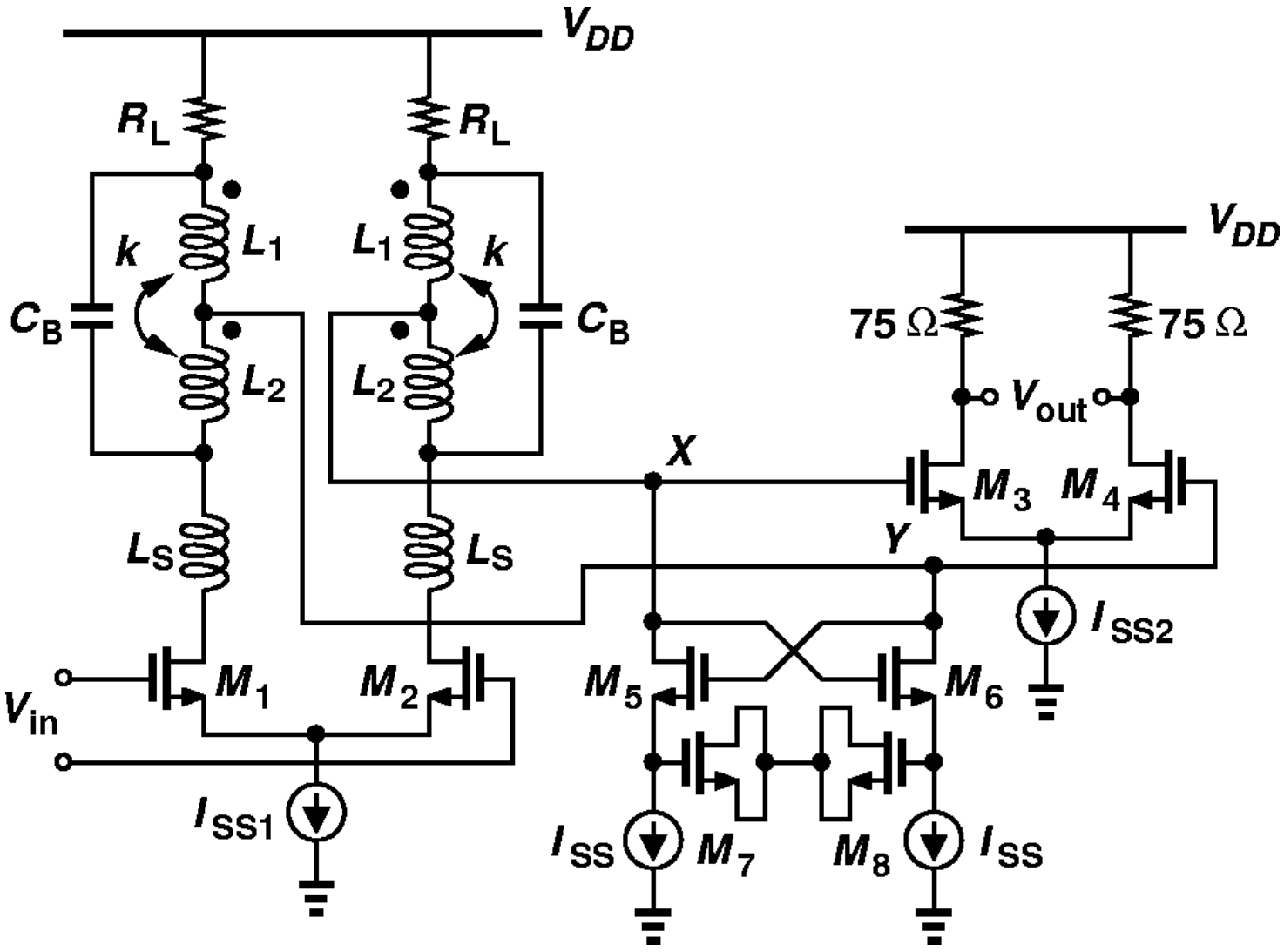

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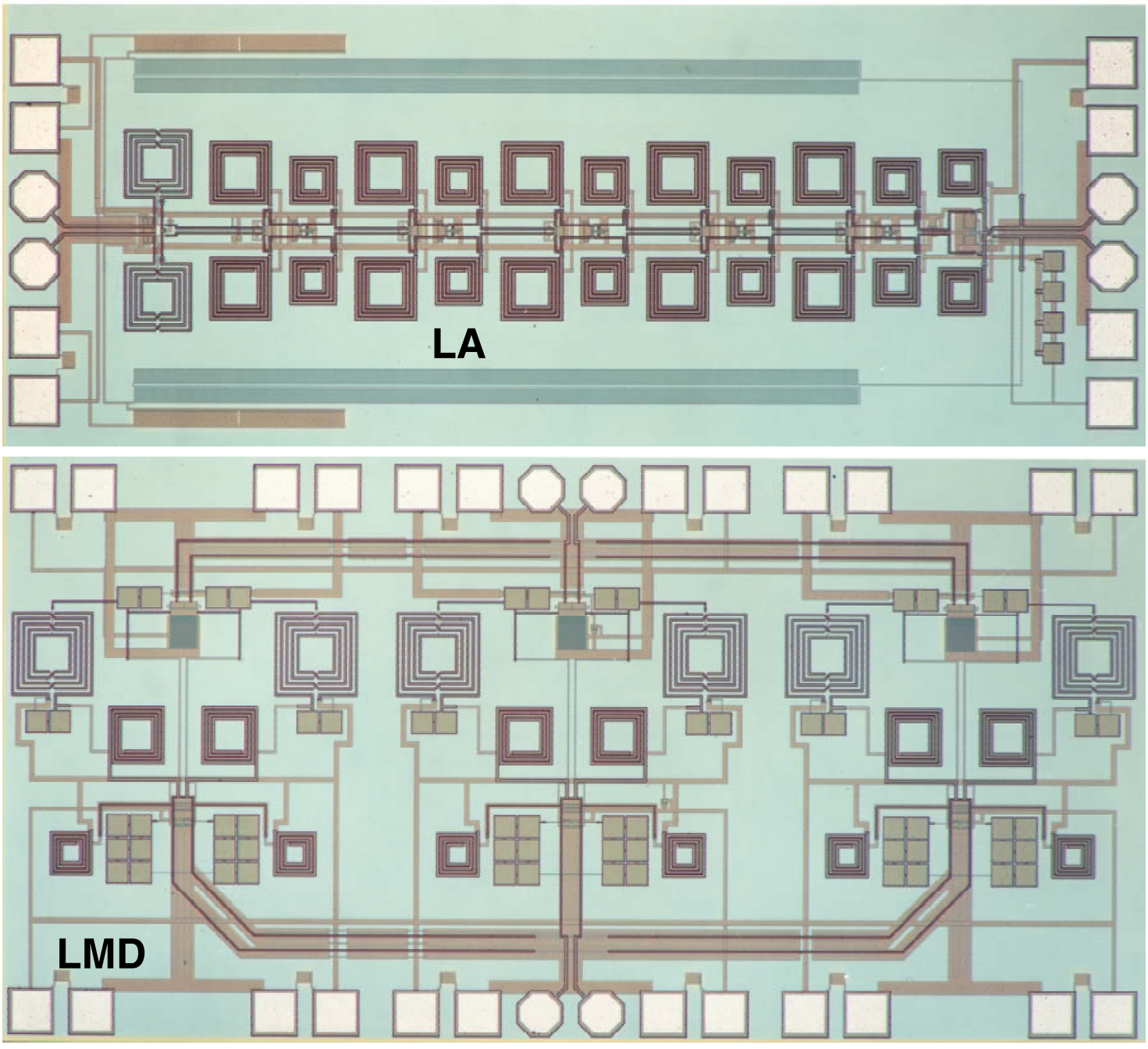

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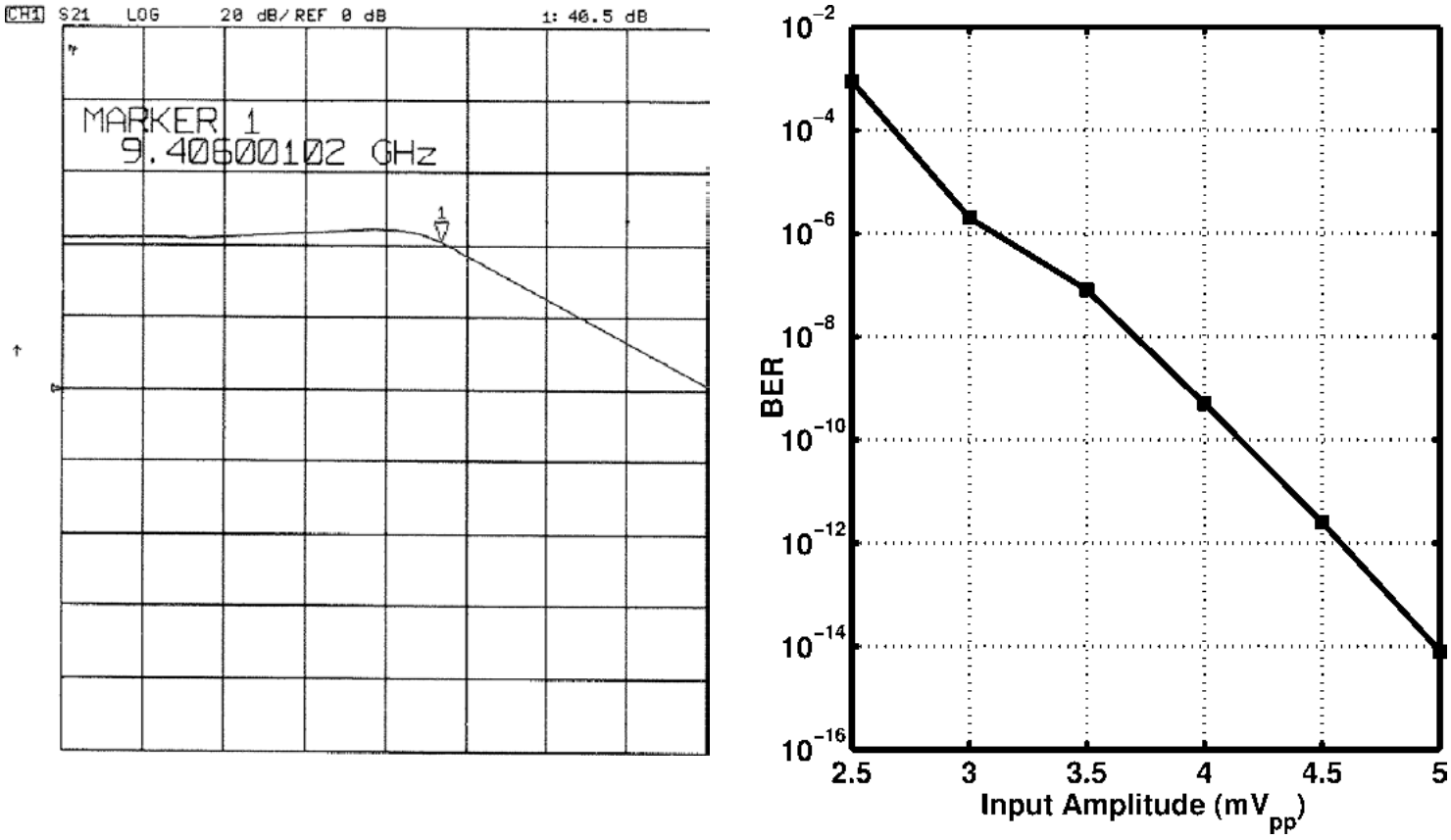

(a) (b)

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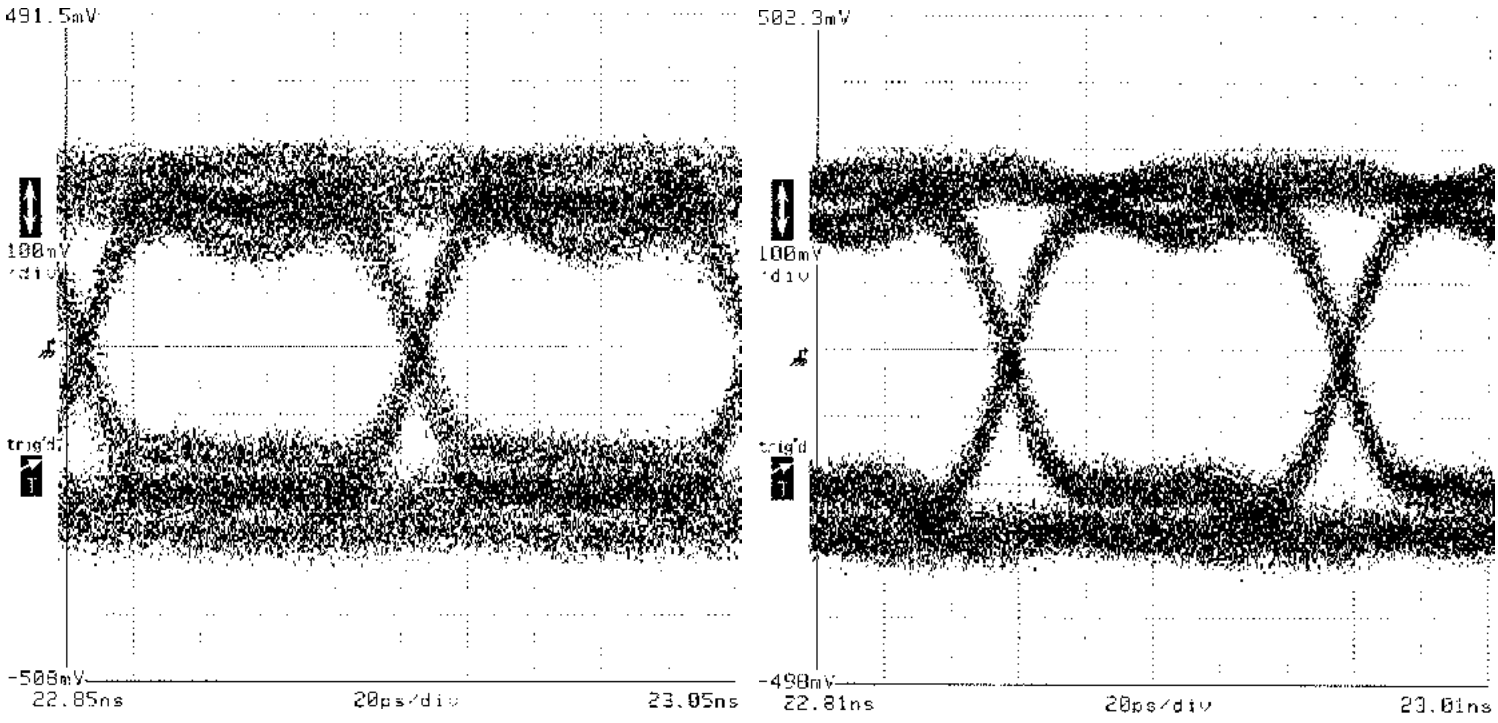

(a) (b)

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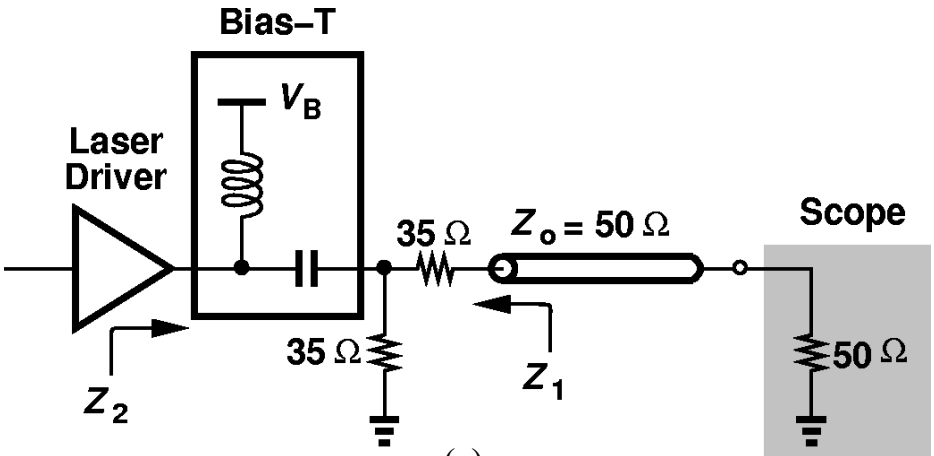

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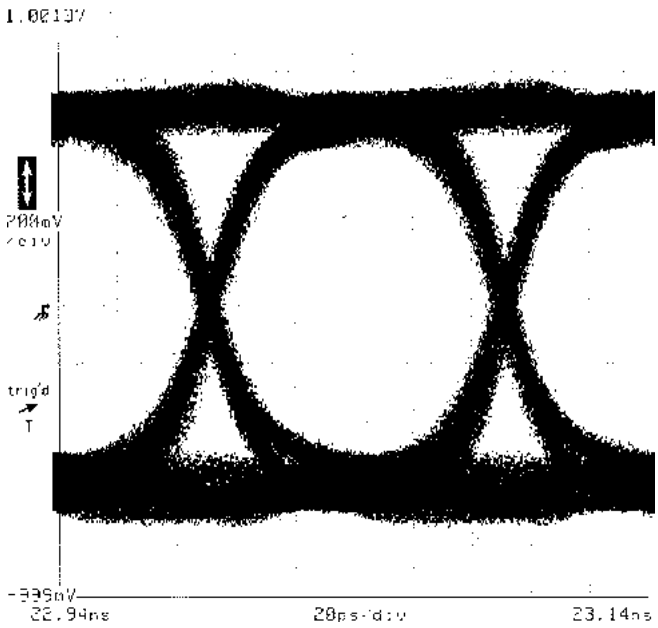

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