A 10-Gb/s CMOS Merged Adaptive Equalizer/CDR Circuit for Serial-Link Receivers[1]

Srikanth Gondi, Behzad Razavi

Electrical Engineering Department
University of California, Los Angeles

Abstract

A merged equalizer/CDR circuit employs a parallel-path equalizer and triple-loop adaptation to achieve a binary data rate of 10 Gb/s. Realized in 0.13-μm CMOS technology, the circuit adapts to FR4 trace lengths up to 24 inches with BER<10^{-13} while consuming 133 mW from a 1.6-V supply.

For data rates approaching 10 Gb/s, backplane transceivers may employ pre-emphasis in the transmitter and equalization in the receiver [1]. In [1], however, the transmitter output dynamic range requires a 2.5-V supply. It is therefore desirable to perform extensive equalization in the receiver to relax the design of the transmitter. Moreover, the equalization and clock and data recovery (CDR) functions can be merged so as to reduce the area and power dissipation. This paper describes an adaptive equalizer/CDR circuit that reproduces retimed data received on 24-in traces on FR4 boards.

Architecture. The architecture of the merged equalizer/CDR is shown in Fig. 1. Unlike stand-alone equalizers [2, 3], this design omits the explicit (multistage) slicer necessary after the equalization path and views the *retimed data* as the sliced signal. The difference between the high-frequency energies of D_{eq} and D_{out} is then extracted to control the amount of boost. Similarly, the difference between the low-frequency contents controls the swing of the sliced data information to accommodate errors due to swing uncertainties [2].

The architecture of Fig. 1 entails a start-up issue. With high intersymbol interference (e.g., for a 24-in trace), if the equalizer begins with minimum boost, then each data edge applied to the CDR spans several bit periods, thus prohibiting proper phase-lock. For this reason, the equalizer boost is set to maximum on power-up. Nonetheless, the architecture contains three feedback loops whose time constants must be chosen carefully to ensure convergence. In this design, the swing control loop is the fastest, and the boost control loop, the slowest.

Equalizer Path. Figure 2 depicts the adaptive equalizer block diagram. Three boost stages provide up to 18 dB of peaking at 5 GHz, and a weighted sum of the input and the output allows boost control. This technique maintains a constant output swing while providing a much wider tuning range than resistor or varactor tuning does. However, the large phase shift through the boosting stages distorts the linear summation of the equalized and the unequalized signals for intermediate trace lengths ($\alpha_1\alpha_2 \neq 0$). A phase shift network is therefore inserted in the all-pass path.

In order to provide significant peaking at high frequencies with low power dissipation, this work introduces a passive boost technique. Passive peaking can be realized by means of the simple RC topology shown in Fig. 3(a), where the pole and the zero (with negligible C_{in}) provide a boost factor of $1+R_1/R_2$. However, for a reasonable return loss, $|Z_{in}|$ must be much greater than 50 Ω at frequencies in the range of 5 to 10 GHz, requiring that R_1 and R_2 be relatively large (~300-1000 Ω). As a result, the transfer function is considerably altered by the input capacitance of the first active stage, C_{in}, leading to a lower boost. This difficulty is resolved by employing series peaking as shown in Fig. 3(b). Here, L_1 provides additional peaking at frequencies above 5 GHz, while the input return loss remains better than 10 dB up to 10 GHz. Using an on-chip spiral inductor, the passive network of Fig. 3(b) exhibits a peaking of 9 dB and a low-frequency loss of 8 dB. Figure 3(b) also shows the cascade of the passive and active boost stages of the equalizer.

Reverse scaling [2] and active feedback techniques are applied to the equalizer path to improve the bandwidth. Although the input of the first active boost stage is not terminated into 50 Ω as in [2], the reverse scaling technique does provide similar bandwidth improvements due to the use of series peaking in the passive stage. Since active feedback trades with gain and voltage headroom, it is applied only to the last stage. Other broadband techniques such as capacitive degeneration, negative Miller capacitors, and inductive peaking [2] are used to increase the bandwidth to about 18 GHz per stage, yielding an overall bandwidth of 7 GHz in the equalizer path.

The phase shift network in Fig. 2 is realized as a single differential pair with capacitive and resistive degeneration to save power and bandwidth. While less than the delay through the equalizer path, the phase shift produced by this stage is adequate for correcting the distortion.

CDR Circuit. Illustrated in Fig. 4, the CDR circuit incorporates an Alexander phase detector (PD) and an LC voltage-controlled oscillator (VCO). To isolate the VCO from the data coupling through the PD flip-flops and to provide large drive capability, the VCO output is buffered by an inductively-loaded differential pair.

For operation at 10 Gb/s, the PD employs current-steering flipflops using class AB tail currents. The current-steering XOR gates must present symmetric paths to avoid systematic

[1] This work supported by Kawasaki Microelectronics.

phase offsets while driving a voltage-to-current (V/I) converter that can accommodate a nearly rail-to-rail range for V_{cont}. This is accomplished by the topology shown in Fig. 4. Here M_1-M_6 form the XOR core [4] and M_7 copies the average output current into M_8. To allow low-voltage operation, the drain voltage of M_7 is raised by $I_1R_1 \approx |V_{THP}|$ above its gate voltage, thus saving one threshold in the headroom.

Experimental Results. The equalizer/CDR circuit has been fabricated in 0.13-µm CMOS technology and tested on a chip-on-board assembly with a 1.6-V supply. Figure 5 depicts the measured input and output eye diagrams at 10 Gb/s for an FR4 trace length of 24 inches that has a loss of 18 dB at 5 GHz. The BER sensitivity graph in Fig. 6(a) indicates that the adaptive equalizer/CDR achieves a BER < 10^{-13} for an input differential swing of 640 mV_{pp}. The circuit consumes 133 mW, of which 41 mW is dissipated in the equalizer and 92 mW in the CDR. The recovered clock achieves a phase noise of −109 dBc/Hz at 1-MHz offset with an rms jitter of 2.22 ps. Figure 6(b) shows a photograph of the die, whose active area measures approximately 0.94 mm x 0.65 mm.

References. [1] K. Krishna, *et al*., "A 0.6 to 9.6Gb/s Binary Backplane Transceiver Core in 0.13µm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 64-65, Feb. 2005.

[2] S. Gondi, *et al*., "A 10Gb/s CMOS Adaptive Equalizer for Backplane Applications," *ISSCC Dig. of Tech. Papers*, pp. 328-329, Feb. 2005.

[3] G. Zhang, M. M. Green, "A BiCMOS 10Gb/s Adaptive Cable Equalizer," *ISSCC Dig. of Tech. Papers*, pp. 482-483, Feb. 2004.

[4] B. Razavi, *et al*., "Design techniques for low-voltage high-speed bipolar circuits," *IEEE J. Solid-State Circuits*, vol. 29, pp. 332-339, Mar. 1994.

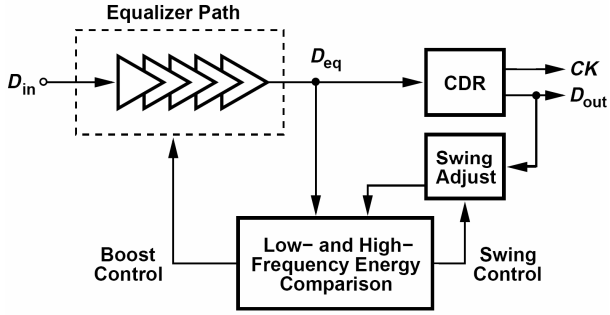


Fig. 1. Merged equalizer/CDR architecture.

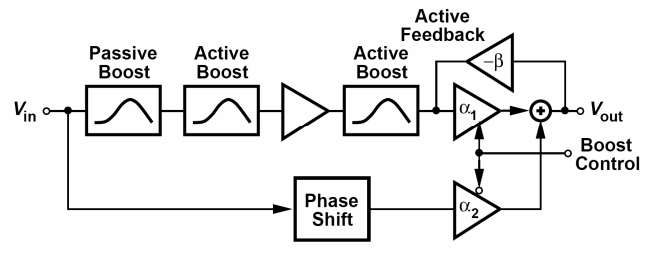


Fig. 2. Equalizer path architecture.

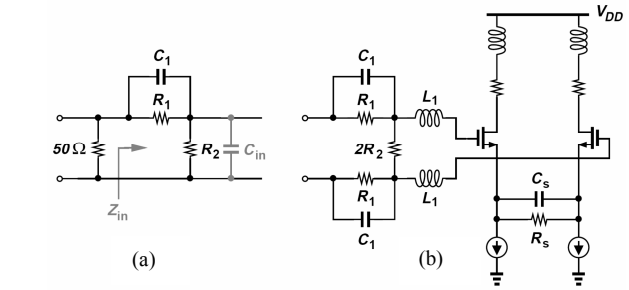


Fig. 3. (a) Passive boost stage, (b) proposed passive and active boost stages.

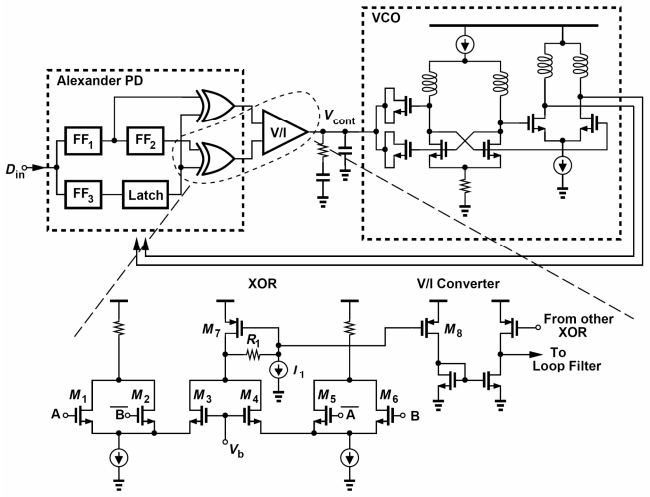
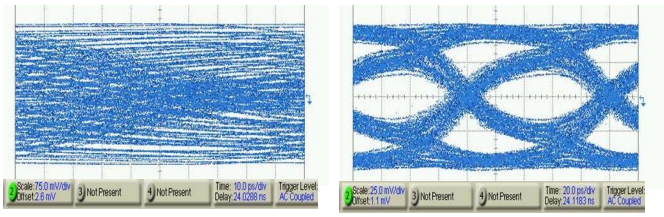
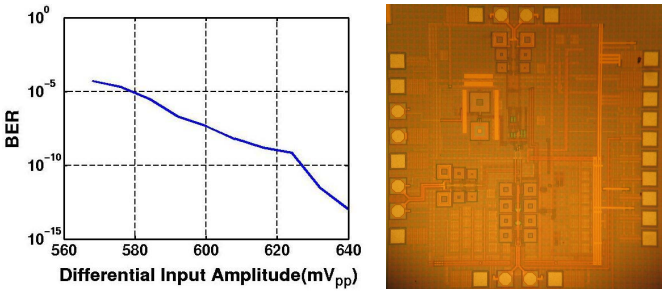


Fig. 4. CDR architecture.



(a) (b)

Fig. 5. Measured results before and after equalization/data recovery at 10 Gb/s for 24-in FR4 trace, [horizontal scale : 20 ps/div, vertical scale : 75 mV/div in (a), 25 mV/div in (b)].



(a) (b)

Fig. 6. (a) BER sensitivity graph, (b) die photograph of adaptive equalizer/CDR.