An 8-Bit 4-GS/s 120-mW CMOS ADC

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Abstract

A four-channel time-interleaved pipelined ADC employs a new timing calibration technique to suppress mismatch-induced spurs and achieve a Nyquist-rate SNDR of 44.4 dB. Designed in 65-nm CMOS technology, the ADC draws 120 mW, providing an FOM of 219 fJ per conversion step.

I. Introduction

The design of gigahertz ADCs greatly benefits from time-interleaving if the interchannel mismatches are corrected efficiently and reproducibly. While offset and gain mismatches can be readily removed by long-term averaging and correction in the digital domain, timing mismatches pose other difficulties. For example, the background calibration proposed in [1] requires digital multipliers and hence a high complexity for more than two channels.

This paper describes a four-channel time-interleaved CMOS ADC that maintains an SNDR of 44 dB up to the Nyquist rate while drawing 120 mW. This performance is achieved through the use of a new background timing mismatch calibration technique requiring no multipliers.

Section II presents the proposed timing mismatch detection technique and its underlying mathematical principles. Section III describes the ADC implementation, including the architecture and the timing mismatch correction circuitry. Section IV summarizes the experimental results for a prototype designed in 65-nm CMOS technology.

II. Timing Mismatch Detection

It is possible to measure the timing mismatch by means of only digital adders. Consider the scenario shown in Fig. 1(a), where sample y_2 is offset from its ideal point in time by ΔT. Noting that the time difference between y_1 and y_2 is $2\Delta T$ seconds greater than that between y_2 and y_3, let us construct Δy_{21}=$|y_2 - y_1|$ and Δy_{32}=$|y_3 - y_2|$. We expect that, with no timing mismatch, Δy_{21} and Δy_{32} exhibit equal averages and surmise that the average value of $\Delta y_{21} - \Delta y_{32}$ is proportional to ΔT. It is difficult to prove this conjecture directly, but if we approximate the absolute value operation by a squaring function, then the proof is as follows. We wish to prove that the average difference between $(y_2 - y_1)^2$ and $(y_3 - y_2)^2$ is proportional to ΔT. To this end, we write the expectation of

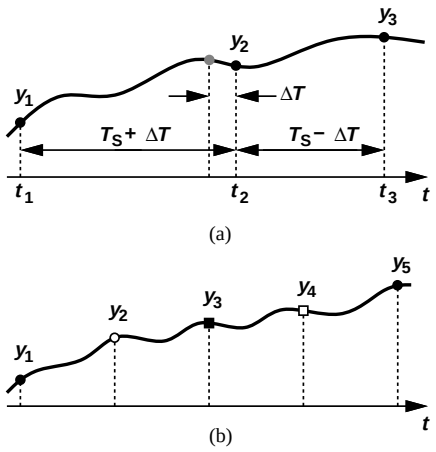

Fig. 1. Waveforms showing effect of timing error in a (a) two-channel or (b) four-channel interleaved ADC system.

$(y_2 - y_1)^2$ as

$$\begin{aligned} E[(y_2 - y_1)^2] &= E[y_2^2] + E[y_1^2] - 2E[y_2 y_1] \\ &= \sigma_{y2}^2 + \sigma_{y1}^2 - 2E[y(t_1 + T_S + \Delta T)y(t_1)], \end{aligned} \quad (1)$$

where σ^2 denotes the average power. We recognize the expectation on the right-hand side as the autocorrelation of $y(t)$, $R(\tau)$, evaluated at $T_S + \Delta T$. That is,

$$E[(y_2 - y_1)^2] = 2\sigma_y^2 - 2R(T_S + \Delta T). \quad (2)$$

Similarly, the average value of $(y_3 - y_2)^2$ is given by

$$E[(y_3 - y_2)^2] = 2\sigma_y^2 - 2R(T_S - \Delta T). \quad (3)$$

For a small ΔT, the two terms on the right-hand side can be approximated by their Taylor series around T_S, yielding

$$E[(y_2 - y_1)^2] - E[(y_3 - y_2)^2] \approx -4\Delta T \frac{dR}{d\tau}. \quad (4)$$

Thus, the average difference between the squares or between $|y_2 - y_1|$ and $|y_3 - y_2|$ can serve as a measure of the mismatch if $dR/d\tau$ does not vanish around $\tau = T_S$.

The above computation of ΔT can be generalized to more than two interleaved channels. Fig. 1(b) shows the case for four. Here, we first consider $|y_3 - y_1|$ and $|y_5 - y_1|$ and detect the timing mismatch between the first and third channels. Once this mismatch is corrected, the third channel can

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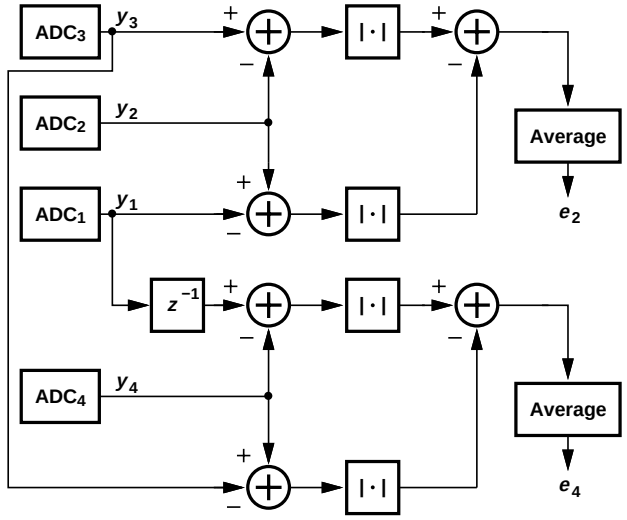


Fig. 2. Timing mismatch detection in a 4-channel ADC system.

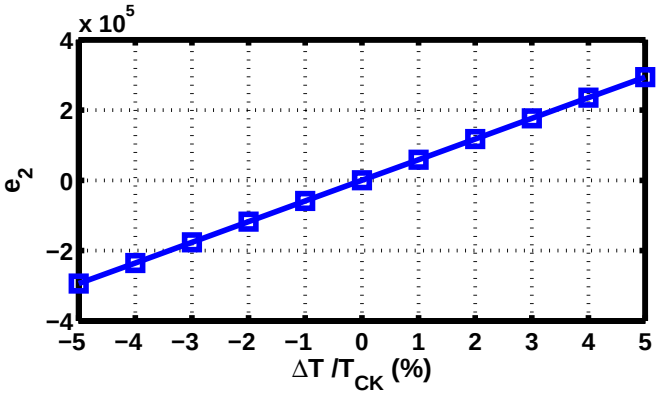
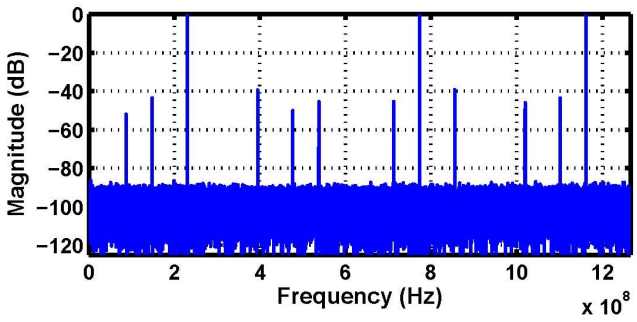
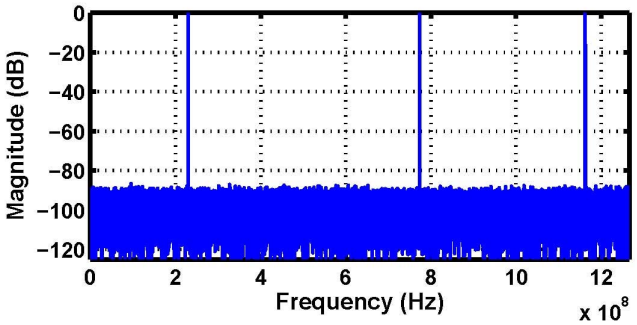


Fig. 3. Simulated error as a function of timing mismatch (arbitrary vertical scale).



(a)



(b)

Fig. 4. Simulated ADC output spectrum (a) before, and (b) after calibration for a multi-tone input.

III. ADC Implementation

A. Architecture

Shown in Fig. 5, the ADC design incorporates four pipelined channels, a phase generator, and a phase correction circuit. Based on the design in [2], each channel consists of a 4-bit first stage, seven 1.5-bit stages, and a 2-bit last stage. The downsampled outputs of the channels are carried off-chip for per-channel gain error calibration, interchannel offset and gain

be considered ideal. Now, as depicted in Fig. 2, we compute the timing mismatch in y_2 by forming the difference between $|y_2 - y_1|$ and $|y_3 - y_2|$ and that in y_4 by forming the difference between $|y_4 - y_3|$ and $|y_5 - y_4|$. Fig. 3 plots, as a example, e_2 versus the displacement of y_2 from its ideal position in time for a random band-limited analog input signal. The error displays a monotonic dependence on ΔT. In another behavioral multi-tone test, Fig. 4 shows the output spectrum for a four-channel ADC before and after calibration with infinite mismatch calibration resolution. We return to the choice of this resolution in Section III.

The digital functions in Fig. 2 require only delay elements and adders. (The absolute value is realized by changing the sign bit). Moreover, to reduce the power consumption, these functions can be enabled for a short time once every few milliseconds to perform the error measurement and kept dormant for the rest of the time [1].

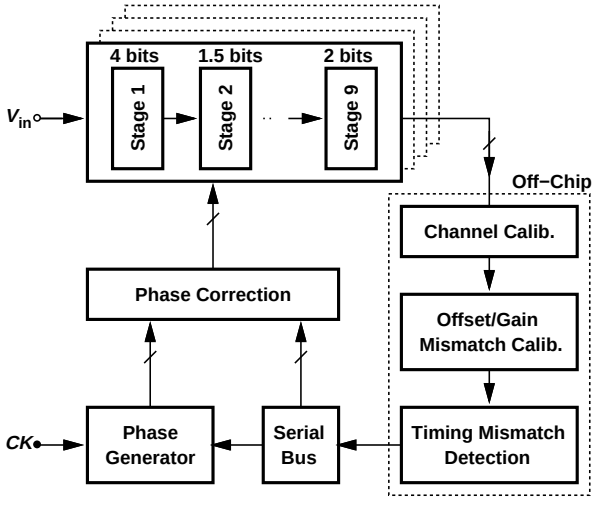


Fig. 5. ADC architecture.

mismatch correction, and timing mismatch detection according to the scheme in Fig. 2. The result of this detection travels back to the chip on a serial bus and adjusts the phase correction circuit.

B. Phase Generation and Correction

The ADC generates four 1-GHz clock phases with a duty cycle of about 25%[1] (Fig. 6). These phases are then adjusted according to the results of timing mismatch detection.

The phase correction circuit must provide (1) a wide enough tuning range to accommodate the maximum anticipated mismatch, ΔT_{max}, and (2) a sufficiently fine step size, ΔT_{min}, to minimize the SNDR penalty due to the residual timing mismatch. It is important to note that the mismatch arises in both the clock paths and the analog signal paths leading to the channels. In this work, we select ΔT_{max}=3.5 ps and ΔT_{min}=30 fs.

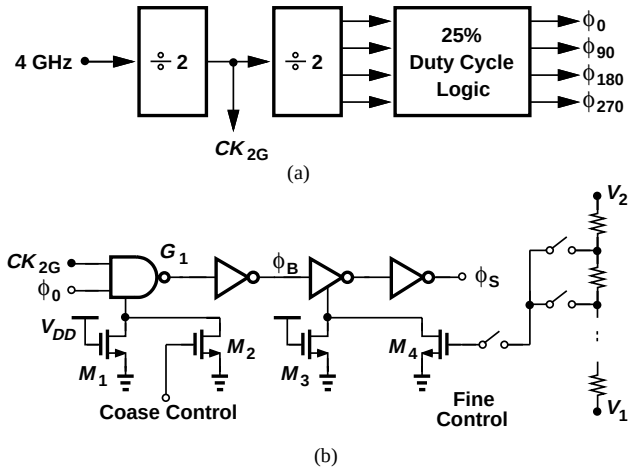


Fig. 6. (a) Phase generation, and (b) phase adjustment circuits.

In order to achieve the above values for ΔT_{max} and ΔT_{min} with minimal phase noise, power, and complexity, we employ, in the clock path of each channel, a short variable delay line (VDL) with a 1-bit coarse control and a 6-bit fine control. Illustrated in Fig. 6(b), the VDL incorporates transistors M_1 and M_2 to adjust the strength of the NAND gate G_1. The relative widths of M_1 and M_2 determine the absolute delay step that the latter can create. In this design, W_2=1.6W_1 and L_1=L_2.

The fine delay adjustment is realized by M_4, whose gate voltage can be varied from V_1 ($\approx V_{TH}$) to V_2 in 64 steps. With W_3=2.25W_4 and L_3=L_4, this scheme provides a ΔT_{min} of 30 fs. Note that CK_{2G} gates the phase entering this circuit so as to remove the skew and phase noise contributed by the second $\div 2$ circuit and the logic in Fig. 6(a). The ADC employs four VDLs to adjust ϕ_0-ϕ_{270}. The phase generation and correction circuits consume a total of 17.7 mW at full rate.

[1]Each channel allocates 25% of its clock cycle to sampling and 75% to conversion.

IV. Experimental Results

The four-channel ADC has been fabricated in 65-nm digital CMOS technology. Fig. 7 shows the die photograph of the prototype, which occupies an active area of 900 μm $\times$1500 μm. All of the measurement results are reported for a sampling rate of 4 GHz.

Fig. 8 plots the measured DNL and INL after per-channel gain error calibration, indicating a maximum of -0.75 LSB for the former and -1.5 LSB for the latter after calibration.

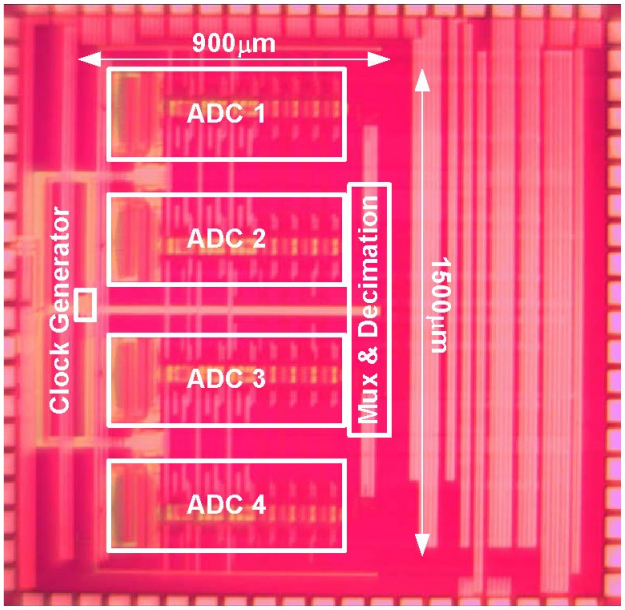


Fig. 7. Prototype ADC micrograph.

Fig. 9 shows the convergence of the phase adjustment codes for channel 2 and 4 in response to a 1.9-GHz sinusoidal input after channel 3 is calibrated as explained in Section II and Fig. 10 depicts the corresponding improvement in the SNDR. Plotted in Fig. 11 is the subsampled output spectrum before and after timing mismatch calibration, demonstrating that the mismatch-induced spurs can be suppressed to about -60 dB.

Fig. 12 plots the SNDR as a function of the analog input frequency. The ADC consumes 120 mW: 57 mW in the analog section, 46 mW in the digital section, and 16 mW in the reference ladders. Table 1 compares our prototype's performance to that of recent gigahertz ADCs with an SNDR range of 44 to 49 dB.

Acknowledgments

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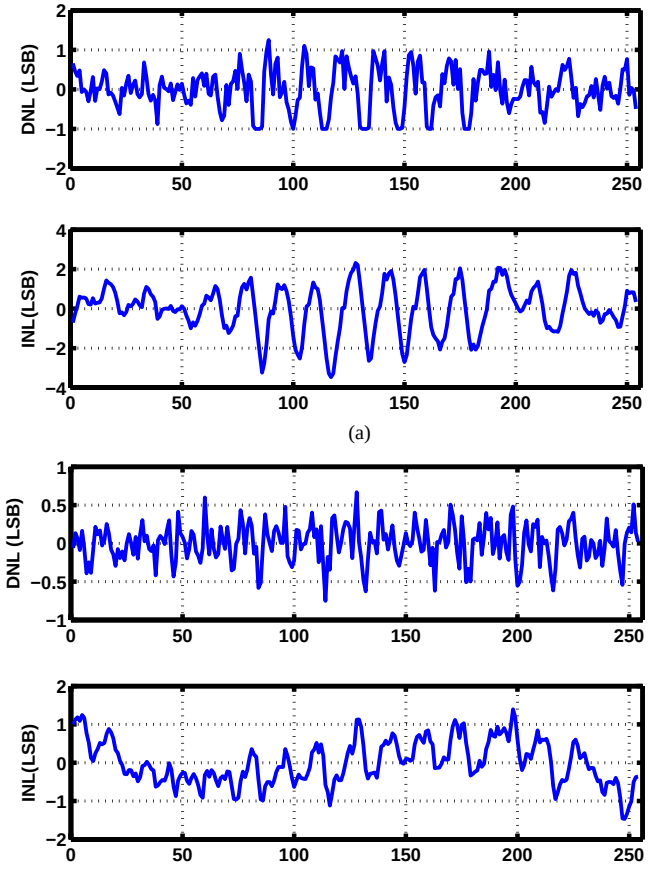

Fig. 8. Measured DNL and INL at a clock rate of 4 GS/s, (a) before , and (b) after per-channel calibration.

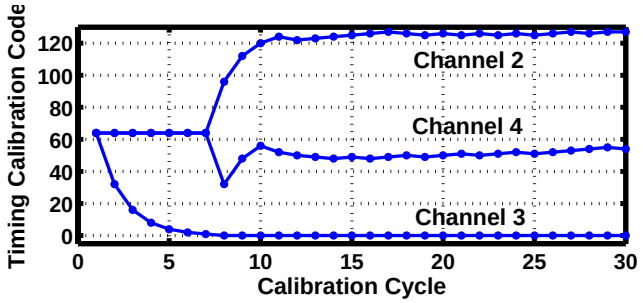

Fig. 9. Measured timing calibration code convergence.

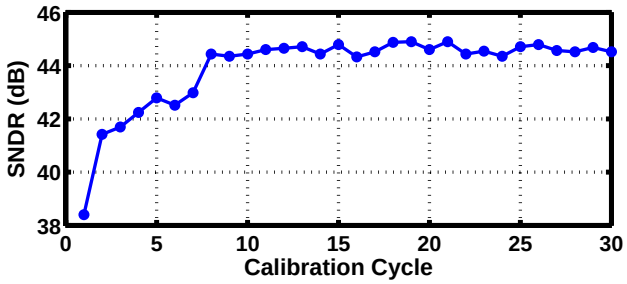

Fig. 10. Measured SNDR during convergence of timing calibration.

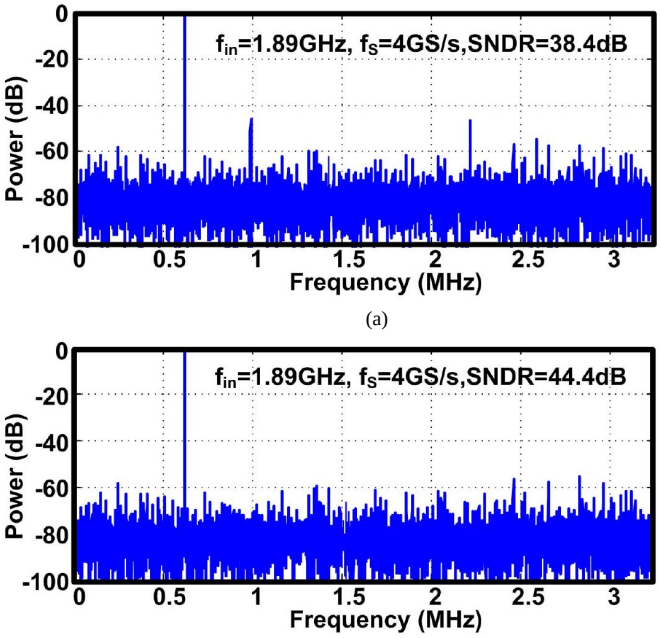

Fig. 11. Measured output spectrum (a) before, and (b) after timing mismatch calibration (decimated by a factor of 625).

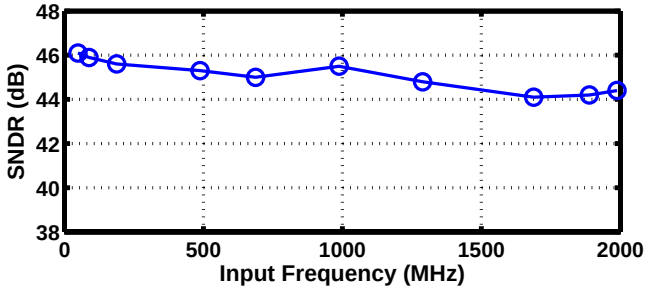

Fig. 12. Measured SNDR as a function of f_{in} at 4 GS/s.

	This Work	JSSC'12 [4]	ISSCC'13 [5]	ISSCC'11 [6]
f_S (GS/s)	4	3	3.6	2.6
SNDR @ Nyq. (dB)	44.4	49	47.5	48.5
Supply (V)	1.2/1.4	2.5	1.2/2.5	1.2/1.3/1.6
Power (mW)	120	500	795	480
FOM (fJ)	219	724	1140	1000
Tech. (nm)	65	40	65	65
Area (mm^2)	1.35	0.4	7.4	5.12

Table 1. Comparison with state-of-the-art designs.