

WP 23.6 A 2.6GHz/5.2GHz CMOS Voltage-Controlled Oscillator*

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New wireless local area network (WLAN) standards have recently emerged in the 5GHz band. For example, High Performance Radio LAN (HIPERLAN) is a European standard operating at 5.2GHz with Gaussian minimum shift keying (GMSK) modulation and a 23MHz channel bandwidth. The voltage-controlled oscillator reported here is to be used in a HIPERLAN transceiver as shown in Figure 23.6.1. Here, the receiver employs two downconversion steps, each with a 2.6GHz local oscillator (LO) frequency, translating the RF spectrum to dc. The second downconversion thus requires the quadrature phases of the LO. The transmitter performs modulation by first placing the VCO in a synthesizer loop and subsequently opening the loop and applying the Gaussian-shaped baseband data to the VCO to perform GMSK modulation.

The VCO core is based on two 2.6GHz coupled oscillators operating in quadrature, as shown in Figure 23.6.2a [1, 2]. The fully differential topology of each oscillator raises the possibility of sensing the common-source nodes A, B, C, or D as the 5.2GHz output. In fact, since the 2.6GHz oscillators operate in quadrature, the waveforms at nodes A and B (or C and D) are 180° out of phase, thereby serving as a differential output at 5.2GHz. Proper sizing and biasing of the transistors yields a relatively large amplitude for the 5.2GHz signal - approximately 0.5V differential.

The tuning of the oscillator poses several difficulties: the varactor diode must exhibit a small series resistance and remain reverse-biased even with large swings in the oscillator; the varactor capacitance must be large enough to yield the required tuning range, but at the cost of increasing the power dissipation or the phase noise. This design incorporates a p^+n^+ diode inside an n-well and strapped with metal to reduce the n-well series resistance [2]. Such a structure suffers from a large parasitic n-well/substrate capacitance, making it desirable to connect the anode of the diode to the oscillator. This is accomplished as shown in Figure 23.6.2b where the control voltage varies the dc potential at nodes X and Y by varying the on-resistance of M_3 .

However, the sharp variation of the on-resistance creates significant change in the gain (sensitivity) of the VCO. To make the transition smoother, another transistor, M_4 , in series with a resistor is added as shown in Figure 23.6.2c. Transistor M_5 serves as a clamp, keeping the tail current source in saturation. Otherwise, the oscillator may turn off during synthesizer loop transients. Since the minimum voltage at node A is only a few hundred millivolts above ground, an nMOS differential pair cannot directly sense the 5.2GHz signal at this node. For this reason, a common-gate stage is used [Figure 23.6.2 d]. But if V_b is constant, then M_6 turns off for low values of V_{cont} . Modifying the circuit as shown in Figure 23.6.2 e, ensures that the common-gate stage carries a constant bias current across the full tuning range.

The choice of the inductors and capacitance of the varactors leads to a compromise between the phase noise and the tuning range. In this design 7nH inductors are used, each contributing a parasitic capacitance of 120fF. The cross-coupled transistors are relatively wide ($W/L=60\mu\text{m}/0.4\mu\text{m}$) to ensure startup, yielding approximately 175fF of gate-source capacitance. The differential pairs coupling the two oscillators also load the tanks. As a result, the varactor capacitance for 2.6GHz operation is approximately equal to 160fF. The inductors are realized as stacked spirals made of metal 4 and metal 3 with 6 μm line width.

Direct generation of a 5.2GHz signal would impose severe trade-offs on the design. Since the value of the inductor would have to be smaller to achieve a higher self-resonance frequency, and since skin effect and substrate loss would further limit the Q, the phase noise, which is proportional to $(\omega/\Delta\omega)^2/Q^2$, would increase dramatically.

The VCO is fabricated in a 0.35 μm CMOS technology and tested with a 2.5V supply. Figure 23.6.3a and b show the measured output spectra at 2.6GHz and 5.2GHz, respectively. In measuring the phase noise from the spectrum, it is important to calculate the carrier power correctly. Note that for a narrow span and a small resolution bandwidth, flicker noise fluctuations "smear out" the carrier, thus underestimating its average power. For this reason, the carrier power is measured with a wider span.

For HIPERLAN applications, the phase noise at 23MHz offset, i.e., in the adjacent channel, is of interest. The spectra of Figure 23.6.3 a and b indicate that the phase noise approaches a constant value at about 5MHz offset. This value is -110dBc/Hz at 2.6 GHz and -104.5dBc/Hz at 5.2GHz with 26mW dissipation. Figure 23.6.4 shows the tuning characteristic of the VCO. The tuning range is 347MHz.

Coupled oscillators tend to operate at many frequencies simultaneously if the coupling coefficient is not sufficiently strong. This behavior, shown in Figure 23.6.5, results if the bias current of the differential pairs coupling the two oscillators is decreased substantially. Table 23.6.1 summarizes the VCO performance.

References:

- [1] Rofugaran, A., et al, "A 900MHz CMOS LC Oscillator with Quadrature Outputs," ISSCC Digest of Technical Papers, pp 392-393, Feb., 1996
- [2] B. Razavi, "A 1.8GHz CMOS Voltage-Controlled Oscillator," ISSCC Digest of Technical Papers, pp 388-389, Feb, 1997.

VCO frequency	2.6 GHz/5.2 GHz
Tuning range	320 MHz
Phase noise	-110 dBc/Hz @ 5-MHz offset for 2.6 GHz
	-104.5 dBc/Hz @ 5-MHz offset for 5.2 GHz
Supply current	5.2 mA/osc
Supply voltage	2.5 V
Technology	0.35 μm CMOS

Table 23.6.1: VCO performance.

*This work was supported by Lucent, Rockwell, the California MICRO program, and a Hewlett-Packard equipment grant.

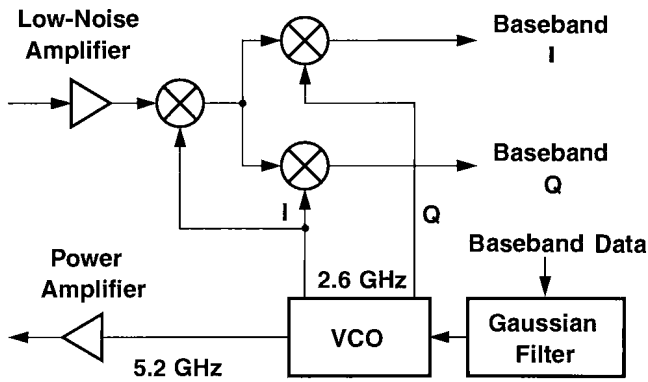
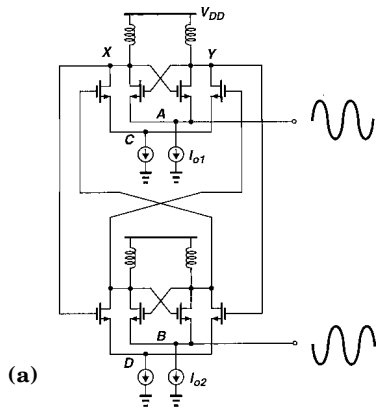


Figure 23.6.1: Transceiver topology.



(a)

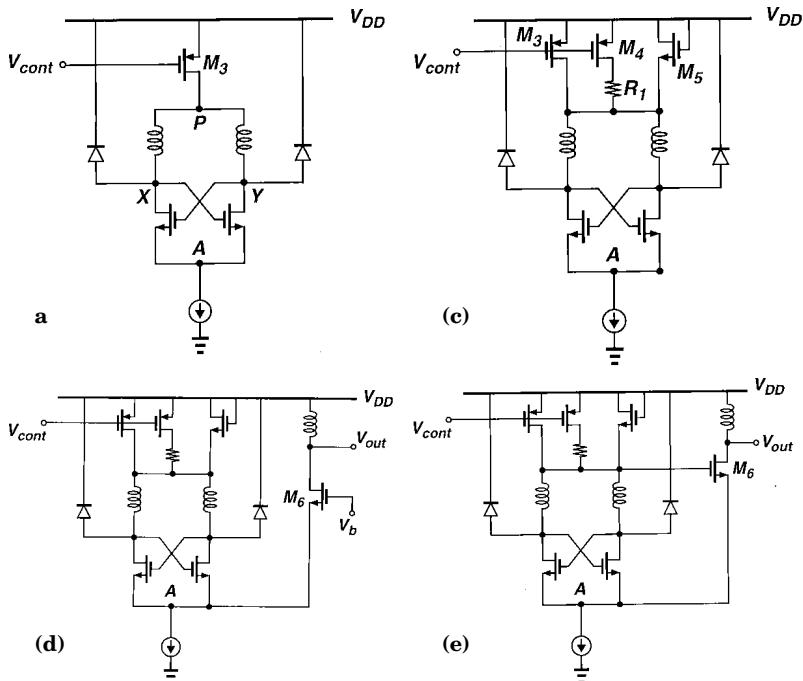
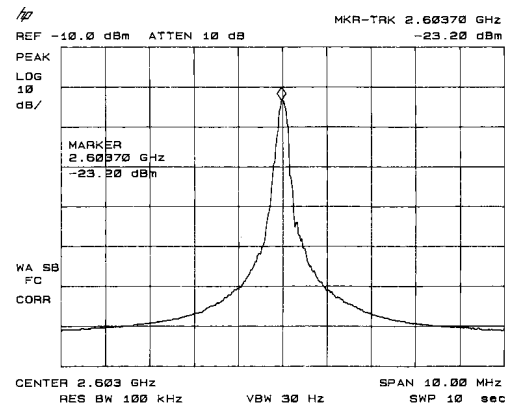
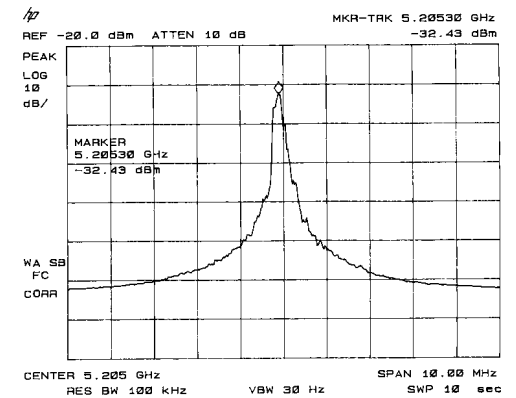


Figure 23.6.2: VCO evolution.



(a)



(b)

Figure 23.6.3: Measured output spectra at: (a) 2.6GHz b) 5.2GHz.

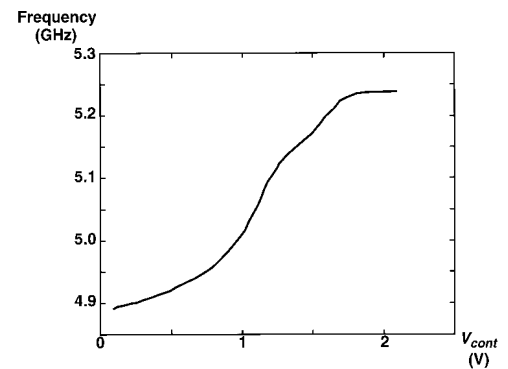


Figure 23.6.4: Measured tuning characteristic.

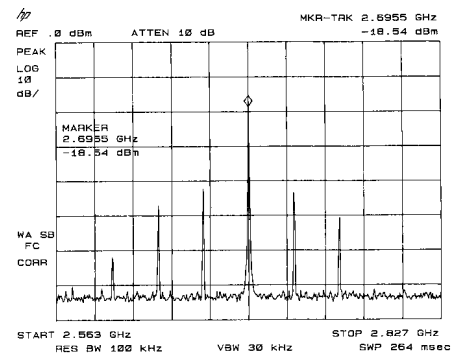


Figure 23.6.5: Output spectrum when coupling coefficient is weak.

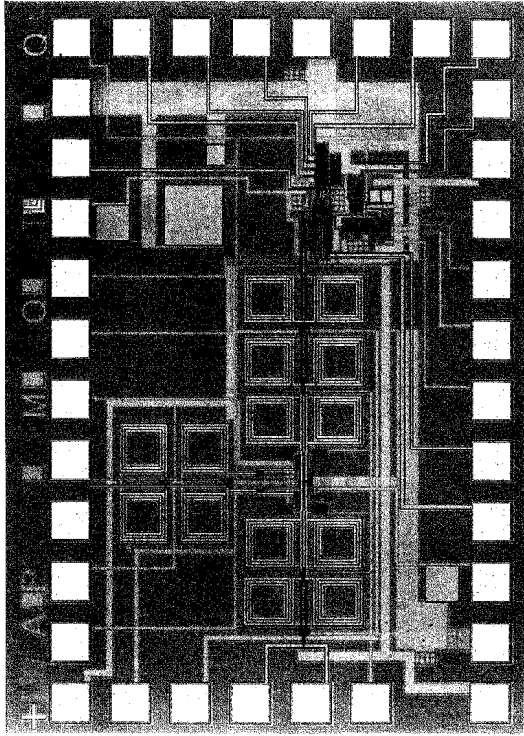


Figure 23.6.6: Chip micrograph

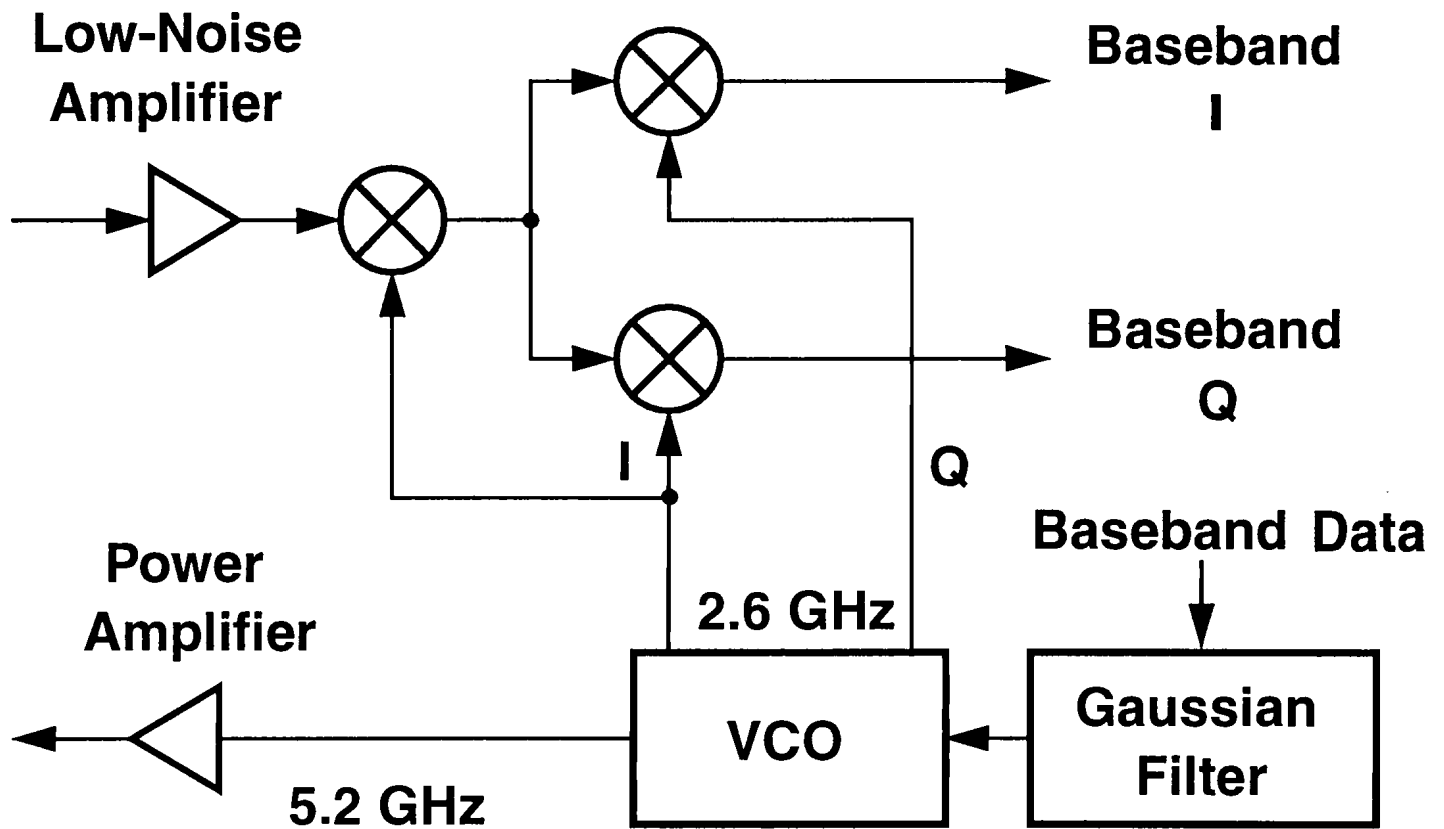


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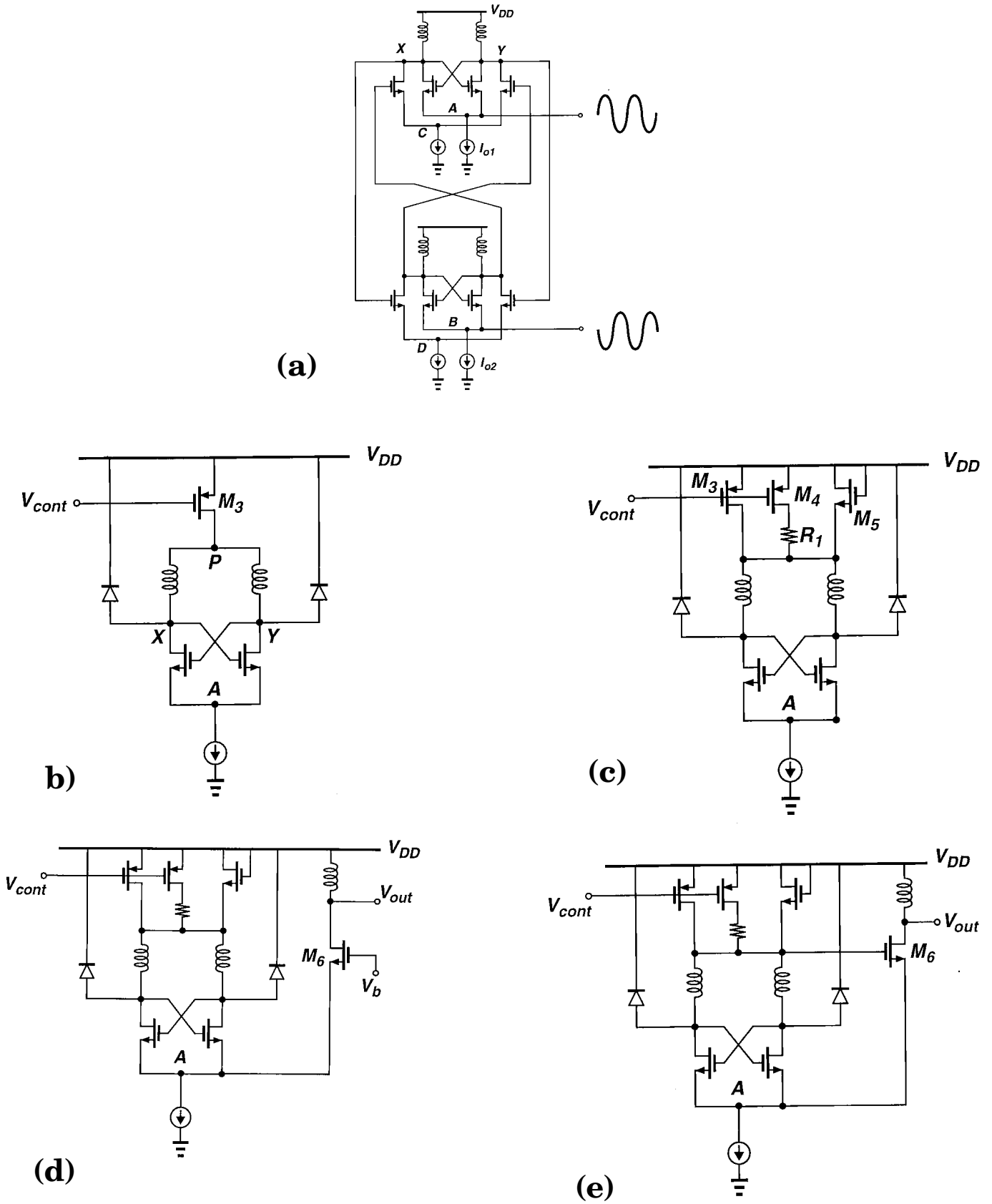
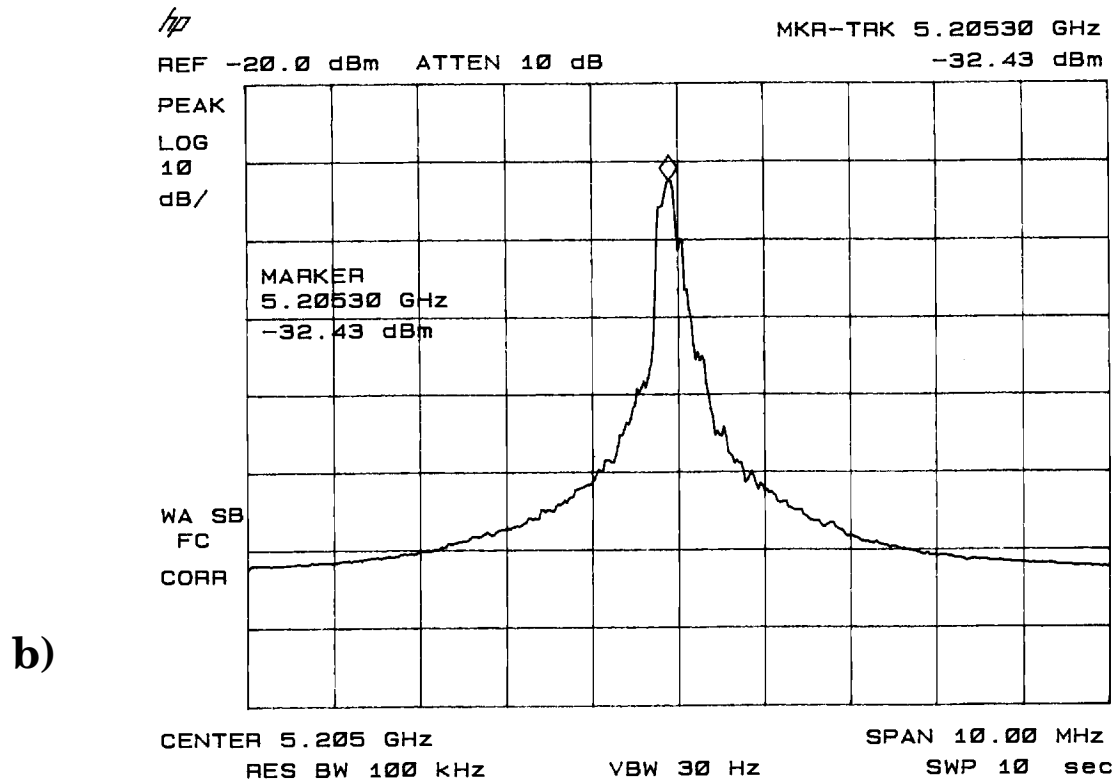
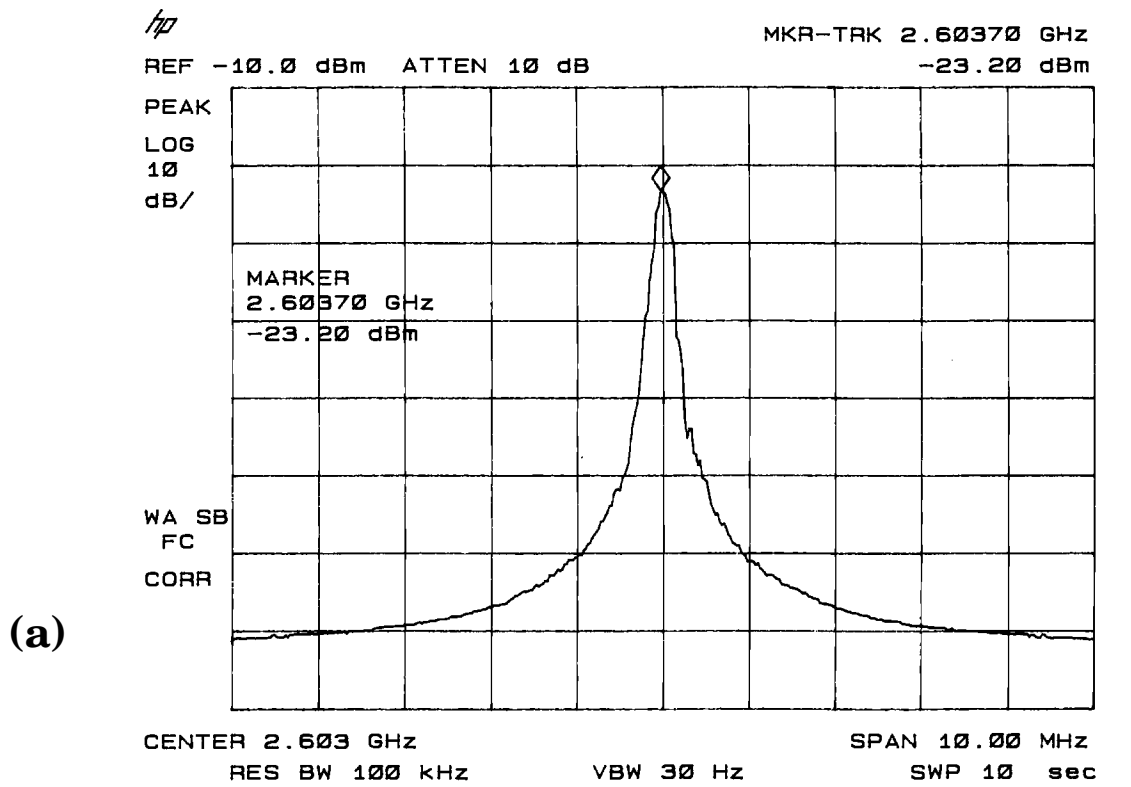


Figure 23.6.2: VCO evolution.



**Figure 23.6.3: Measured output spectra at:
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Frequency
(GHz)

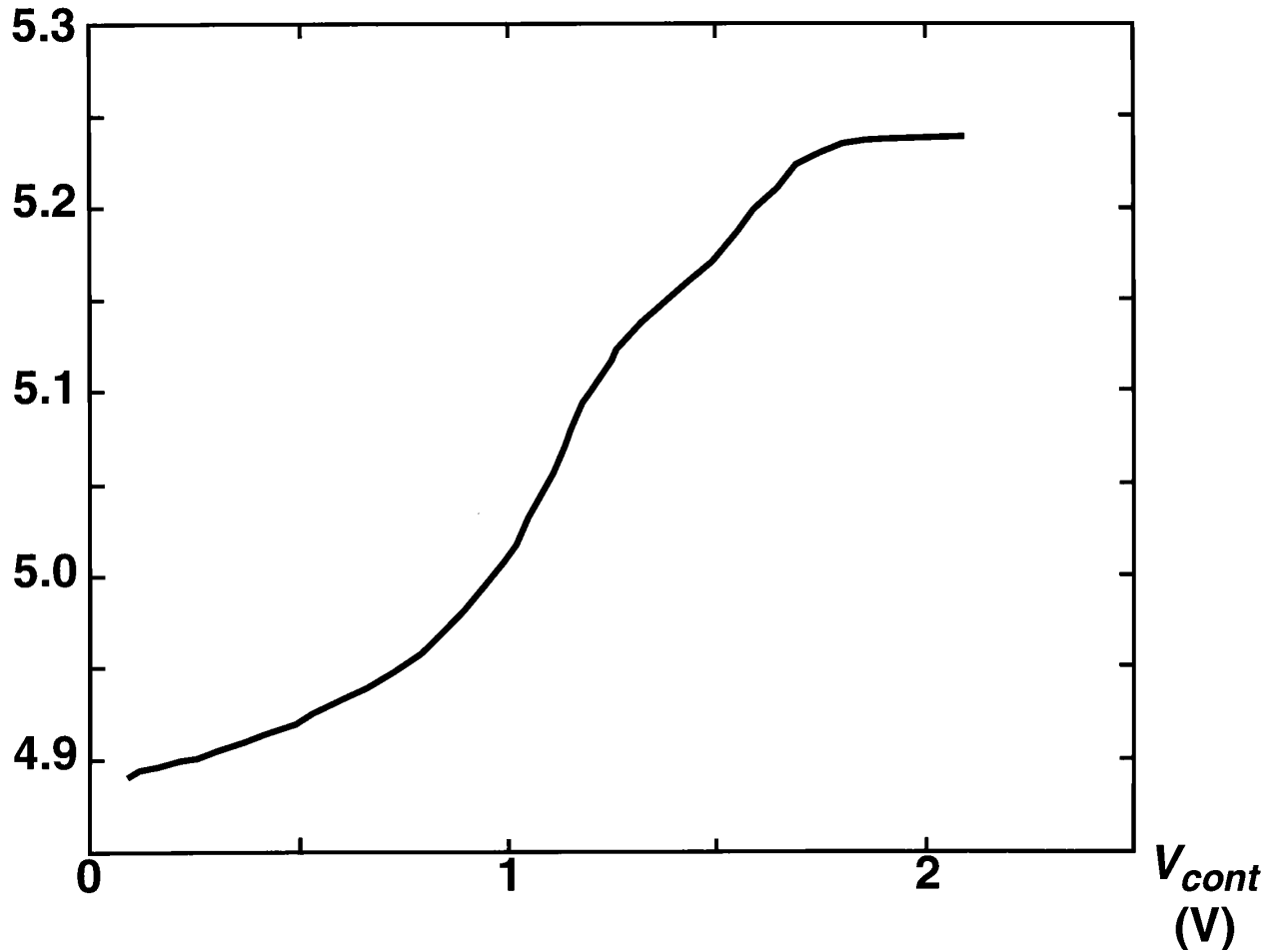


Figure 23.6.4: Measured tuning characteristic.

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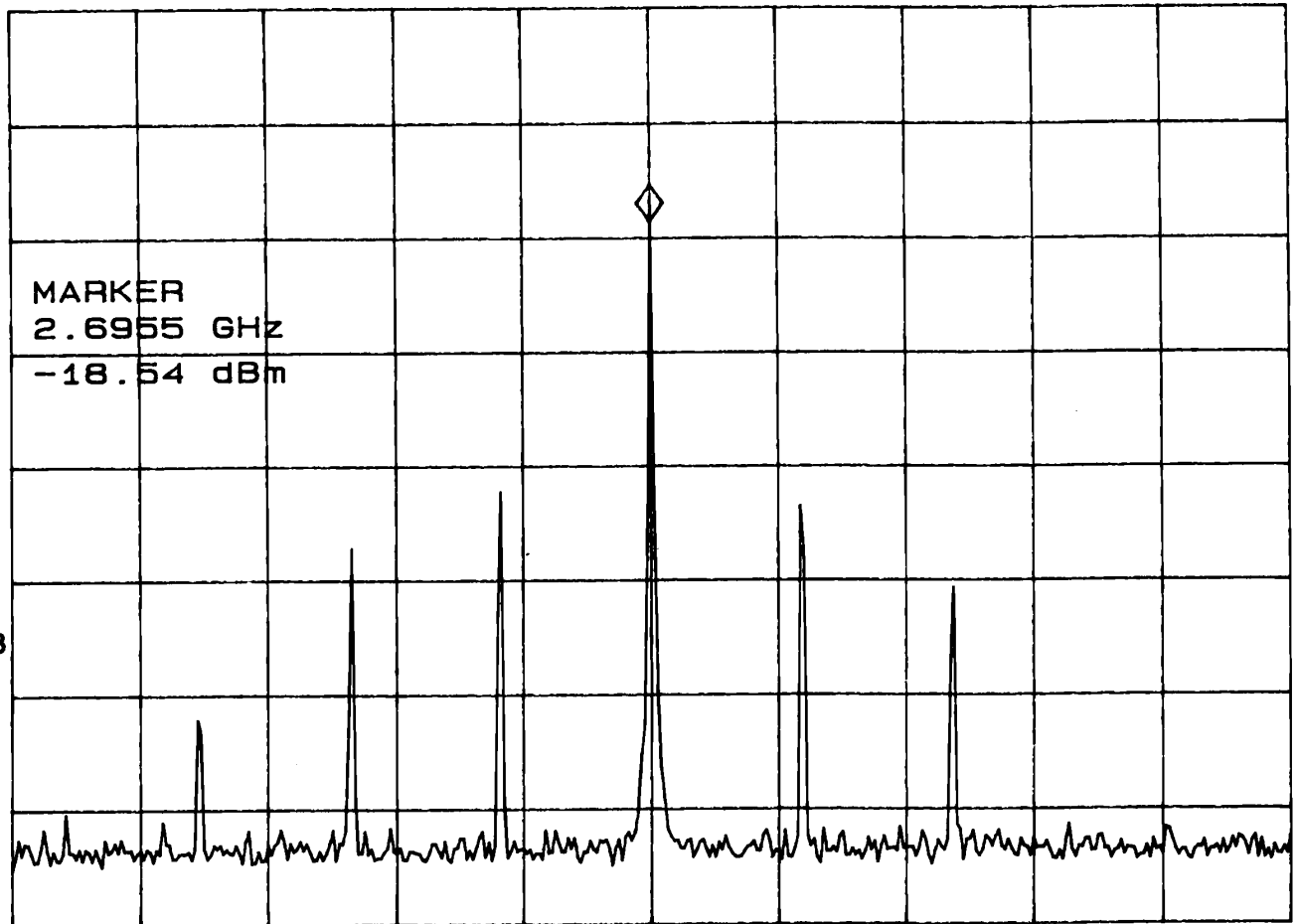
MKR-TRK 2.6955 GHz

REF .0 dBm

ATTEN 10 dB

-18.54 dBm

PEAK
LOG
10
dB/



START 2.563 GHz

RES BW 100 KHz

VBW 30 KHz

STOP 2.827 GHz

SWP 264 msec

Figure 23.6.5: Output spectrum when coupling coefficient is weak.

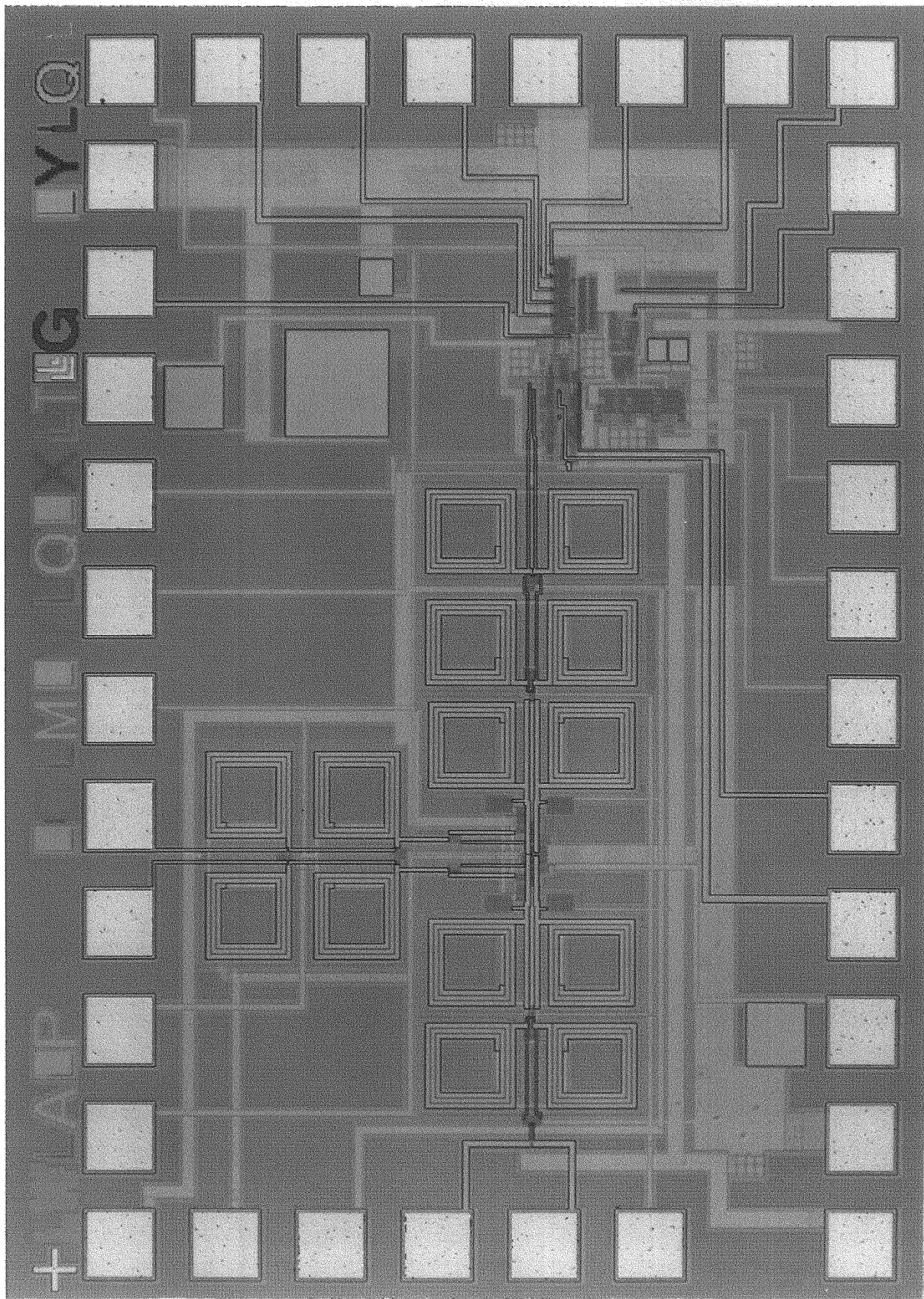


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