9.6 A 60GHz CMOS Receiver Using a 30GHz LO

Ali Parsa, Behzad Razavi

University of California, Los Angeles, CA

Recent work on receivers for the 60GHz band has considered various frequency plans to ease the design of the building blocks, particularly the local oscillator (LO) and the frequency dividers [1-3]. A natural choice of the LO frequency in a heterodyne system is half of the input frequency as it places the image in the vicinity of zero while greatly simplifying the design and distribution of the LO and divider signals [4]. Unfortunately, a simple heterodyne chain consisting of a single RF mixer and quadrature IF mixers suffers from an additional image introduced by the third harmonic of the LO in the RF mixing operation, which flips the signal spectrum horizontally and superimposes it on the original downconverted spectrum. Since the third harmonic of the LO is only 9.5dB lower, this corruption proves serious in modulation schemes having asymmetric spectra, e.g., FM, QPSK, and QAM.

This paper describes a heterodyne receiver architecture that incorporates a 30GHz LO without quadrature phases and resolves the issue of the third harmonic of the LO as well. The architecture thus lends itself better to integration and signal distribution while consuming lower power.

With a 30GHz LO, the switching of the RF mixer convolves the +90GHz harmonic with the signal spectrum at –60GHz, thus translating this spectrum to +30GHz. This component is only 9.5dB below the desired component, which is the result of translating the +60GHz signal spectrum to +30GHz. Any attempt to linearize the LO port of the mixer so as to raise this ratio substantially degrades the conversion gain and increases the noise figure.

As shown in Fig. 9.6.1, the proposed receiver performs quadrature separation in the RF path and downconverts the signal to 30GHz and subsequently to baseband. Figure 9.6.2 illustrates the operation by showing the spectra at various points along the receiver chain. By virtue of quadrature separation, the positive frequency content of the signal is removed; i.e., mixers MX_1 and MX_2 sense a complex RF signal, $[I_1, Q_1]$, that contains energy only around –60GHz. These mixers are also driven by the 30GHz LO frequency and its third harmonic. Upon mixing, MX_1 and MX_2 produce output currents that, viewed as a complex signal $[I_2, Q_2]$, contain (1) the main component around –30GHz, (2) a replica at +30GHz that is 9.5dB lower in magnitude, and (3) a component shifted to –90GHz. Since the output currents of these mixers flow through load tanks resonating at 30 GHz, the –90GHz component is attenuated by 25dB. Consequently, MX_3 and MX_4 sense a complex IF signal that carries the main signal spectrum, S_1, at –30GHz and its attenuated replica, S_2, at +30GHz. The IF mixers therefore generate a complex baseband signal, $[I_B, Q_B]$, equal to the sum of S_1 and S_2. Note that, even though the RF signal spectrum is asymmetric, the complex processing makes it possible for S_2 to *enhance* S_1 rather than corrupt it.

In the presence of mismatches in the polyphase filter, the complex spectrum sensed by MX_1 and MX_2 contains a small replica of the signal at +60GHz, which upon mixing with –90GHz, appears at –30GHz and eventually at baseband. The advantage of the proposed architecture is to suppress this component by 9.5dB plus the image rejection ratio (IRR) of the polyphase filter. For example, with a 0.5dB gain mismatch and a 5° phase mismatch, the unwanted replica remains 35dB below the desired signal.

Quadrature separation in the RF signal path entails issues arising from loss, noise, and loading effects. While suited to frequencies in the range of 20GHz, the current-mode phase shifter in [1] would call for impractically small capacitor values at 60GHz. Also, the microwave couplers proposed in [5] require a large area and accurate impedance matching. To obtain a reasonable image rejection as well as practical component values, a 2-stage polyphase filter is used in this design. The filter also converts the single-ended output of the LNA to differential form, allowing the use of a double-balanced mixer and hence reducing the LO-IF feedthrough that would otherwise desensitize the IF mixers.

Figure 9.6.3 shows the implementation of the LNA and the polyphase filter. A cascode topology is followed by a common-source stage to drive the polyphase filter. The polyphase driver both compensates for the loss of the polyphase filter and lowers its noise contribution to the overall noise figure of the system. To resonate the capacitance at the cascode node (source of M_2), L_3 (=100pH) performs series peaking. In contrast to shunt peaking, this method requires a smaller inductor and, more importantly, does not necessitate a bypass capacitor to a low-impedance ground plane. To maintain a reasonable image rejection and small loss in the polyphase filter, the output must be connected to a relatively high impedance. In this design, R_1=120Ω, R_2=130Ω and $C_{1,2}$=20fF. The LNA draws 8mA from the supply and, along with the polyphase filter, provides a total gain of 13dB and a noise figure of 4dB.

Figure 9.6.4 depicts the RF and IF mixer realization for each path (I or Q). A low-current cross-coupled pair is placed at the output of the RF mixer to raise the gain by 3dB while allowing a reasonable margin from instability. The IF mixer incorporates capacitive coupling between the input transconductor and the switching quad so as to permit independent choice of bias currents and hence optimum conversion gain and noise figure [1]. The RF and IF mixer chain draws 20mA and exhibits a noise figure of 18dB. The differential on-chip LO is realized as a negative-G_m cell with a symmetric inductor. The LO directly drives the capacitance of the four double-balanced mixers to avoid additional inductors that would be required by buffers.

Figure 9.6.7 shows the die micrograph of the receiver. The receiver is fabricated in a 90nm digital CMOS process. The tests are performed on a high-frequency probe station with the DC pads bonded to a PCB. The active area is approximately 500×370μm^2.

Figure 9.6.5 shows the plots of the measured noise figure, gain, and I/Q mismatch across the input frequency range. Figure 9.6.6 compares the measured performance of the receiver with that of the receivers in references [1] and [3].

Acknowledgments:
The authors thank Realtek Semiconductor and Skyworks, for support of this work and TSMC for chip fabrication.

References:
[1] B. Razavi, "A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider," *ISSCC Dig. Tech. Papers*, pp. 188-189, Feb. 2007.
[2] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer et al., "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE J. Solid-State Circuits*, vol.41, no.12, pp 2820-2831, Dec. 2006.
[3] S. Emami, C. H. Doan, A. M. Niknejad and R. W. Brodersen, "A Highly Integrated 60GHz CMOS Frond-End Receiver," *ISSCC Dig. Tech. Papers*, pp. 190-191, Feb. 2007.
[4] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 810-815, May 2001.
[5] C.-H. Wang, H.-Y. Chang, P.-S. Wu et al., "A 60GHz Low-Power Six-Port Transceiver for Gigabit Software-Defined Transceiver Applications," *ISSCC Dig. Tech. Papers*, pp.192-193, Feb. 2007.

 978-1-4244-2011-7/08/$25.00

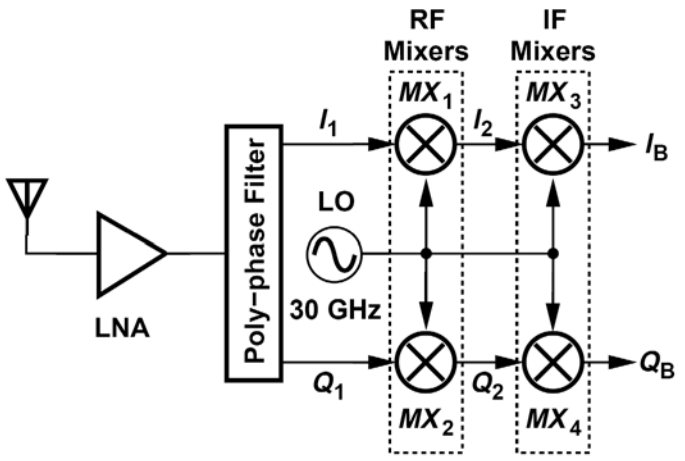

Figure 9.6.1: Receiver architecture.

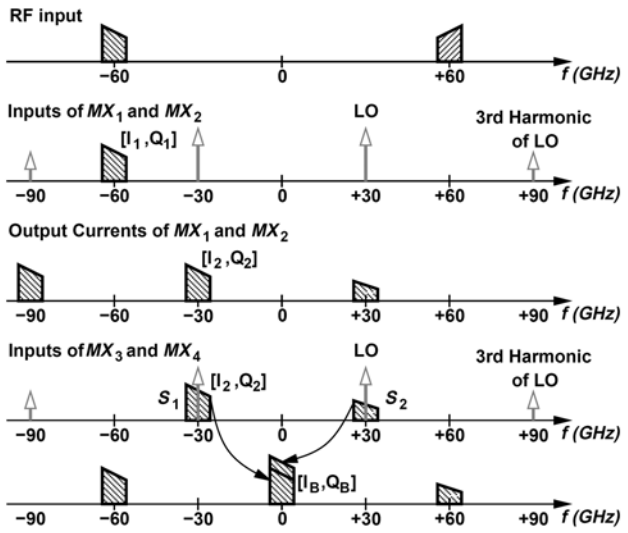

Figure 9.6.2: Signal spectra along the receiver chain.

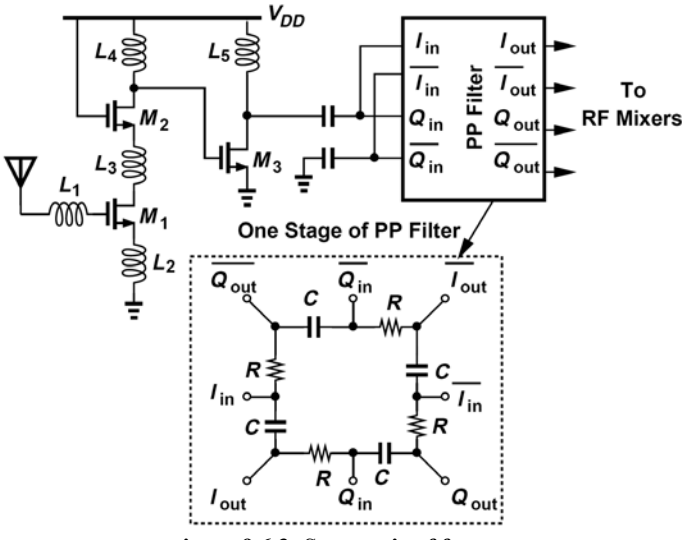

Figure 9.6.3: Schematic of front-end.

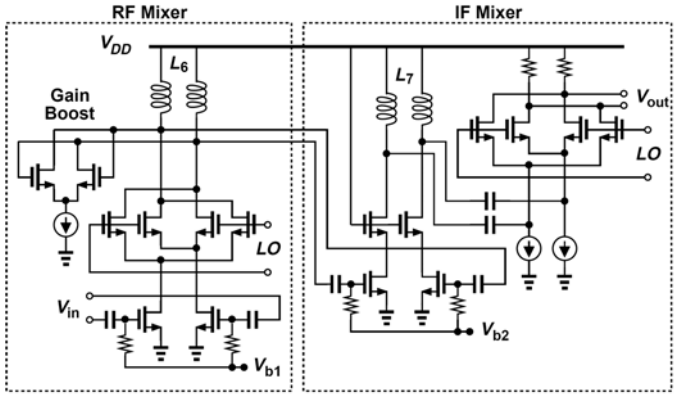

Figure 9.6.4: Schematic of RF and IF mixers.

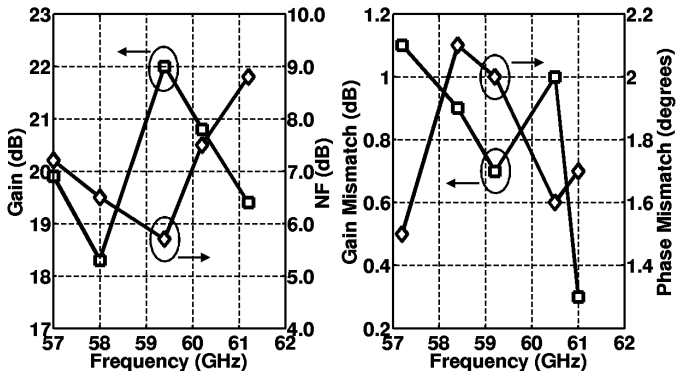

Figure 9.6.5: Plot of gain, noise figure and gain and phase mismatch versus input frequency.

	Receiver in [3]	Receiver in [1]	This work
Noise Figure (dB)	10.4 to 11	6.9 to 8.3	5.7 to 8.8
Gain (dB)	4 to 12	26 to 31.5	18.3 to 22
P_{1dB} (dBm)	-15.8	-25.5	-27.5
LO Leakage to Input (dBm)	N/A	-47	-65
I/Q Mismatch	N/A	6.5°/ 1.5dB	2.1°/ 1.1dB
LO Phase Noise (dBc/Hz @ 1MHz offset)	-86	-95	-87
Power Dissipation (mW)	77	80	36
Supply Voltage (V)	1.2	1.8	1.2
Technology	0.13µm CMOS	90nm CMOS	90nm CMOS

Figure 9.6.6: Measured performance of the receiver.

Continued on Page 606

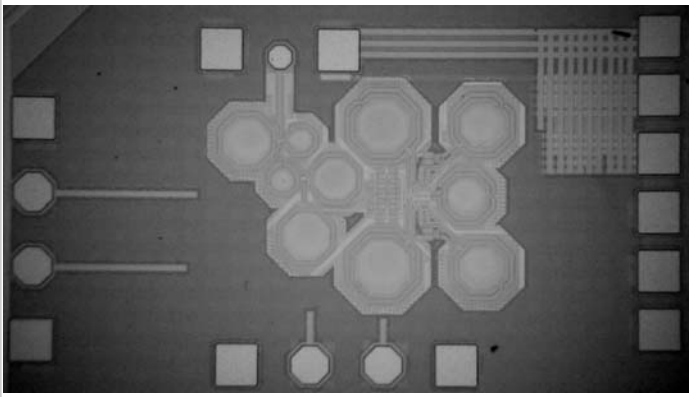

Figure 9.6.7: Die micrograph of the receiver.

 978-1-4244-2011-7/08/$25.00