A Harmonic-Rejecting CMOS LNA for Broadband Radios

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Abstract—A feedback LNA employs programmable notch filtering so as to suppress by 20 dB blockers at LO harmonics from 300 MHz to 10 GHz. Fabricated in 65-nm technology, the LNA exhibits a noise figure of less than 3 dB from 300 MHz to 4 GHz while consuming 8.6 mW from a 1.2-V supply.

A critical issue in broadband receivers relates to the mixing of the local oscillator (LO) harmonics with large blockers, and has been addressed by harmonic-rejection mixers (HRMs) in recent work [1, 2]. However, rejection levels of 60 dB or higher have been obtained for input frequencies only up to 800 MHz. For radios operating with a wider bandwidth, e.g., 10 MHz, HRMs do not readily provide such rejection levels because the LO phase mismatches must be corrected to within 150 fs and the mixer gains to within 0.1 %. Moreover, HRMs do not suppress harmonics above the fifth order unless many more LO phases are available.

This paper proposes that a programmable harmonic-rejecting low-noise amplifier (LNA) can greatly relax the accuracies required of the HRMs and their LO phases. In this work, a rejection of at least 20 dB is targeted so as to afford a tenfold improvement in the overall receiver’s tolerance of blockers located at the LO harmonics. In addition, the filteration provided by the LNA also suppresses all blockers above the third harmonic of the LO.

LNA Architecture The design of a broadband harmonic-rejecting LNA faces a number of challenges: (1) the circuit must incorporate a programmable notch in its frequency response that can be varied by more than one decade without degrading the other LNA parameters, such as the noise figure and the input return loss; (2) the notch frequencies must be calibrated so that, upon receiving a desired channel, the notch can be accurately positioned atop the targeted LO harmonic. The LNA reported here is designed for a frequency range of 100 MHz to 10 GHz, requiring that the notch vary from 300 MHz to 10 GHz. Fig. 1 shows the proposed LNA architecture. The amplifying core consists of the three stages $M_1$-$M_4$ and the feedback resistor $R_F$. In a manner similar to the topology in [3], the poles within the core along with the feedback provide wideband input matching. Harmonic rejection is achieved by adding the feedforward stages $A_1$ and $A_2$ and feedback path $A_3$. These stages as well as $C_1$ and $C_2$ are digitally programmable so as to shape the LNA frequency response according to the desired signal frequency. Capacitor $C_F$ adjusts the input reactance for each setting of the digital controls, ensuring a good match.

Programmable Notch A notch whose frequency can be varied by a factor of 30 places difficult burdens on the LNA because the devices that establish a low-frequency notch may introduce parasitics that degrade the high-frequency performance. For this reason, we confine the notch-defining components to only the auxiliary paths in Fig. 1. Illustrated in Fig. 2 is the principle of notch creation. Amplifier $A_1$ incorporates three programmable zeros to remove the desired signal at $f_1$, amplify the blocker at $3f_1$, and subtract the result from the main path. This third-order high-pass filtering is necessary so as to ensure that the desired signal is heavily suppressed before reaching the summing node. Note that the noise contribution of $A_1$ at $f_1$ is minimal owing to its low gain at this frequency.

Located at $f_1$, the three zero frequencies in Fig. 2 produce some phase shift at $3f_1$, prohibiting complete cancellation. This issue is resolved by adding a programmable pole at node $X$ at a frequency of approximately $6 \times (3f_1)$ and hence compensating for the phase. The feedforward path provided by $A_1$ introduces a notch at $3f_1$ but only slightly attenuates higher frequencies. To extend the rejection bandwidth, feedforward path $A_2$ is added. This stage creates a notch at a higher frequency and, together with $A_1$, produces a more uniform rejection at $4f_1$, $5f_1$, etc.

Stages $A_1$ and $A_2$ offer heavy harmonic rejection for $f_1$ up to about 1 GHz. At higher frequencies, the parasitic poles of these stages (e.g., those at $Y$ and $Z$ in Fig. 2) alter the phase significantly, limiting the rejection level. To provide greater roll-off, a Miller capacitor $C_1$ is inserted at the input and driven by amplifier $A_3$. This amplifier unilaterizes the feedback path (to avoid an unwanted zero) and isolates the output of the first stage ($M_1$-$M_2$ in Fig. 1) from the loading presented by $C_1$. With a 50-$\Omega$ source impedance driving the LNA, the Miller capacitor can attenuate signals at 500 MHz or higher. Finally, as the parasitic poles in $A_3$ begin to manifest themselves, $C_2$ is switched in, attenuating components above 7 GHz.

Calibration The proposed harmonic-rejecting LNA readily lends itself to calibration in a direct-conversion environment. Depicted in Fig. 3, the calibration proceeds as follows. The LO is set to the desired notch frequency, $3f_1$, and a fraction of it is injected into the LNA (e.g., onto node $P$ in Fig. 1), thus generating a dc offset proportional to the LNA output amplitude in $x_P$. The quantity $x_P^2 + x_Q^2$ is computed by the baseband processor. Now, the digital tune control is stepped through its codes, and that code is sought which yields the minimum value for $x_P^2 + x_Q^2$. Such a code is hereafter used for creating the notch at $3f_1$.

Experiment Results The overall LNA has been fabricated in 65-nm CMOS technology and tested with a 1.2-V supply (die shown in Fig. 4). A serial bus carries the digital controls. The circuit consumes 8.64 mW, of which 7.56 mW is drawn by the core and the remainder by $A_1$, $A_2$, and $A_3$. The measured IIP$_3$ is $-12$ dBm.
Fig. 5 plots the measured frequency response with example of code settings, demonstrating at least 20 dB of harmonic rejection from 300 MHz to 10 GHz. Fig. 6 plots $S_{11}$ and the measured noise figure, revealing some $1/f$ noise penalty at the lower end. With harmonic rejection turned on, the NF degrades by about 1 dB.

To assess the calibration, the environment of Fig. 3 is created externally around the LNA and the time evolution of the frequency response is monitored. As illustrated in Fig. 7, the loop indeed converges, adjusting the capacitor banks such that a high harmonic rejection is obtained.

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References