Challenges in the Design of Frequency Synthesizers for Wireless Applications

Behzad Razavi
Integrated Circuits and Systems Laboratory
University of California, Los Angeles

Abstract

This paper describes the challenges in the design of frequency synthesizers used in wireless transceivers. Following a review of design issues and the effect of nonidealities, we present a number of synthesizer architectures along with their merits and drawbacks. We also describe the difficulties in the design of some of the building blocks and consider the role of synthesizers in emerging applications.

I. Introduction

The limited bandwidth available to each user in wireless systems mandates the precise definition of the carrier frequency in both the transmit and receive paths. Frequency synthesizers generate periodic signals with accurately-defined frequencies, thus serving as an integral part of RF transceivers.

Frequency synthesis continues to be a challenge, fundamentally because performing algebraic operations on frequencies is more difficult than on other electrical quantities such as voltages or currents. The challenge has taken different directions throughout the years, motivating the invention of various architectures and circuit techniques [1, 2, 3]. As RF systems incorporate higher levels of integration, frequency synthesizers must deal with additional trade-offs resulting from requirements such as monolithic implementation, low cost, minimal number of external components, and low power dissipation.

This paper describes the challenges in the design of frequency synthesizers at both architecture and circuit level. In Section II, we consider a typical synthesizer environment, review important performance parameters, and analyze the effect of nonidealities. In Section III, we describe a number of synthesizer architectures along with their merits and drawbacks, especially with respect to monolithic integration. The design of building blocks is presented in Section IV and the role of synthesizers in some of the emerging applications is discussed in Section V.

II. General Considerations

In RF transceivers, a frequency synthesizer generates the periodic signals required for both upconversion and downconversion. As shown in the generic transceiver of Fig. 1, each mixer is driven by a local oscillator (LO) that is embedded in the synthesizer because the frequency must be defined with very high accuracy —ranging from 0.1 ppm for GSM to 25 ppm for DECT. Moreover, the frequency must be varied in small, precise steps, as depicted in Table 1 for the mobile units of some cellular and cordless phone standards. Some of the considerations in such an environment are as follows.

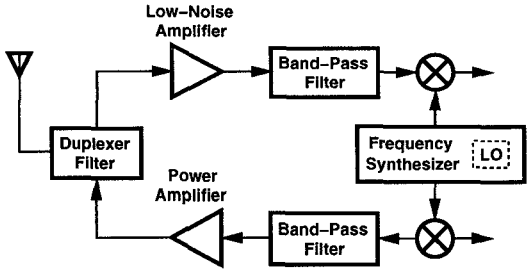

Fig. 1. Generic RF Transceiver.

	TX Band	RX Band	Channel BW
IS-54	824–849 MHz	869–894 MHz	30 kHz
IS-95	824–849 MHz	869–894 MHz	1.25 MHz
GSM	890–915 MHz	935–960 MHz	200 kHz
DECT	1.88–1.9 GHz	1.88–1.9 GHz	1.728 MHz

Table 1. Frequency bands of cellular and cordless phone standards.

A. Frequency Accuracy

While the reference frequency of synthesizers is usually derived from a crystal oscillator to achieve a high accuracy, some frequency error is inevitable, especially if temperature variation and aging of crystals are taken into account. The effect of this error in translating the spectrum of a quadrature-modulated signal is to periodically rotate the signal constellation.

The problem of frequency error further complicates the design of RF transceivers. In high-precision applications such as GSM, some means of automatic frequency control (AFC) is necessary. A possible approach is conceptually illustrated in Fig. 2. Here, during the training sequence transmitted at the beginning of the communication, the rotation frequency of the constellation is measured in the digital domain and the result is used to adjust the frequency of the crystal oscillator.

B. Phase Noise

The local oscillator used in a synthesizer exhibits finite phase noise, corrupting both the upconverted and downconverted signals [4]. As shown in Fig. 3(a), the phase noise of an interferer transmitted by a powerful, nearby station degrades the detection of a weak signal even with a noiseless

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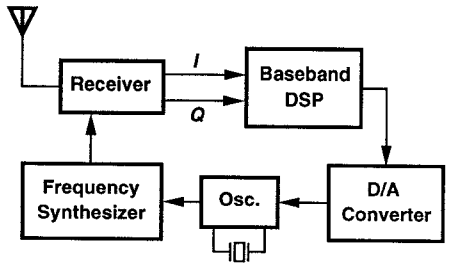

Fig. 2. AFC by feedback from DSP to oscillator.

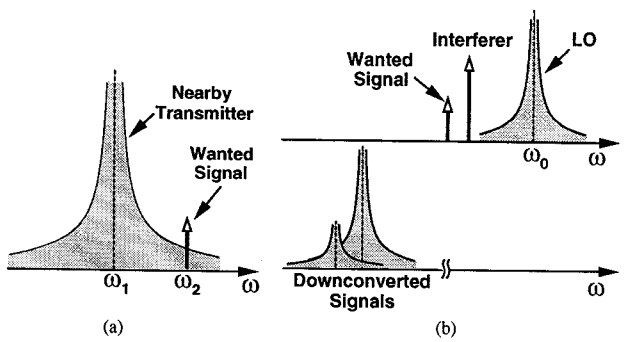

Fig. 3. Effect of phase noise in (a) a transmitter, (b) a receiver.

receiver. Moreover, if the receiver LO contains phase noise, then downconversion creates two overlapping noisy spectra, thus corrupting the wanted signal by the tail of the interferer [Fig. 3(b)]. This effect is called "reciprocal mixing."

Wireless standards impose stringent constraints on the close-in and far-out phase noise of synthesizers. For example, DECT systems require that the output phase noise remain below the mask shown in Fig. 4.

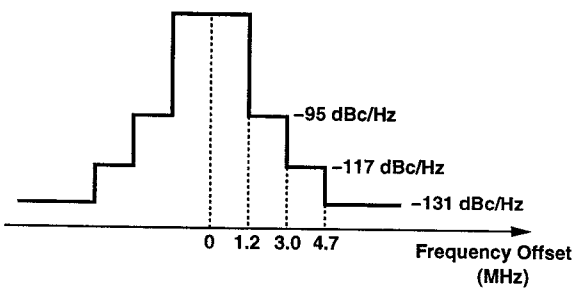

Fig. 4. DECT phase noise mask.

The issue of phase noise is perhaps the principal obstacle in fully integrating synthesizers, especially in mainstream VLSI technologies that lack high-quality inductors. We return to this point in Section IV.A.

C. Sidebands

In addition to phase noise, the output of a synthesizer may contain unwanted sidebands ("spurs"), for example those generated by the reference frequency of a phase-locked architecture (Section III.A). Shown in Fig. 5, the effect of sidebands is particularly troublesome in the receive path. Suppose the synthesizer output consists of a carrier at ω_{LO} and a spur at

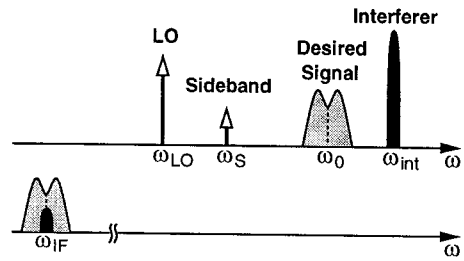

Fig. 5. Effect of synthesizer sideband in receiver.

ω_S, while the received signal is accompanied by an interferer at ω_{int}. It can be seen that two important components appear after downconversion: the desired channel convolved with the LO signal, and the interferer convolved with the sideband. If $\omega_{int} - \omega_S = \omega_{IF}$, the downconverted interferer falls in the desired channel.

Typical systems require that all sidebands be approximately 60 to 70 dB below the carrier, introducing a trade-off between sideband suppression and switching speed in phase-locked topologies (Section III.A).

D. Switching Time

When the digital input of a synthesizer commands a change in the channel, the circuit requires a finite time to establish the new output frequency. As the instantaneous value of the frequency changes, the upconverted signal in the transmitter leaks into adjacent channels, often requiring that the power amplifier be turned off until the synthesizer settles. For this reason, applications such as frequency-hopped spread-spectrum systems demand relatively fast switching.

The trade-off between the switching speed and the sideband magnitude in phase-locked topologies calls for architectural innovations so as to achieve faster channel selection.

E. Sensitivity to Noise

In a transceiver environment, a frequency synthesizer is subjected to various sources of noise, from digital baseband circuits to the transmitter power amplifier. The latter is particularly troublesome because of the enormous transient currents it draws from the supply and ground of the system. As depicted in Fig. 6, despite various shielding techniques, the

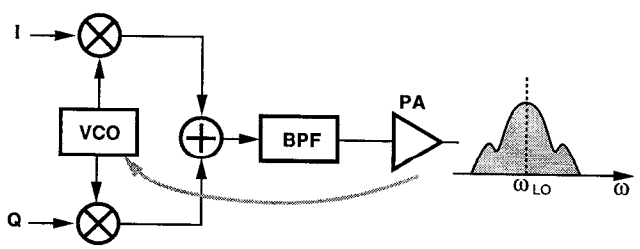

Fig. 6. VCO pulling due to PA noise.

randomly-modulated output of the PA still corrupts the synthesized signal (e.g., through "injection pulling"). Thus, the synthesizer, especially the voltage-controlled oscillator (VCO) must reject this type of disturbance. However, in practice it is difficult to achieve adequate oscillator purity in the presence

of the PA noise, unless the frequency planning ensures that the PA output spectrum is sufficiently far from the LO output frequency [5].

Another issue arises in portable systems in which the PA is periodically turned on and off to save power. With the finite output impedance of the battery, the large supply current of the PA may introduce several hundred millivolts of change in the supply voltage [6], affecting the oscillator frequency and hence giving rise to a transient in the synthesizer. A locally-generated supply devoted to the synthesizer alleviates this problem, but at the cost of complicating the design and increasing the power dissipation.

III. Synthesizer Architectures

The high accuracy required in the definition of the output frequency has made phase-locked loops (PLLs) the dominant architecture for frequency synthesis. In this section, we describe a number of synthesizer architectures.

A. Integer-N Architecture

A PLL incorporating a programmable divider in the feedback path can operate as a synthesizer. Shown in Fig. 7, the integer-N architecture follows the voltage-controlled oscilla-

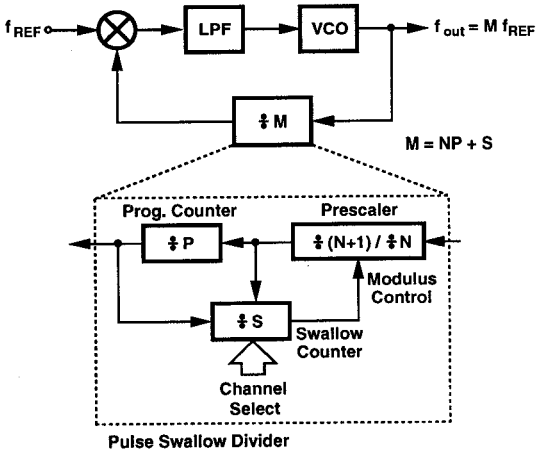

Fig. 7. Integer-N architecture.

tor (VCO) with a pulse swallow divider so as to provide an output frequency step equal to the input reference, f_{REF} [7]. The divider consists of a dual-modulus prescaler, a swallow counter, and a program counter. When the divider begins from the reset state, the prescaler divides by $N+1$ until the swallow counter overflows, changing the modulus control signal. The prescaler then divides by N until the program counter is full. Thus, for every $(N+1)S+(P-S)N = NP+S$ pulses generated by the VCO, one pulse appears at the divider output.

The simplicity of the integer-N architecture has made it a popular choice. In RF systems, the synthesizer has been traditionally partitioned into three separate chips: the VCO; the dual-modulus prescaler; and the combination of the program counter, the swallow counter, the phase/frequency detector (PFD), and the loop low-pass filter (LPF). The VCO and the prescaler have typically been designed in silicon bipolar or GaAs processes and the rest in CMOS technology. Note that a buffer must be interposed between the VCO and the prescaler to isolate the former from the kickback switching noise of the latter [8].

The integer-N architecture nevertheless suffers from a number of drawbacks. First, since the reference frequency is equal to the channel spacing, and since stability considerations limit the loop bandwidth to approximately $f_{REF}/10$, the switching time is quite long. Second, the loop cannot suppress the phase noise of the VCO for frequency offsets greater than roughly $f_{REF}/10$, an especially serious issue in MOS implementations because the upconverted $1/f$ noise of the oscillator is quite significant for offsets as large as several hundred kilohertz. Third, the periodic disturbance of the VCO control line by the charge pump creates sidebands at an offset equal to $\pm f_{REF}$, requiring further limitation of the LPF bandwidth so that the magnitude of these sidebands is sufficiently small. Fourth, the dual-modulus prescaler may appear as the speed bottleneck of the system because its maximum operation frequency is about half that of a simple divide-by-two circuit (Section IV.B).

B. Fractional-N Architecture

In integer-N synthesizers, the loop bandwidth is limited because the input reference frequency must be equal to the channel spacing, a property resulting from the fact that the output frequency changes by only *integer* multiples of f_{REF}. In fractional-N loops, on the other hand, the output frequency can vary by a *fraction* of f_{REF}, allowing the latter to be much greater than the channel spacing.

Illustrated in Fig. 8, a fractional-N topology incorporates a "pulse remover," a circuit that blocks one of the input pulses

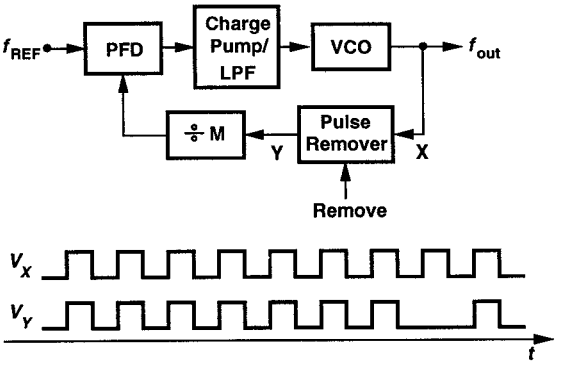

Fig. 8. Fractional-N architecture.

upon assertion of the remove command [1]. Since under locked condition the two frequencies presented to the phase detector must be equal, the average output frequency of the pulse remover equals f_{REF} and hence $f_{out} = Mf_{REF}+1/T_P$, where T_P is the period with which the remove command is applied. In practice, the pulse remover is merged with the divider. For example, if the VCO output is divided by M for some time and by $M+1$ for some other time, the average divide ratio can be set between M and $M+1$ (Fig. 9). With f_{REF} in the range of tens of megahertz, the loop bandwidth can be as large as a few megahertz, yielding a fast lock transient as well

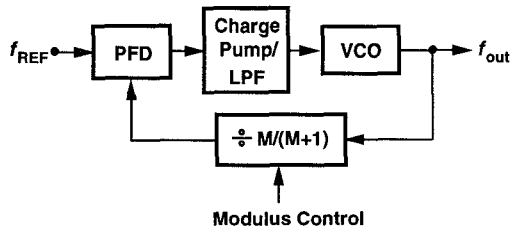

Fig. 9. Use of a dual-modulus prescaler as pulse remover.

as suppressing the VCO close-in phase noise.

The principal drawback of fractional-N loops is the existence of "fractional spurs" at the output [1]. Since each period of f_{out}/M must be slightly shorter than the reference period, the phase difference between the reference and the feedback signal grows in every period until it falls to zero when one pulse is removed. Thus, the charge pump produces increasingly wider current pulses, periodically varying the oscillator control voltage and creating spurs at $1/T_P$ with respect to the carrier.

Fractional-N spurs can be suppressed by predicting the charge packet generated by the charge pump and injecting an equal and opposite packet so as to minimize the disturbance on the oscillator control line [1]. However, device mismatches limit the accuracy of this cancellation, often requiring external adjustment [9].

Another approach is to randomize the choice of the modulus in Fig. 8 such that the *average* divide ratio is still equal to the desired value but individual division factors occur only for short periods of time. This technique in effect converts the systematic fractional sidebands to random noise. The idea can be taken one step further by *shaping* the resulting noise spectrum such that most of its energy appears at large offset frequencies [10]. Thus, noise in the vicinity of the divided carrier frequency is small and noise at higher offsets is suppressed by the low-pass filter following the PFD.

The noise shaping function can be realized by means of a $\Sigma\Delta$ modulator [10]. Depicted in Fig. 10, the modulator generates a binary stream representing a well-defined average

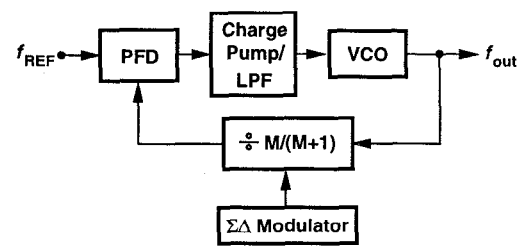

Fig. 10. Use of a $\Sigma\Delta$ modulator to shape the noise due to modulus randomization.

value accompanied by quantization noise. The spectrum of the phase noise in the feedback signal can then be expressed as

$$S_\phi(f) \propto \frac{|Q(f)|^2}{f^2}, \qquad (1)$$

where $Q(f)$ is the (voltage) noise-shaping function provided by the modulator.

While relatively complex, noise-shaping fractional-N loops are an interesting alternative whose properties merit further study. In particular, the stability and lock behavior and the existence of tones in the output of the modulator need to be investigated.

C. Dual-Loop Architectures

The relationship between the channel spacing and the reference frequency of integer-N synthesizers can be altered by employing two or more loops. A simple approach to generating fine frequency steps is to *add* a variable, low frequency to a fixed, high frequency. Depicted in Fig. 11, this technique utilizes PLL_1 to generate the carrier frequency, and PLL_2 to

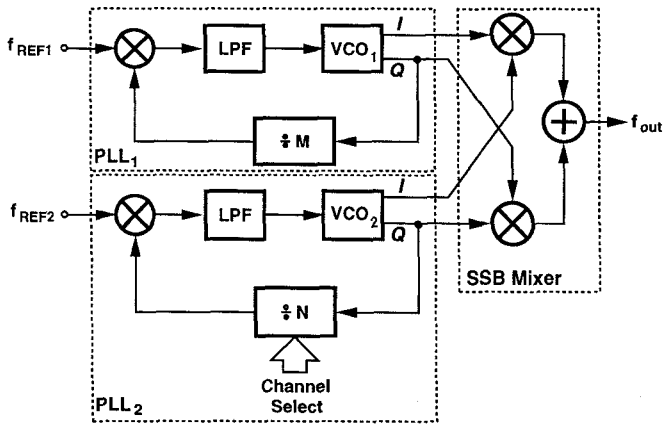

Fig. 11. Dual-loop architecture.

produce increments equal to f_{REF2}. Varying the divide ratio of PLL_2 therefore yields the fine steps required in the output frequency. The addition of the two frequencies is performed by a single-sideband (SSB) mixer.

The principal advantage of this architecture over single-loop integer-N topologies is that the loop bandwidth of PLL_1 can be chosen to be large so as to reduce the close-in phase noise of VCO_1. The phase noise of VCO_2 is much lower because of the trade-off with the center frequency [11, 4]. The major drawback is that accurate single-sideband mixing requires precise generation of quadrature phases in both PLLs, low harmonic distortion in either VCO_1 or VCO_2, and sufficiently small mismatches in the two mixers [12]. Thus, it is difficult to ensure that sidebands resulting from mismatches and nonlinearities are 60 to 70 dB below the carrier.

The above issues can be alleviated as shown in Fig. 12. Here, the SSB mixer is designed to *subtract* the two frequencies and it is placed *inside* the feedback loop. Furthermore, f_2 has a large offset: $f_2 = f_0 + kf_{REF2}$, where f_0 is a fixed value, e.g., 25 MHz. Thus, $f_{out} = Nf_{REF1} + f_0 + kf_{REF2}$. The key point here is that the sidebands resulting from mismatches and harmonics are at relatively large frequency offsets and hence are suppressed by the loop low-pass filter. In addition, if the sidebands at the output of the synthesizer fall outside of the band of interest, their magnitude is allowed to be higher than in-band spurs because the transceiver front-end duplexer (or band-pass filter) attenuates out-of-band interferers, making the effect illustrated in Fig. 5 less significant.

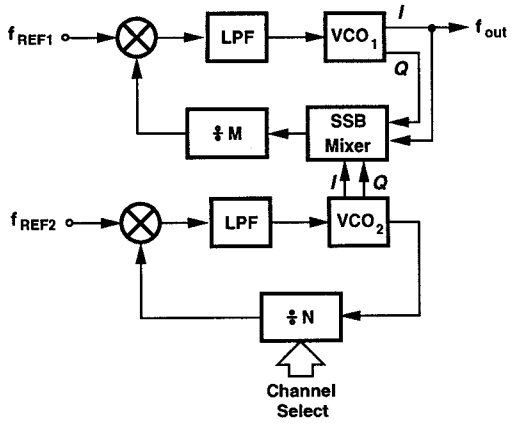

Fig. 12. Dual-loop architecture with SSB mixer in one loop.

Another dual-loop architecture is depicted in Fig. 13. Two PLLs generate outputs at $f_1 = f_0 + kf_{REF1}$ and $f_2 = f_0 -$

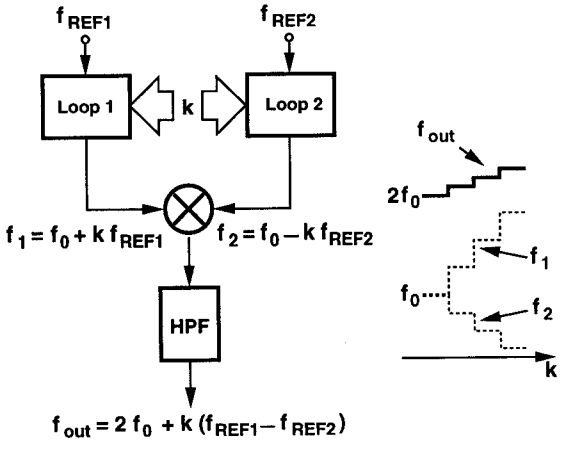

Fig. 13. Dual-loop architecture using vernier effect.

kf_{REF2}, respectively. These outputs are mixed and the result is high-pass filtered to yield: $f_{out} = 2f_0 + k(f_{REF1} - f_{REF2})$. Thus, f_{out} can increment in steps equal to $f_{REF1} - f_{REF2}$ while f_1 and f_2 increment in much greater steps, allowing a relatively large loop bandwidth in both PLLs. For example, if $f_0 = 450$ MHz, $f_{REF1} = 1$ MHz, and $f_{REF2} = 1.2$ MHz, we have $f_{out} = 900$ MHz $- k \times 200$ kHz. Another advantage of this architecture is that the dual-modulus divider required in each loop operates at approximately half the output frequency.

The primary difficulty in the architecture of Fig. 13 is that the mixer generates cross products of the harmonics of f_1 and f_2, restricting the choice of f_0, f_{REF1}, and f_{REF2} if the spurs are to fall outside the desired band. In some cases, a solution may not even exist.

In the dual-loop configurations considered above, the two oscillators may "pull" each other through the parasitic paths in the mixer. For this reason, each oscillator must be followed by a buffer with high reverse isolation.

D. Direct Digital Synthesis

Direct sigital synthesis (DDS) produces the signal in the digital domain and utilizes digital-to-analog conversion and filtering to reconstruct the waveform in the analog domain. Illustrated in Fig. 14, DDS employs an accumulator, a look-

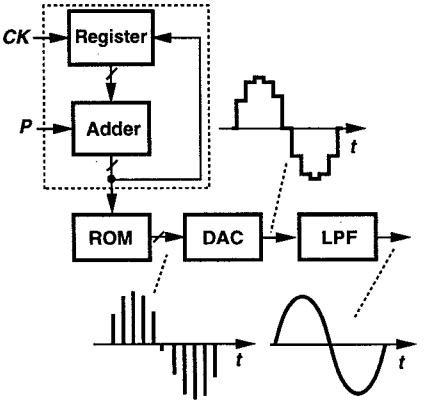

Fig. 14. Direct digital synthesis.

up read-only memory (ROM), a digital-to-analog converter (DAC), and a low-pass filter [2]. The accumulator generates a digital ramp that is mapped to a sinusoid by the ROM. As the increment value, P, increases, so does the rate at which the accumulator overflows, thus yielding a shorter period for the output sinusoid.

DDS offers a number of advantages over phase-locked architectures: much less phase noise, fine frequency steps, much faster channel switching, and provision for direct modulation. However, speed issues have limited the use of DDS in the RF range. Since the clock frequency is typically about three to four times the maximum output frequency so as to relax the LPF rejection requirements, for a 900-MHz signal, the circuit of Fig. 14 would need to be clocked at a rate between 2.7 GHz and 3.6 GHz. In today's VLSI technologies, it is difficult to perform the operations shown in Fig. 14 at such speeds, especially if power dissipation is critical. Even if the digital section can be realized with acceptable complexity and power drain, the DAC remains the speed bottleneck. The trade-offs among settling time, harmonic distortion, spurious response, and power dissipation of the DAC prevent its use in the RF range.

The low phase noise and fast switching of DDS make it attractive for use as the low-frequency generator in the dual-loop architectures of Figs. 11 and 12, replacing the slower PLL (Fig. 15). In such an approach, however, two issues must

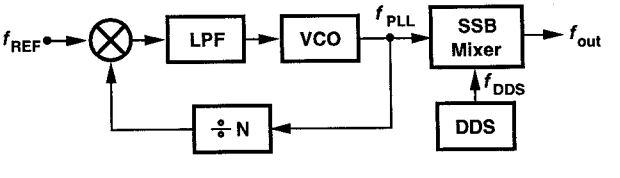

Fig. 15. Combination of phase-locking and DDS.

be considered. First, if the high-frequency VCO is on the same chip as the DDS circuit, then the substrate and supply noise produced by the accumulator and the ROM may significantly corrupt the VCO output. Second, if the dual-loop architectures require a wide tuning range in the low-frequency generator, e.g., a factor of two to one, then the DDS output LPF must have

a tunable cut-off frequency to suppress the aliased components while maintaining a constant fundamental amplitude.

IV. Building Blocks

A. VCOs

VCOs are perhaps the most critical building block of RF synthesizers. Difficult issues such as phase noise, tuning range, power dissipation, and sensitivity to supply and substrate noise have motivated a great deal of research on VCO design.

The stringent phase noise requirements in wireless systems usually lead to three general rules originating from Leeson's equation [11, 4]:

$$\text{Relative Phase Noise} = \frac{1}{4Q^2}\left(\frac{\Delta\omega}{\omega_0}\right)^2 \frac{P_{\text{noise}}}{P_{\text{carrier}}}, \qquad (2)$$

where Q is the open-loop quality factor, $\Delta\omega$ is the frequency offset, ω_0 is the center frequency, and P_{noise} is the spectral density of each source of noise. The three rules are: (1) use high-Q passive resonators; (2) minimize the number of active (and lossy passive) devices in the oscillation path; (3) maximize the oscillation swing (P_{carrier}). Through these rules, we can understand the challenges in VCO design.

Rules number 1 and 2 have made topologies such as ring oscillators and relaxation oscillators less attractive for RF applications. Despite their wide tuning range, these circuits exhibit an open-loop Q in the vicinity of unity [4] while containing many noisy devices in the oscillation path. Thus, RF oscillators have predominantly incorporated surface acoustic wave (SAW) devices, transmission lines, or LC tanks, along with one or two transistors.

In monolithic implementations, on the other hand, inductors and varactors suffer from a low Q. As shown in Fig. 16, the Q of inductors is limited by three mechanisms: metal line

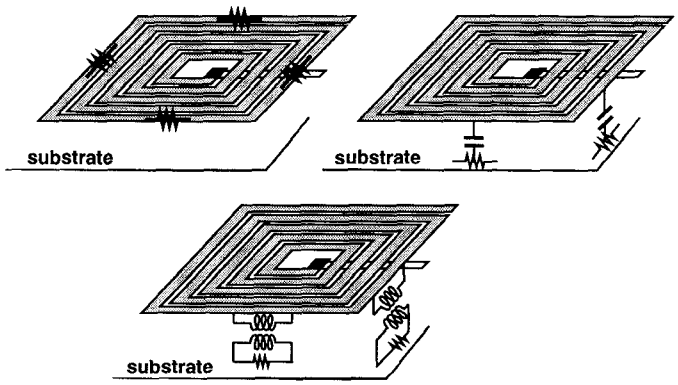

Fig. 16. Loss mechanisms in monolithic inductors.

resistivity, capacitive coupling to the substrate, and magnetic coupling to the substrate. Manifesting themselves at high frequencies, the last two effects are much more pronounced in silicon technologies with heavily-doped substrates, yielding a general variation of Q as plotted in Fig. 17.

The effect of metal line resistance can be lowered by removing the first few internal turns of a spiral inductor because the small area and large (negative) mutual coupling of these

Fig. 17. Degradation of Q due to substrate loss.

turns make their contribution to the total inductance negligible. Also, the substrate loss due to capacitive coupling can be reduced by placing under the spiral a conductive plate (e.g., n-well) that is periodically broken in the direction perpendicular to the current flow (Fig. 18). Unfortunately, the magnetically-

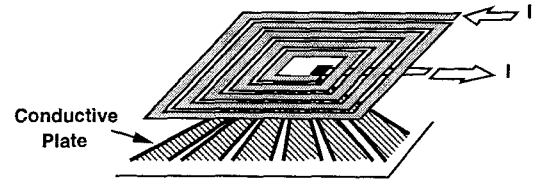

Fig. 18. Suppression of capacitively-coupled currents in the substrate.

induced current would still flow through the substrate. The Q of inductors in today's mainstream bulk CMOS technologies rarely exceeds five.

The series resistance of varactors is also of concern. In CMOS technology, grounded and floating diodes can be realized as shown in Fig. 19, with significant resistance arising from the p-substrate or the n-well. The resistance can be low-

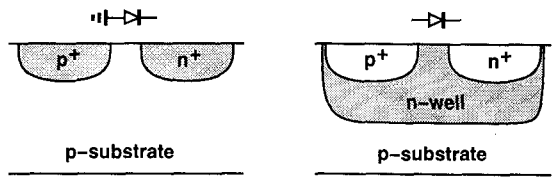

Fig. 19. Varactor structures in CMOS technology.

ered by the strapping method depicted in Fig. 20 [13].

Another important phenomenon in CMOS oscillators is the upconversion of $1/f$ noise. Since in typical submicron CMOS devices the $1/f$ noise corner may be as high as 1 MHz, oscillator phase noise at small frequency offsets is dominated by this type of noise.

LC VCOs also suffer from a trade-off between the phase noise and the tuning range, especially at low supply voltages. To lower the relative phase noise at a given power dissipation, it is desirable to increase the value of the inductor. This is because the equivalent parallel resistance of an inductor can be expressed as $R_P \approx (L\omega)^2/R_S$, where R_S is the series resistance; although L and R_S scale proportionally, R_P still increases linearly with L [13]. The upper bound on the value of L is of course determined by its self-resonance frequency, f_{SR}. Considering the substantial parasitic capacitance of the inductor and the transistor(s), we note that the *variable* component of the tank capacitance is quite small, e.g., about 30% in [13]. At low supply voltages and with large oscillation voltage swings, this component cannot be varied by more than roughly 50%, giving a tuning range of approximately 10%. Even with

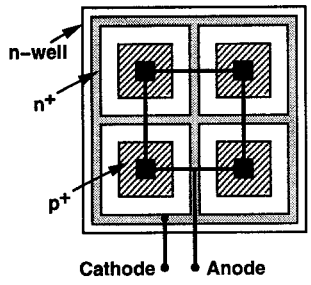

Fig. 20. Strapping n-well to reduce the series resistance.

the aid of additional circuit techniques [13], the tuning range is still quite limited.

The narrow tuning range of LC oscillators has been viewed as both a merit and a drawback! On the one hand, since the VCO "gain" is relatively low, the effect of noise on the control line is small. On the other hand, additional means of adjusting the frequency are required to ensure operation in the band of interest despite manufacturing variations. In many RF systems, this is accomplished by adding a small, mechanically trimmable capacitor in parallel with the varactor, but the tuning range must still be wide enough to cover variations with the temperature.

The second rule mentioned above makes one-transistor oscillator topologies such as the Colpitts configuration of Fig. 21(a) attractive. In this circuit, the voltage divider consisting

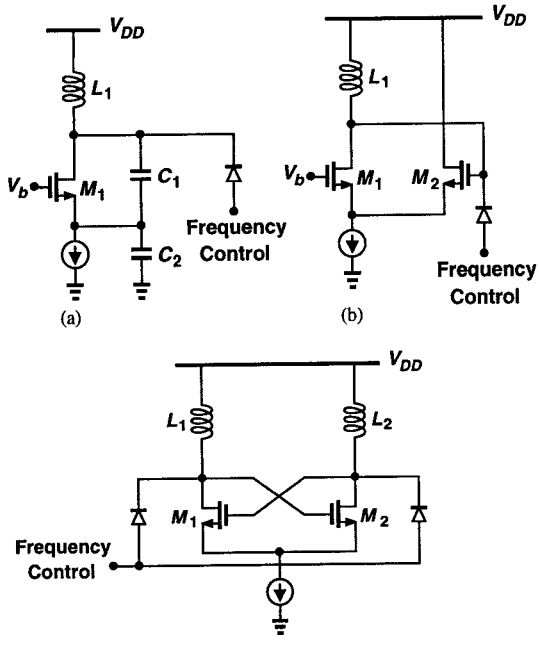

Fig. 21. (a) Colpitts oscillator, (b) use of source follower for impedance tranformation, (c) differential negative-G_m oscillator.

of C_1 and C_2 transforms the resistance seen looking into the source of M_1 [$\approx 1/(g_{m1} + g_{mb1})$] to a higher value, thereby minimizing resistive loading of the tank. As shown in Fig. 21(b), this transformation can alternatively be performed by means of a source follower, leading to a negative-G_m oscillator. With on-chip inductors, a fully differential configuration [Fig. 21(c)] proves extremely useful in driving mixers and single-sideband modulators.

The relatively high phase noise and limited tuning range of monolithic LC oscillators appear to be difficult problems, calling for solutions through synthesizer architecture innovations.

B. Frequency Dividers

Single-modulus and multi-modulus dividers are widely used in RF transceivers. Simple divide-by-two circuits can generate quadrature phases that are required in I/Q upconversion and downconversion. For this purpose, a master-slave D-flipflop employing a current-steering latch can be used (Fig. 22). Proper sizing of M_1-M_4 yields speeds in excess of 2 GHz in

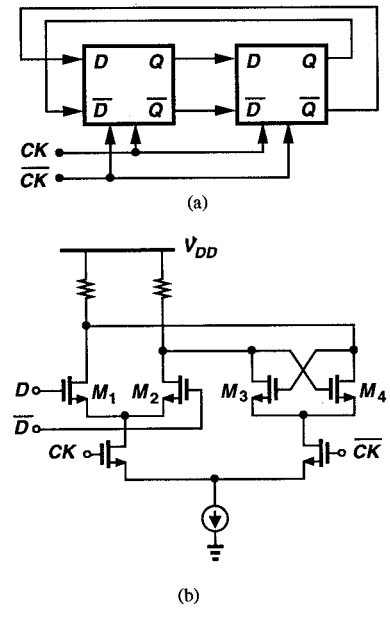

Fig. 22. (a) Divide-by-two circuit, (b) implementation of each latch.

0.6-μm CMOS technology even if each latch is loaded with an output differential pair. Simulations and experiments indicate that this configuration achieves a higher speed than dividers incorporating the true-single-phase-clocking technique [14].

An intriguing divide-by-two circuit is the "analog" divider proposed by Miller [15]. Illustrated in Fig. 23, the circuit incorporates a mixer and a low-pass filter with a cut-off fre-

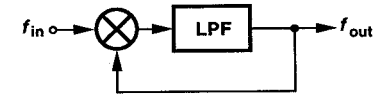

Fig. 23. Miller divider.

quency equal to $f_{in}/2$. Upon multiplication of the input and output signals, the mixer generates components at $f_{in} + f_{out}$ and $f_{in} - f_{out}$, with the former being suppressed by the filter. Thus, $f_{in} - f_{out} = f_{out}$ and hence $f_{out} = f_{in}/2$. Owing to the simplicity of the feedback loop, this topology operates at speeds even greater than half of the f_T of the transistors [16].

The Miller divider, however, is known to suffer from substantial phase noise. A possible explanation is as follows. Suppose a noise component at $f_{in}/2 + \Delta f$ appears in the feed-

back path. Multiplication of this component by the input and low-pass filtering yield the *image* frequency, $f_{in}/2 - \Delta f$, at the output. Now if this component goes around the loop, the original frequency, $f_{in}/2 + \Delta f$, is generated. In other words, the loop circulates noise components at $f_{in}/2 \pm \Delta f$ with negligible attenuation if Δf is small, a behavior similar to that of ring oscillators.

Dual-modulus dividers entail more design difficulties than divide-by-two circuits. As shown in the $\div 2/3$ circuit of Fig. 24, the critical signal path consists of the gate G_1 and the

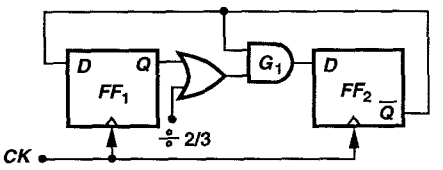

Fig. 24. Dual-modulus 2/3 divider.

input stage of FF_2. Furthermore, the output of FF_2 must drive the input capacitance of both G_1 and FF_1. For these reasons, dual-modulus dividers used in frequency synthesizers typically exhibit a maximum speed roughly half that of $\div 2$ circuits.

The limited speed of CMOS dual-modulus dividers present an important challenge to the design of multi-gigahertz synthesizers, demanding new circuit and architecture techniques.

V. Emerging Applications

A. Dual-Standard Transceivers

The existence of various wireless standards within the US and around the world has created a demand for transceivers that can operate in more than one mode. In the simplest case, two different receive and transmit frequency bands must be supported while other properties of the system remain unchanged. For example, GSM and DCS1800 differ by primarily their frequency bands. In a more sophisticated scenario, the transceiver can operate with two vastly different standards, e.g., IS-54 and IS-95.

Even in the simple case of GSM and DCS1800, the frequency planning of the transceiver is quite difficult. The need for two receive bands and two transmit bands raises a number of questions: How many VCOs and synthesizer loops are required? How should the frequencies be chosen so that harmonics and intermodulation products fall out of the band of interest or below an acceptably low level? How many stages of upconversion and downconversion are needed?

Answering these questions requires that the receive and transmit paths be designed in conjunction with the frequency synthesizer(s).

B. Multi-Gigahertz Transceivers

The availability of spectrum at higher frequencies, e.g., around 2.4 GHz and 5.5 GHz, has heightened the interest in many new standards for applications such as wireless local area networks (WLANs). An example is the high-performance radio local area network (HIPERLAN), which is expected to operate in the vicinity of 5.2 GHz.

While initial studies indicate that sub-half-micron CMOS technologies may provide a reasonable performance in the receive and transmit paths of a HIPERLAN system, the problem of frequency synthesis persists. The substrate loss at 5 GHz may limit the Q of inductors to less than unity. Furthermore, even simple divide-by-two circuits may not operate reliably at these frequencies. In this case, too, the transceiver architecture and frequency planning must be chosen according to the frequency synthesis capabilities of the technology.

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