TA 9.7 A 622Mb/s 4.5pA/√Hz CMOS Transimpedance Amplifier*

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High-speed transimpedance amplifiers (TIAs) used at the front end of optical fiber receivers present design challenges in the form of trade-offs between input noise current, speed, transimpedance gain, power dissipation, and supply voltage. This transimpedance amplifier in 0.6μm CMOS exhibits 4.5pA/√Hz average input noise current, 622Mb/s data rate, and 8.7kΩ transimpedance gain while dissipating 30mW from a 3V supply.

Two TIA topologies are shown in Figures 9.7.1a and b. The common-gate stage provides a broad band but a relatively high input noise current because the noise currents due to R_D and M_2 are directly referred to the input [1]. Since the dc voltage drop across R_D must be maximized to minimize its noise current and achieve a high gain, the allowable headroom for M_2 is limited, making its noise contribution significant. Note that for large transistors and/or a large photodiode capacitance, C_D , the noise contributed by M_1 rises at high frequencies.

The topology of Figure 9.7.1b is more commonly used because R_F does not carry a large bias current and hence its value can be maximized. However, the circuit suffers from three drawbacks. First, the feedback resistor along with the input capacitance of M_1 (which is usually a wide device) and C_D creates a pole at the input, degrading the stability and pulse response [2]. This is a serious issue because the circuit contains two other poles at the drain of M_1 and source of M_2. Second, the open-loop gain is limited at low supply voltages because the drop across R_D cannot exceed V_{DD}-V_{GS2}-V_{GS1}. Owing to this headroom limitation, R_D and M_2 may also contribute substantial noise. Third, the gate-referred noise voltage of M_1, $V_{n,M1}$, results in an input noise current equal to $V_{n,M1}/R_F$. Thus, with typical speed, headroom, and power constraints, M_1 may contribute as much input noise current as R_F does.

The TIA reported here is based on the topology depicted in Figure 9.7.1c, where C_1 senses the voltage across C_2 and returns a proportional current to the input. Here, if $A_1 >>1$, then $I_{out}/I_{in} \approx 1+C_2/C_1$, suggesting that the circuit can operate as a current amplifier and, with a resistor R_{D2} tied to the drain of M_2, it provides a transimpedance of $(1+C_2/C_1)R_{D2}$. The closed-loop 3dB bandwidth of the circuit is equal to $(1+A_1)g_{m2}/(2\pi C_2)$. For fair comparison of Figure 9.7.1b and 9.7.1c, it is assumed that (1) both circuits have the same gain, e.g., $R_F=(1+C_2/C_1)R_{D2}$ and (2) $V_{n,M1}=V_{n,A1}$.

The topology of Figure 9.7.1c has three advantages over that in Figure 9.7.1b. First, the gain definition network (C_1 and C_2) contributes no noise. Second, the capacitance seen at the input node to ground simply lowers the dc loop gain rather than degrade the stability. Third, the input-referred noise voltage of the first stage, A1, results in an input noise current of $I_{n,A1}=V_{n,A1}C_2s/(1+C_2/C_1)$. By contrast, if in Figure 9.7.1b, R_F is chosen equal to $(1+C_2/C_1)R_{D2}$, then the input noise current due to M_1 is $I_{n,M1}=V_{n,M1}/[(1+C_2/C_1)R_{D2}]$.Thus, $I_{n,A1}$ remains below $I_{n,M1}$ for $|C_2s|<R_{D2}^{-1}$. In this design, C_2=0.5 pF and R_{D2}=500Ω, suggesting that $I_{n,A1}$ exceeds $I_{n,M1}$ only for frequencies above 640MHz. The total noise current contributed by A_1 in this band is lower than that due to M_1 in Figure 9.7.1b by a factor of 3.

In Figure 9.7.1c, the noise of M_2 and I_{SS} is also of concern. If represented as a voltage source in series with the gate, this noise can be simply divided by A_1 and treated as part of the noise of A_1. Therefore, with proper design the contribution of M_2 is made negligible. It can also be shown that the noise of I_{SS} in Figure 9.7.1c directly adds to the noise current of R_{D2}, a behavior similar to that of the common-gate stage in Figure 9.7.1a.

The foregoing observations indicate that the topology of Figure 9.7.1c has significant advantages over the common-gate circuit of Figure 9.7.1a as well. First, in Figure 9.7.1a, R_D and M_2 directly contribute noise whereas in Figure 9.7.1c the noise current of R_{D2} and I_{SS} is divided by $(1+C_2/C_1)$. Second, the transimpedance gain is equal to R_D in Figure 9.7.1a but $(1+C_2/C_1)R_{D2}$ in Figure 9.7.1c.

Figure 9.7.2a illustrates implementation of the amplifier core. To maximize open-loop gain and minimize noise contributed by R_{D1}, the voltage drop across R_{D1} must be maximum, prohibiting direct coupling to the following stage. Transistor M_3 is biased with a large gate-source voltage ($V_b \approx 0$) to minimize its noise contribution while providing half of the drain current of M_1. The core is followed by another gain stage and an output buffer to drive a 50Ω load. Since the output driver incorporates a large device (200μm/0.6μm), a 15nH on-chip inductor added to the second stage extends the bandwidth with negligible phase distortion.

The lower end of the amplifier bandwidth is critical because it determines how much of the energy of the random binary signal is removed and how much intersymbol interference (ISI) is generated. Simulations indicate that binary data experiences an eye closure of 0.44dB if the low-end cut-off frequency of a 622Mb/s amplifier is 50kHz. Such a low cut-off frequency requires resistors on the order of 2MΩ connected to the gates of M_1 and M_2 in Figure 9.7.2a with minimal parasitic capacitances. Figure 9.7.2b shows the input bias network. Here, I_1 and M_7 define the on-resistance of M_5, and M_6 and M_1 constitute a current mirror. If $(W/L)_7$=100x(1.5μm/4μm) and $(W/L)_5$=1.5μm/4μm, then $R_{on5}=100g_{m7}^{-1}$ (with negligible mismatches between M_5 and M_7). The bias current of M_7 is chosen so $g_{m7}^{-1} \approx 15k\Omega$. Since the 1.5x4μm² channel yields a threshold mismatch <10mV, the gate-source overdrive voltage (V_{GS}-V_{TH}) of M_5 and M_6 is ~100mV to minimize uncertainty in R_{on5}[3]. A similar network biases the gate of M_2 in Figure 9.7.2a.

Since the current produced by the photodiode contains a significant dc component, the circuit may require a pMOS current source connected to the gate of M_1 and controlled by the drain voltage of M_1 through a low-pass filter. The filter would incorporate a network similar to that in Figure 9.7.2b to achieve a low cut-off frequency.

Testing and characterization of TIAs using standard instrumentation is difficult. Driving the circuit by a 50Ω source overestimates the bandwidth and applying the output of a photodiode does not easily allow calculation of the gain and transfer function. It is possible to utilize a large on-chip resistor to approximate a current source [2]. As shown in Figure 9.7.3, this design precedes the TIA by a voltage-to-current converter (VIC) realized as an nMOS transistor, M_{in1}. Transistor M_{in2} is identical to M_{in1} and provides a means of monitoring the current applied to the TIA. With a 10% mismatch between the bias currents of M_{in1} and M_{in2}, their transconductance mismatch remains <5%. This setup does not require precise knowledge of the input voltage level.

The TIA is fabricated in a 0.6μm CMOS technology and tested with a 3V supply. Figure 9.7.4 shows the 400x500μm² die. The circuit (excluding the output transistor) consumes 30mW.

Figure 9.7.5 plots the composite gain of the VIC and TIA as a function of frequency, indicating 550MHz 3dB bandwidth. With the aid of the monitoring output, the gain of the TIA is obtained to be equal to 8.7kΩ, close to the simulated value. The low end of the band is manually measured to be 40kHz.

*This work was supported by Cypress Semiconductor.

Noise measurements are illustrated in Figure 9.7.3. An external amplifier (EA), following the TIA, raises the output noise level to approximately 15dB above the noise floor of the spectrum analyzer. The measurement proceeds in two steps. First, the equivalent transimpedance of the TIA/EA cascade is calculated at each frequency. This is necessary because the external amplifier suffers from nearly 5dB passband ripple. Next, the input VIC is tuned off and the TIA noise is amplified and displayed on the spectrum analyzer. Figure 9.7.6 shows the noise across a 1GHz bandwidth with 1MHz resolution bandwidth. (Noise near 100MHz is attributed to an FM radio station.) Using the definition in Reference [2] yields an average input noise current of 4.5pA/√Hz, about twice that predicted by simulation using a MOS excess noise coefficient of 2/3.

Figure 9.7.7 compares performance of this design with that of the TIAs reported in References [2] and [4].

References:

[1] Razavi, B., Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2000.

[2] Taylor, S. S. and T. P. Thomas, "A 2pA/√Hz 622Mb/s GaAs MESFET Transimpedance Amplifier," ISSCC Dig. Tech. Papers, pp. 254-255, Feb. 1994 (also the slide supplement).

[3] Pelgrom, M. J. M., H. P. Tuinhout, and M. Vertregt,"Transistor Matching in Analog CMOS Applications," IEDM Dig. of Tech. Papers, pp. 34.1.1-34.1.4, Dec. 1998.

[4] Mohan, S. S. and T. H. Lee, "A 2.125Gbaud 1.6kΩ Transimpedance Preamplifier in 0.5μm CMOS," Proc. CICC, pp. 513-516, May 1999.

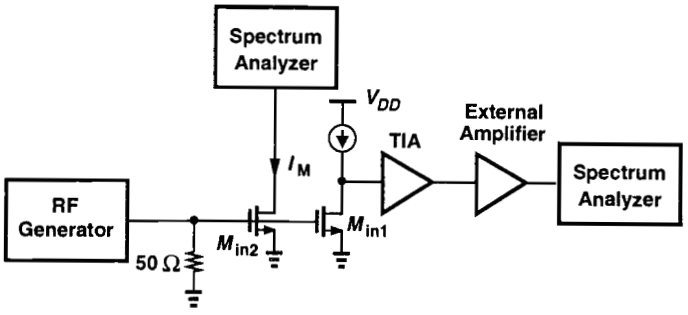

Figure 9.7.3: Addition of VIC and monitor device to front end.

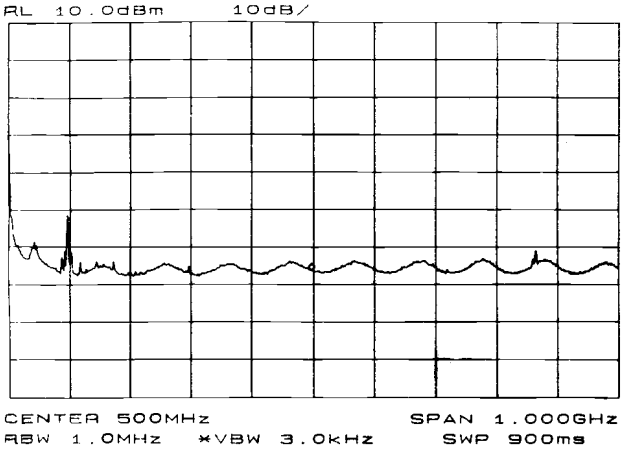

Figure 9.7.6: Measured output noise.

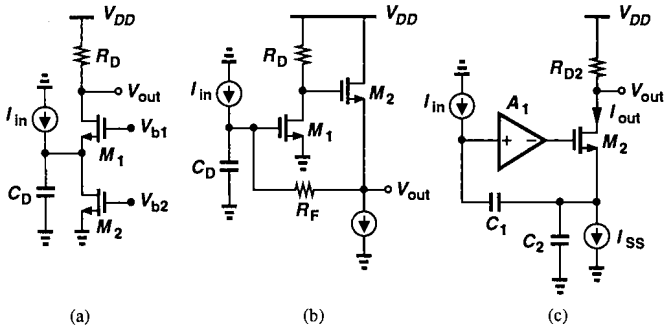

Figure 9.7.1: (a) CG TIA, (b) TIA with resistive feedback, (c) TIA with capacitive network.

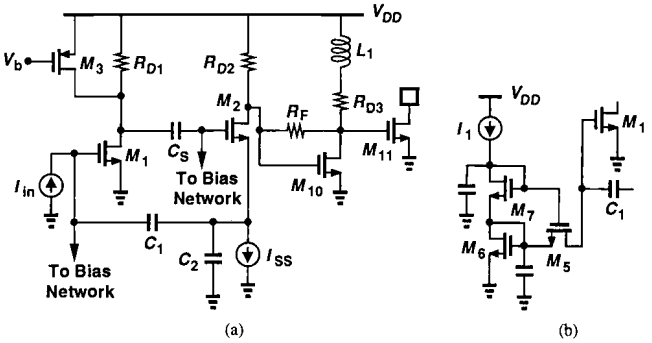

Figure 9.7.2: (a) Overall TIA implementation, (b) bias network.

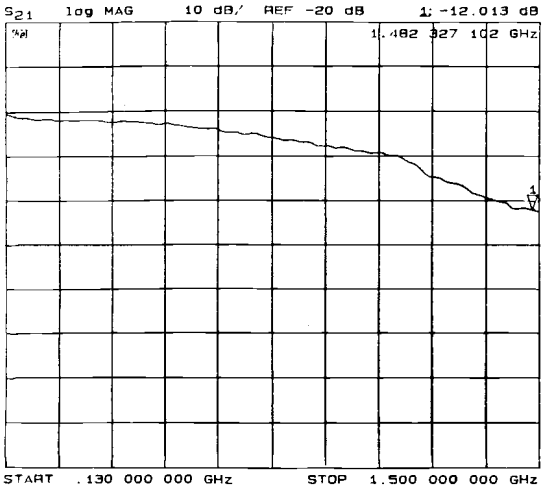

Figure 9.7.5: Measured frequency response.

	Design in [2]	Design in [4]	This Work
Gain (With 50-Ω load)	6.8 kΩ	1.6 kΩ	8.7 kΩ
Average Input Noise	2 pA/√Hz	17.3 pA/√Hz (simulated result)*	4.5 pA/√Hz
Bandwidth	500 MHz	1.2 GHz	550 MHz
Supply Voltage	±5 V	NA	3 V
Power Dissipation (excluding output buffer)	100 mW	115 mW	30 mW
Technology	12-GHz GaAs MESFET	0.5-um CMOS	0.6-um CMOS

*The paper specifies a total simulated noise of 0.6 uA. With a bandwidth of 1.2 GHz, the noise density is equal to17.3 pA/√Hz.

Figure 9.7.7: Performance of several TIAs.

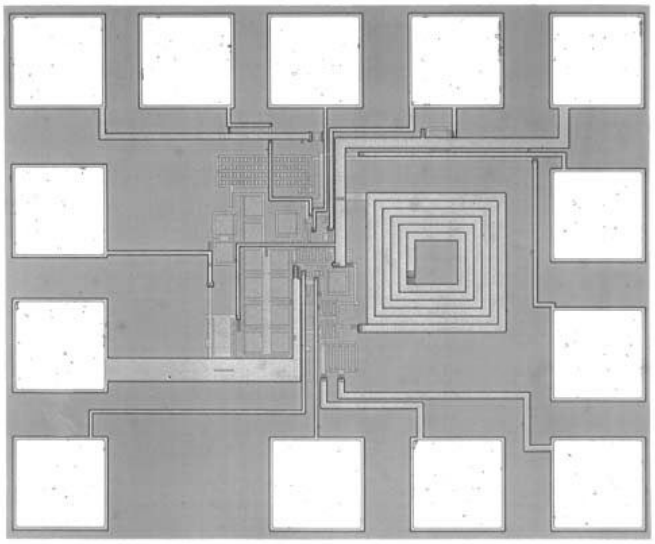

Figure 9.7.4: Die micrograph.

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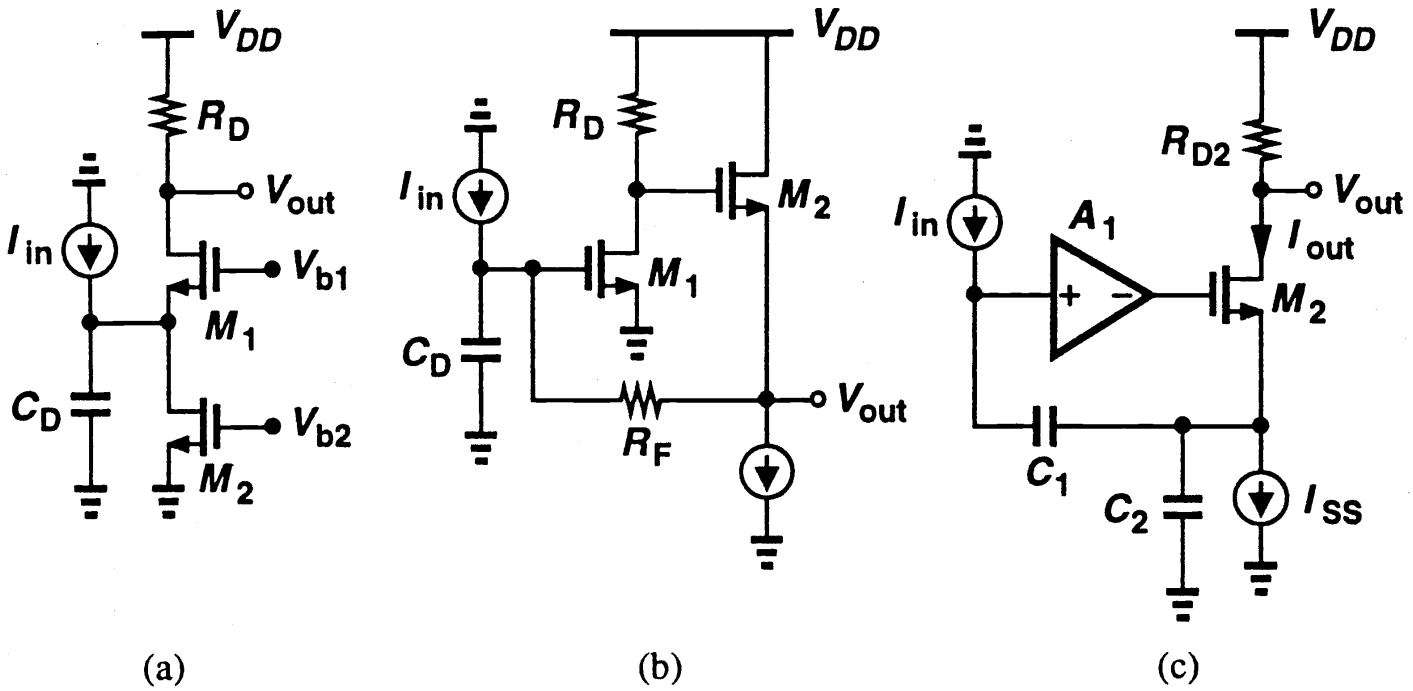

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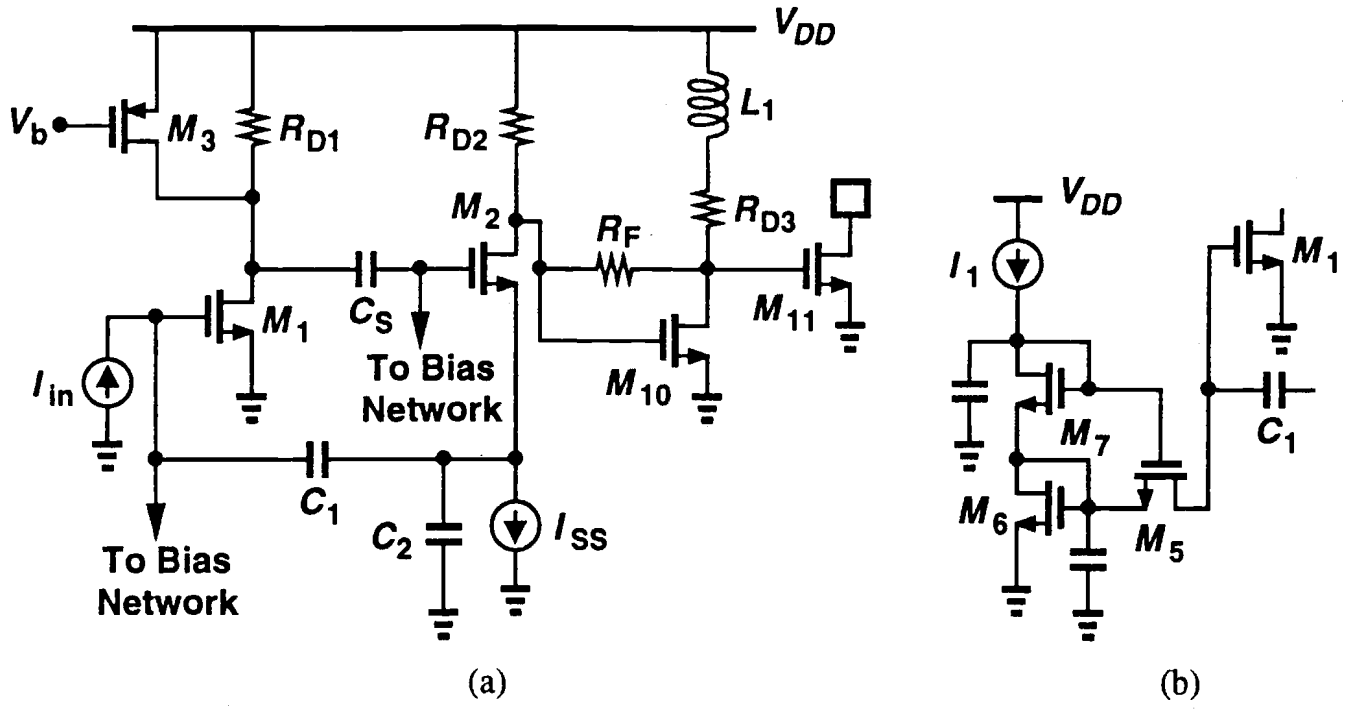

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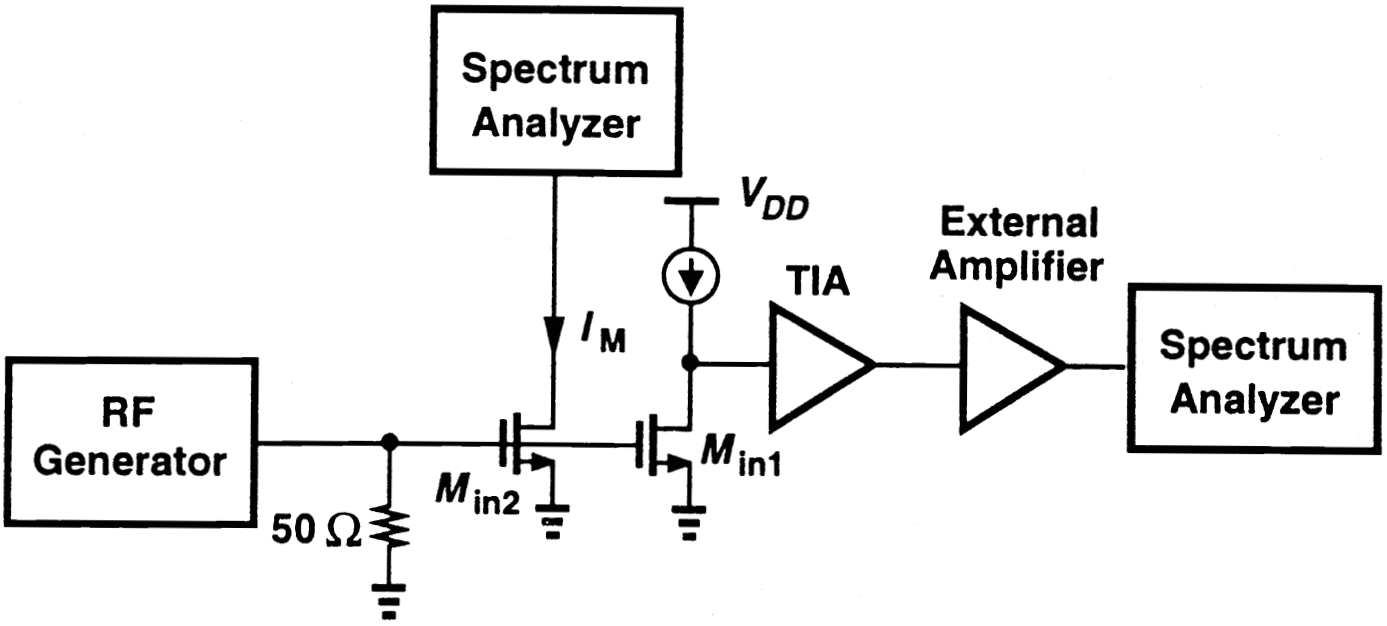

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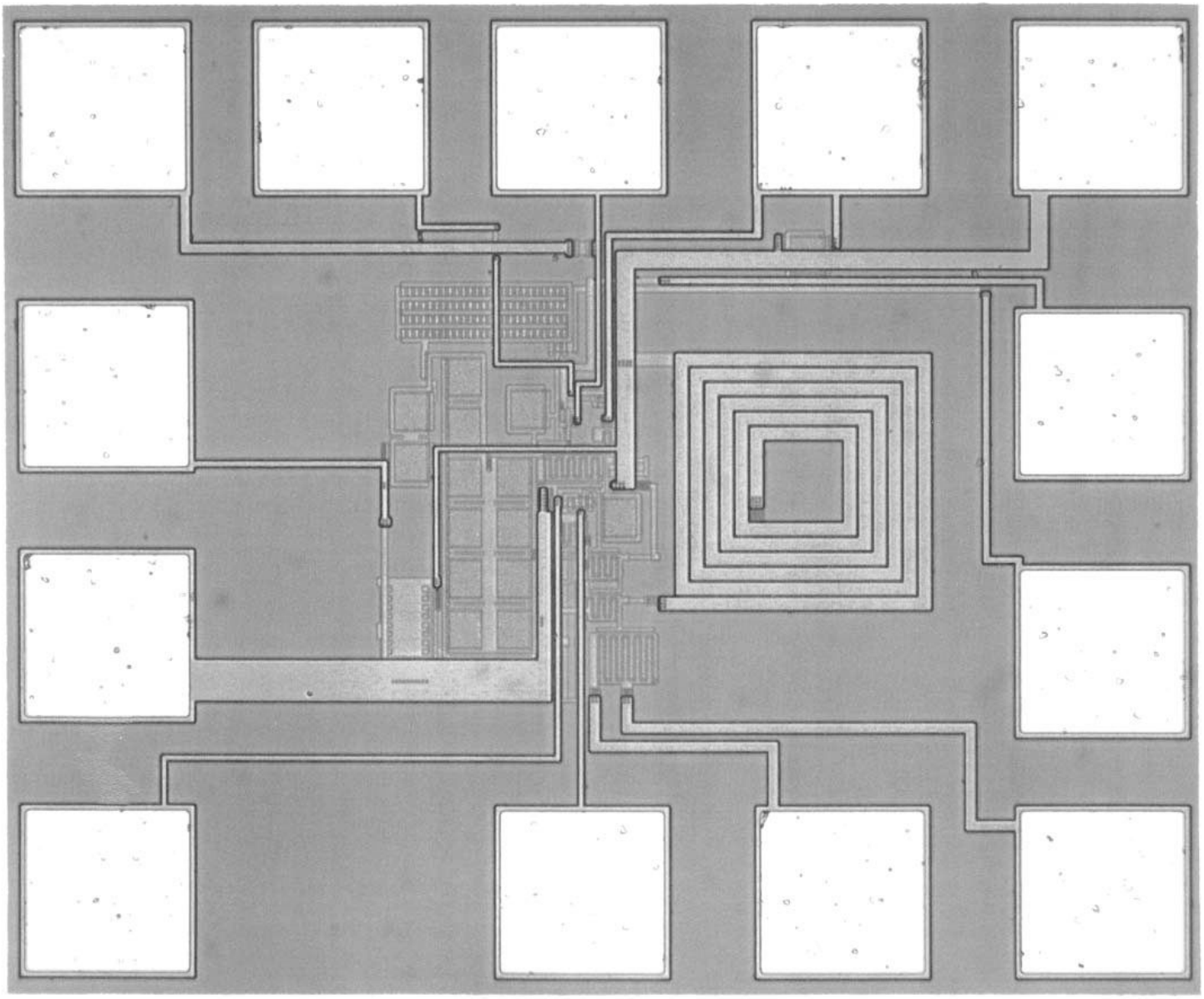

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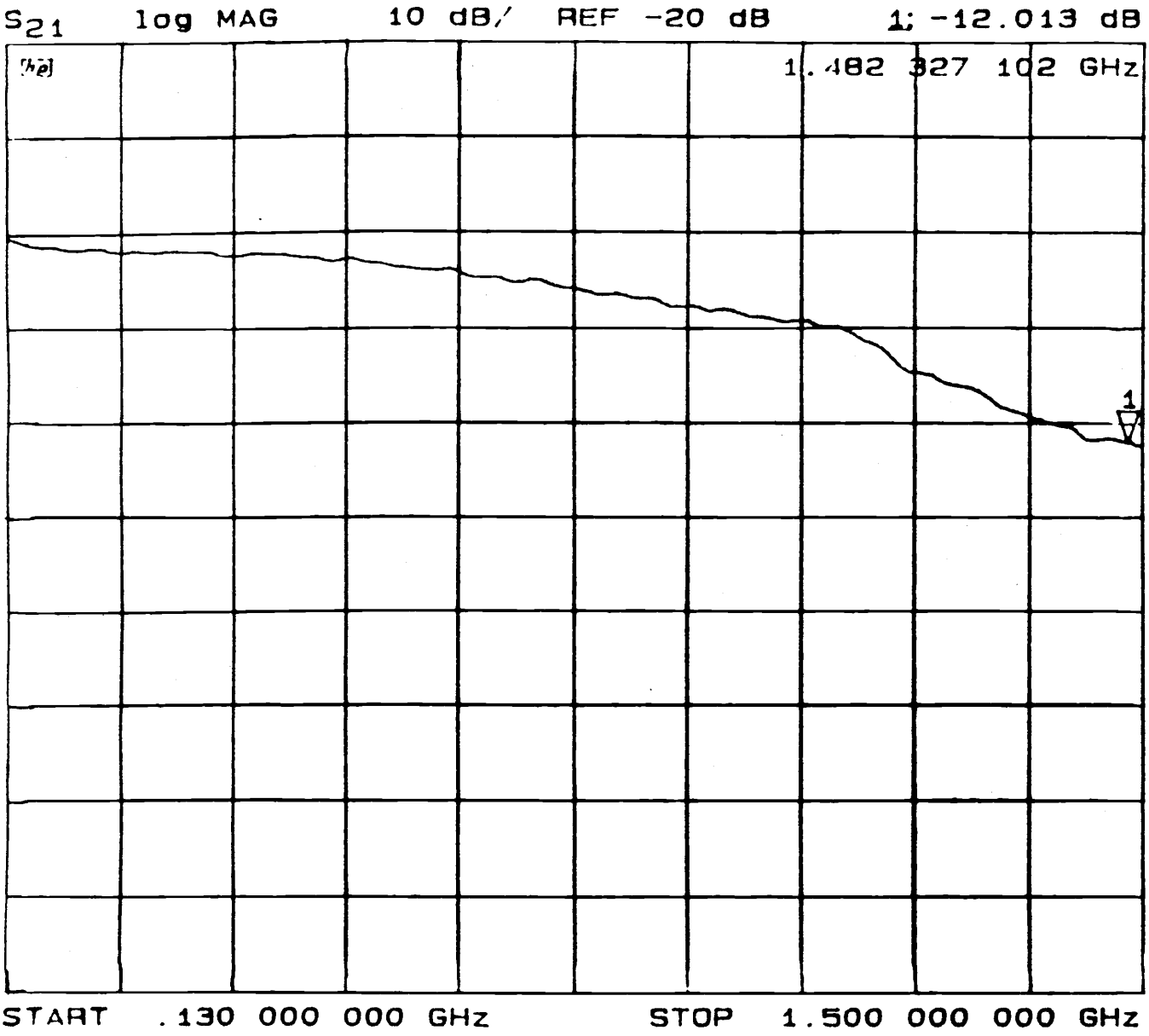

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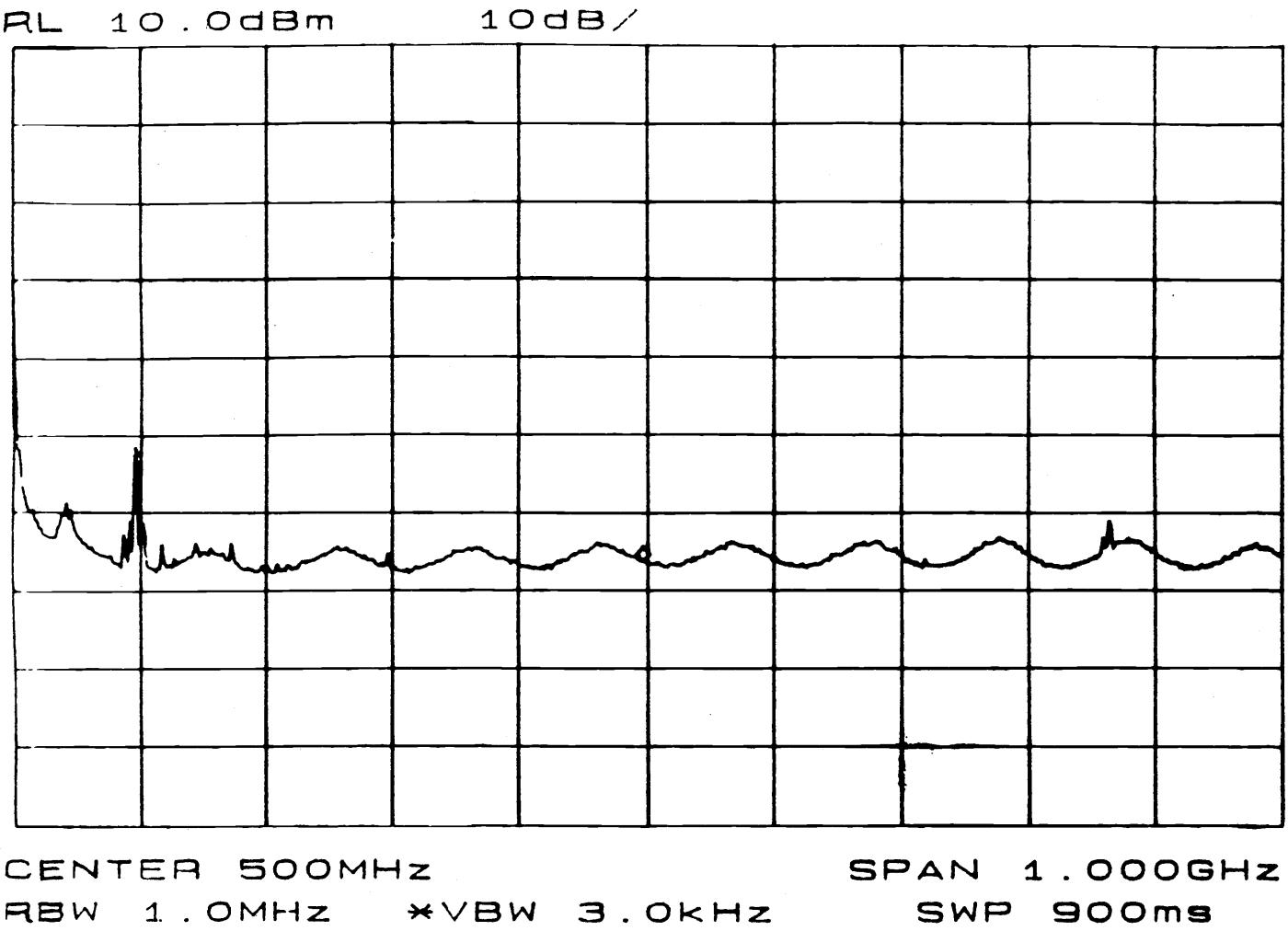

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