## 23.6 Heterodyne Phase Locking: A Technique for High-Frequency Division

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The task of frequency division entails serious challenges at speeds greater than a few tens of gigahertz as flip-flop-based topologies fail and narrowband alternatives emerge as the only viable solution. These alternatives include the Miller regenerative topology and injection-locked oscillators, both of which suffer from a narrow lock range at very high frequencies. For example, the injection-locked divider in [1] achieves a lock range of about 1.5% if no external tuning is applied. Furthermore, these topologies do not readily lend themselves to divide ratios greater than 2 [2].

This paper introduces the concept of "heterodyne phase locking," a technique that can be used to construct high-speed dividers with arbitrary integer or fractional divide ratios. Consider the phase-locked loop (PLL) shown in Fig. 23.6.1, where the phase detector (e.g., a single mixer) is replaced with a cascade of $N$ mixers that are driven by the voltage-controlled oscillator (VCO) output. It is assumed that each mixer is followed by a filter to remove the sum frequency generated by that mixer. In a manner similar to a heterodyne receiver, this cascade of mixers downconverts the input N times, producing a dc component at node X if $f_{in}=N\cdot f_{out}$. In other words, if the loop locks, then $f_{out}=f_{in}/N$.

Heterodyne phase locking offers a number of advantages over other frequency division techniques. First, a divide ratio of, say, 3 is as easily afforded as a divide ratio of 2 – a sharp contrast to flip-flop-based and injection-locked topologies. In fact, as $N$ increases, the only trade-offs that arise are from the necessary reduction of the loop bandwidth, which is tolerable so long as the settling of the PLL is much faster than that of the synthesizer in which it is embedded, and the higher loading imposed on the oscillator, which can be accommodated because the oscillator operates at a proportionally lower frequency.

The second advantage is associated with the lock range. Using a relatively high loop gain (while maintaining a reasonable phase margin), the PLL can achieve a lock range almost equal to the tuning range of the oscillator, which is typically 5 to 10 times the lock range of an injection-locked divider. Note that external (discrete or continuous) tuning techniques applied to injection-locked dividers [1, 2] can be used here as well to further widen the lock range.

The third advantage relates to the output phase noise. Injection-locked dividers, if designed for higher speeds, require that, on the one hand, the tank Q be scaled up to maintain a constant phase noise and, on the other hand, the tank Q be constant to maintain a constant fractional lock range. Therefore, these dividers suffer from a trade-off between the tank Q and produce greater phase noise as the circuit approaches the edge of the lock range. Heterodyne PLLs, however, entail no such trade-offs if their loop gain remains high.

Heterodyne phase-locking can also provide *fractional* divide ratios. If a $\div M$ circuit is inserted in the feedback path of Fig. 23.6.1, then $f_{out}=M\cdot f_{in}/N$. In a more general topology, the LO port of mixer number $j$ of the cascade can include a divide-by-$k_j$ circuit, yielding an overall divide ratio of the form $M/(k_1^{-1}+k_2^{-1}+\ldots+k_N^{-1})$. Many other combinations can be envisaged, e.g., insertion of dividers in series with the RF ports of the mixers, etc.

To demonstrate the potential of heterodyne phase locking, a divide-by-two circuit is designed in a 0.13µm CMOS technology. Figure 23.6.2 shows the realization of the first mixer. Early simulations indicated that, for a given input capacitance and input voltage swing, passive mixers followed by amplifiers provide a greater gain across a wider frequency range than do active mixers. This is partly due to the nearly rail-to-rail swings provided by the VCO. Thus, $M_1$–$M_4$ downconvert $f_{in}$ to $f_{in}/2$, and apply the resulting signal to the tuned stage consisting of $M_5$–$M_6$ and $L_1$–$L_2$. A double-balanced mixer is chosen as it would receive differential inputs when following an on-chip oscillator, but for test purposes, one input is tied to ground through a 25Ω resistor. With their small dimensions ($W/L$=2.5µm/0.13µm), $M_1$–$M_4$ present little capacitance at the input or to the VCO.

Shown in Fig. 23.6.3, the second mixer incorporates PMOS devices $M_7$–$M_{10}$ to both avoid capacitive coupling and bias the gates of the source followers $M_{11}$–$M_{12}$ at $V_{DD}$. The level shift provided by the source followers allows the amplifier $M_{13}$–$M_{16}$ to sustain large output swings, thus maximizing the tuning range of the VCO.

The circuit is fabricated in a 0.13µm CMOS technology and tested with a 1.2V supply and an input swing of –2 dBm. Figure 23.6.4 shows the die micrograph. The die occupies an active area of 200×100µm$^2$. Figure 23.6.5 shows the output spectrum at 35GHz. The circuit achieves a lock range from 64GHz to 70GHz with the –2dBm input swing.

Figure 23.6.6 plots the signal source phase noise and the output phase noise across the lock range, indicating little change in the phase noise suppression provided by the PLL.

*Acknowledements:*
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*References:*
[1] K. Yamamoto and M. Fujishima, "70GHz CMOS Harmonic Injection-Locked Divider," *ISSCC Dig. Tech. Papers*, pp. 600-601, Feb., 2006.
[2] H. Wu and L. Zhang, "A 16-to-18GHz 0.18µm Epi-CMOS Divide-by-3 Injection-Locked Frequency Divider," *ISSCC Dig. Tech. Papers*, pp. 602-603, Feb., 2006.

 

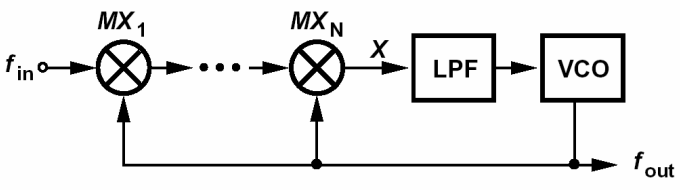


Figure 23.6.1: Heterodyne PLL concept.

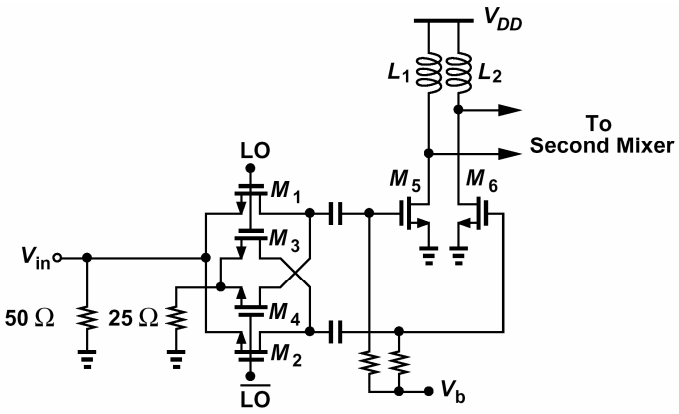


Figure 23.6.2: First mixer implementation.

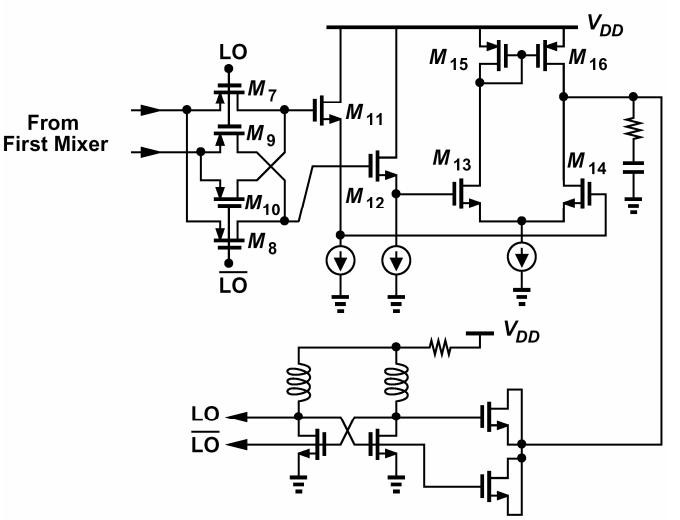


Figure 23.6.3: Second mixer and VCO.

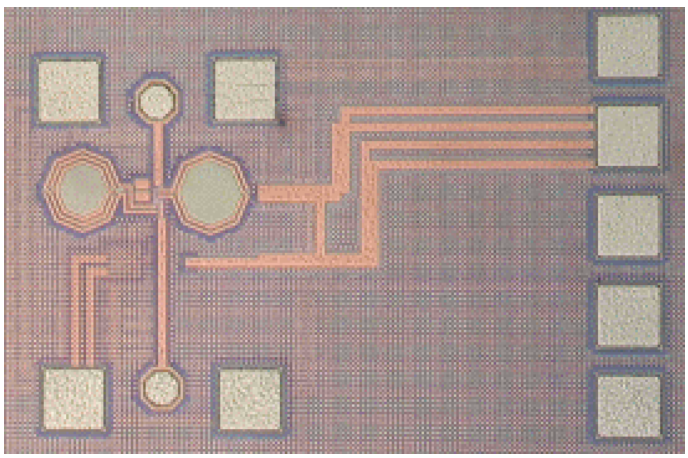

Figure 23.6.4: Divider die micrograph.

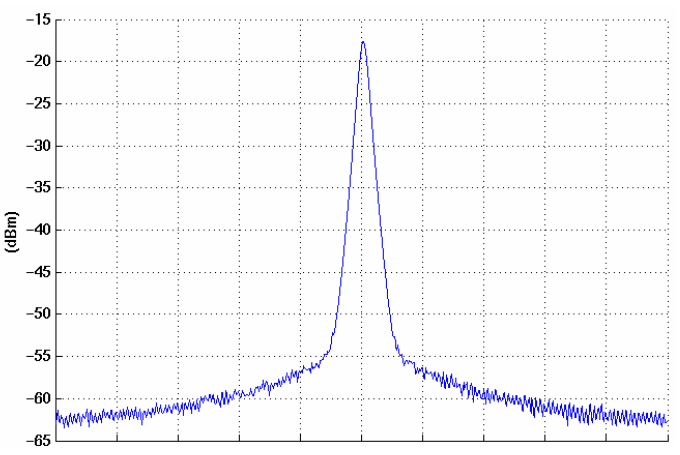


Figure 23.6.5: Measured output spectrum (center frequency: 35GHz, span: 10MHz, RBW: 10kHz).

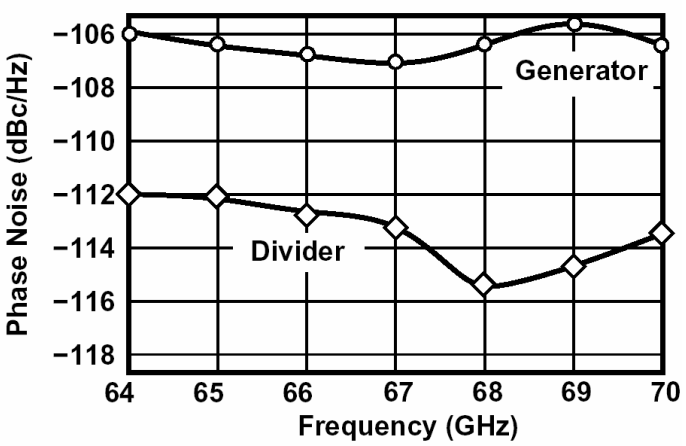


Figure 23.6.6: Measured phase noise.