CMOS Transceivers for the 60-GHz Band[1]

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Abstract

This paper gives an overview of millimeter-wave CMOS transceiver design and presents several critical building blocks operating around 60 GHz. A direct-conversion receiver front end employing new LNA and mixer topologies is described that exploits resonance by means of folded microstrips Also, a direct-conversion transmitter incorporating an on-chip dipole antenna is introduced that paves the way for beamforming and MIMO systems. Finally, a new phase-locked frequency divider is described that, unlike its injection-locked counterparts, maintains a constant phase noise across the input frequency range. The circuits have been fabricated in standard 0.13-μm CMOS technology. Experimental results for each prototype are presented.

I. Introduction

The unlicensed band around 60 GHz presents the possibility of short-range communications at high data rates. The anticipated complexity of transceivers designed for operation in this band makes the use of CMOS technology attractive, especially if techniques such as beamforming and multiple-input-multiple-output (MIMO) signaling are considered.

Today's development of 60-GHz CMOS transceivers is reminiscent of the challenges that faced 5-GHz CMOS wireless LAN circuits in the mid-1990s: the intrinsic speed of the then-available transistors was inadequate, and no significant commercial value had been identified. Nonetheless, if 60-GHz transceivers follow the fate of their 5-GHz counterparts, both of these issues will be resolved in the near future.

This paper reports recent work in the area of CMOS transceiver design for the 60-GHz band, focusing on three challenging circuits: receiver front ends, transmitter front ends, and frequency dividers. Section II describes the design of the receiver front end and some of its building blocks. Section III deals with the transmitter front end and the integrated antenna. Section IV presents a phase-locked frequency divider.

II. Receiver

Figure 1 shows the receiver architecture [1]. The circuit consists of a low-noise amplifier (LNA), quadrature mixers, and baseband gain stages. Since it is extremely difficult to externally generate and distribute differential local oscillator (LO) signals, a single-ended to differential (S/D) converter (balun) is included on-chip. (The port LO_Q is terminated but not driven.)

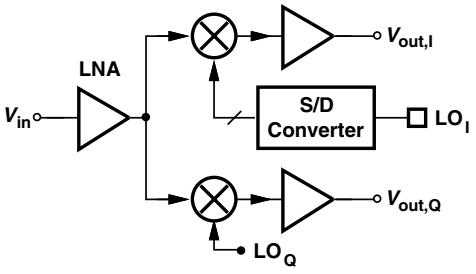

Fig. 1. Receiver architecture.

With an NMOS f_T of about 75 GHz in 0.13-μm technology, the receiver would suffer from a poor performance unless passive resonant devices are exploited in the design. This work incorporates a "folded" microstrip structure as an inductor.

Figure 2(a) shows the LNA implementation, where L_1 resonates with $C_{GS1} + C_{SB1}$ and the pad capacitance, and L_2 with the total capacitance at node X. Transistor M_2 provides

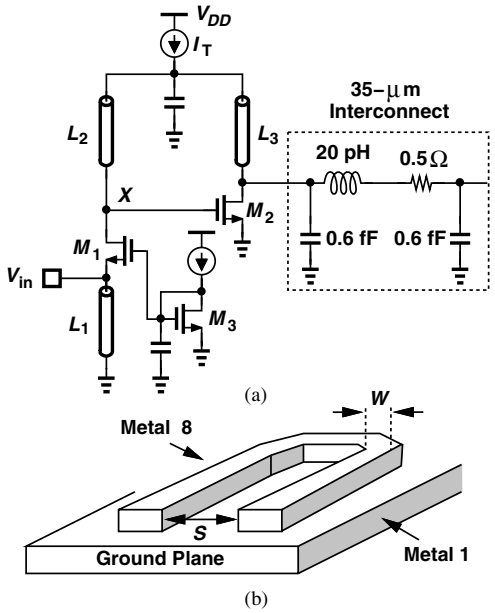

Fig. 2. (a) LNA circuit diagram, (b) folded microstrip.

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additional gain and drive capability for the subsequent quadrature mixers. The three inductors are realized as the folded microstrip depicted in Fig. 2(b). With an equivalent parallel resistance of about 700 Ω, L_1 contributes negligible noise.

It is desirable to avoid ac coupling between the two stages of the LNA and between the LNA and the mixers. Metal-sandwich capacitors suffer from large bottom-plate parasitics, and lateral fringe structures may exhibit resonances close to the band of interest. A biasing scheme is introduced here that obviates the need for coupling capacitors. In the circuit of Fig. 2(b), transistor M_2 serves as a diode-connected device, carrying a current equal to $I_T - I_{D1}$. Thus, if the dc drops across L_2 and L_3 are negligible, M_2 forms a current mirror along with the common-source devices in the next stage, defining the bias current of the mixers.

Due to the physical dimensions of the folded microstrips in the layout, the LNA output must travel 35 μm before reaching the mixers. This interconnect is modeled by the simple network in the dashed box shown in Fig. 2(a).

Figure 3 shows the conventional and proposed mixer topologies. According to simulations, the circuit of Fig. 3(a) exhibits

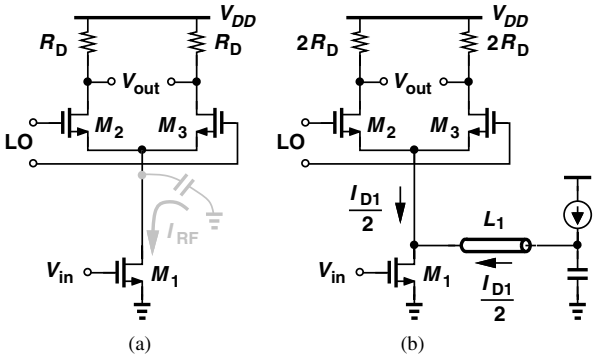

Fig. 3. (a) Conventional and (b) proposed mixer topologies.

a noise figure of 26 dB and a conversion gain of 0 dB. Several mechanisms account for this poor performance [1]. To alleviate these issues, we introduce the topology depicted in Fig. 3(b), where inductor L_1 (a folded microstrip) resonates with the total capacitance seen at the drain of M_1 and also carries about half of the drain current of M_1. Now, most of the RF current is commutated by M_2 and M_3 because the equivalent parallel resistance of L_1 is much greater than the average resistance seen looking into the sources of the switching pair. (For the same reason, the thermal noise contributed by L_1 is negligible.) Moreover, carrying a smaller current, M_2 and M_3 switch more abruptly. Finally, the load resistors can be doubled. As a result, the noise figure falls to about 18 dB and the conversion gain rises to 12 dB.

The receiver front end has been designed and fabricated in 0.13-μm CMOS technology and tested with a 1.2-V supply. Table 1 summarizes the measured performance of the receiver.

III. TRANSMITTER

This section describes the design of a CMOS transmitter front end targeting the 60-GHz band. In addition to tackling challenges in millimeter-wave CMOS design, this work also includes an antenna on the chip to demonstrate the potential of full integration.

Voltage Gain	**28 dB**
Noise Figure	**12.5 dB**
1–dB Compression Point	**–22.5 dBm**
Power Dissipation	**9 mW**
Supply Voltage	**1.2 V**
Active Area	**300 um x 400 um**
Technology	**0.13–um CMOS**

Table 1. Measured performance of receiver.

While somewhat lossy, on-chip antennas offer several significant benefits: (1) they obviate the need for expensive and lossy millimeter-wave packaging; (2) they lend themselves to differential operation, transmitting a greater power for a given voltage swing; (3) the receive and transmit paths can incorporate separate antennas to avoid the use of lossy transmit/receiver switches; (4) the transmitter need not be ac-coupled to the antenna; (5) the antennas can serve in a beamforming array, raising the output power. The last property is particularly important because, with the low supply voltage of deep submicron devices, it is much simpler to construct a multitude of low-power transmitters than one high-power counterpart.

Figure 4(a) shows the fully differential front-end architec-

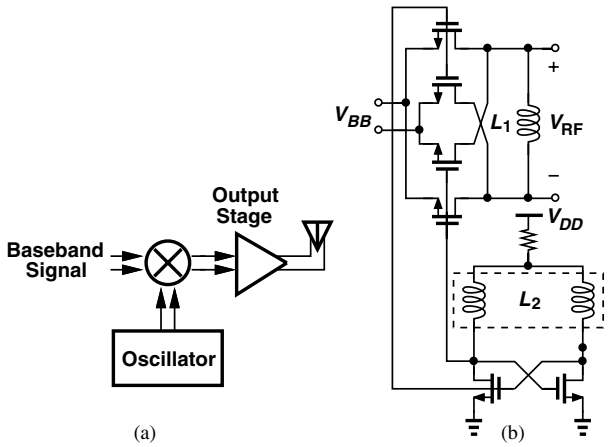

Fig. 4. (a) Transmitter architecture, (b) upconversion mixer and LO.

ture. The transmitter consists of an upconversion mixer, an output stage, and an oscillator. Since it is extremely difficult to generate differential phases from an external source at these frequencies (especially if swings of several hundred millivolts are required) it was decided to include an LC oscillator on chip to drive the mixer directly.

The design of the building blocks is greatly influenced by both the limited speed of the 0.13-μm MOS devices and the heavy load presented by the 50-Ω antenna (100-Ω differential) to the output stage. The large current levels in the output stage (10 mA) call for wide transistors, which in turn limit the bandwidth at the output nodes and create a large load capacitance for the mixer. Use of resonant devices is therefore essential here.

Figure 4(b) depicts the upconversion mixer along with the LC oscillator. The passive double-balanced mixer employs a differential inductor at the output to tune out its own parasitics as well as the input capacitance of the subsequent stage. Since the latter capacitance limits the value of L_1 to about 0.3 nH, an active mixer would suffer from a greater loss here and was discarded. In this design, $L_1 = 0.2$ nH and it is realized as a single turn. The LC oscillator also incorporates a single-turn differential inductor, L_2.

It is desirable to interpose a buffer between the oscillator and the mixer so as to suppress the coupling of (high-speed) basedband data to the oscillator. However, such a buffer would also require one or two inductors, leading to long interconnects at millimeter-wave frequencies. The oscillator produces an output common-mode level of about V_{DD}/2 with rail-to-rail swings. Under this situation, the mixer exhibits a (simulated) conversion loss of -5 dB while driving the output stage.

Figure 5 shows the output stage. With $(W/L)_1 = (W/L)_2 =$

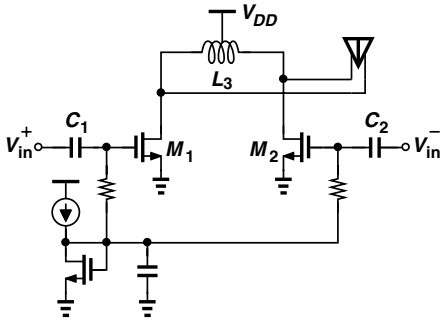

Fig. 5. Transmitter output stage.

25 μm/0.13 μm to carry a bias current of 10 mA, each output node would suffer from a -3 dB bandwidth of 46 GHz with a 50-Ω antenna. Thus, a single-turn differential inductor $L_3(= 0.4$ nH) is added to both tune out the capacitance and provide a dc path to V_{DD}. The output stage delivers a differential voltage swing of 285 mV to the antenna.

The integration of antennas on low-resistivity substrates presents a difficult challenge. Among microstrip, loop, slot and dipole structures, the last one exhibits the lowest loss, about -6 dB. The dipole, which is realized in metal 8, is 1 mm long and 18 μm wide.

With several inductors and one antenna, the routing of millimeter-wave signals between the mixer and the output stage and between that stage and the antenna becomes problematic. To alleviate layout issues, the mixer inductor [L_1 in Fig. 4(b)] is placed inside the output inductor (L_3 in Fig. 5). Shown in Fig. 6 is the overall floor plan, revealing the inevitably long legs between the output stage and the antenna.

The placement of L_1 within L_3 naturally raises concern regarding the coupling between the two. With a coupling factor of $k = 0.27$, the direction of currents in L_1 and L_3 is chosen such that they enhance each other, thus raising the output level by a few dB.

The transmitter front end has been fabricated in 0.13-μm CMOS technology and tested on a chip-on-board assembly with a 1.5 V supply. The circuit consumes 44 mW. Figure 7

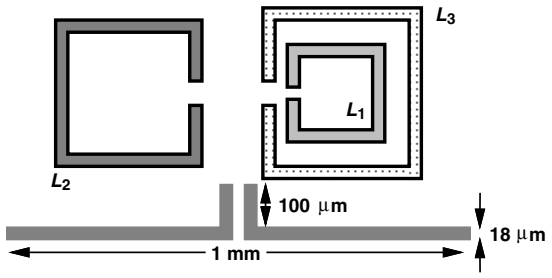

Fig. 6. Transmitter floor plan.

plots the measured far field radiation patterns of the antenna.

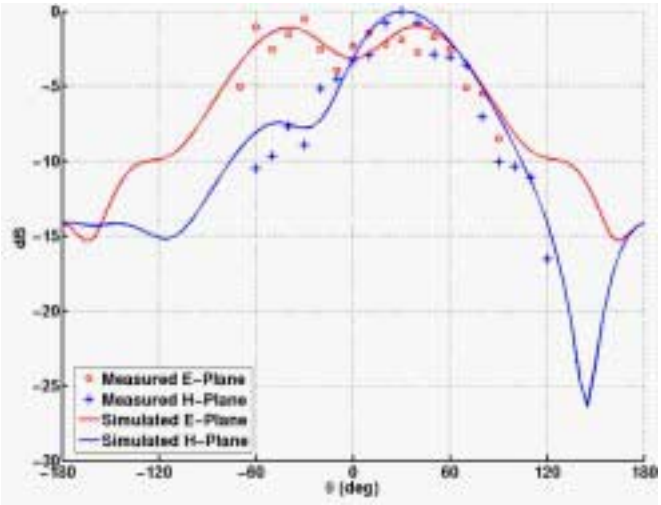

Fig. 7. Measured radiation patterns.

In this test, a differential sinusoid is applied to the baseband.

IV. Frequency Divider

RF transceivers operating in the 60-GHz band require high-speed frequency dividers. Flip-flop-based dividers fail at frequencies above approximately 25 GHz in 0.13-μm CMOS technology, leaving Miller (dynamic) and injection-locked dividers as the two contenders. The use of resonance techniques can improve the speed of CMOS Miller dividers [2], but at the cost of input frequency range. The principal issue with respect to injection locking is that the phase noise of the divider is suppressed significantly only if its natural oscillation frequency is close to half of the input frequency. That is, since the main oscillator and the injection-locked divider in a synthesizer employ fundamentally different tanks, and hence suffer from significant mismatches, the divider input frequency may fall near the edge of its injection lock range, thus allowing the circuit to assume its unlocked phase noise profile [Fig. 8(a)]. Note that ganging the controls of the main oscillator and the divider [3] does not resolve this issue because a mismatch between the two remains if $K_{VCO} \approx 2K_{div}$ [Fig. 8(b)].

This paper introduces a divide-by-two topology that exhibits both a high speed and a relatively constant phase noise across the input frequency range. Shown in Fig. 9(a), the cir-

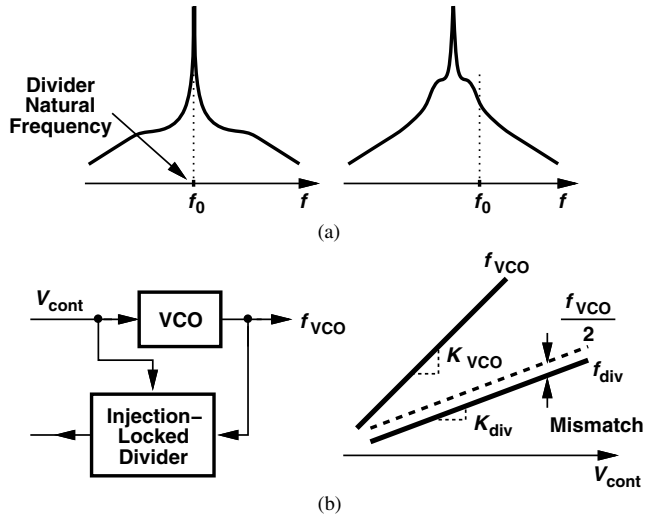

Fig. 8. (a) Phase noise suppression by injection locking, (b) effect of mismatch between $f_{VCO}/2$ and divider frequency.

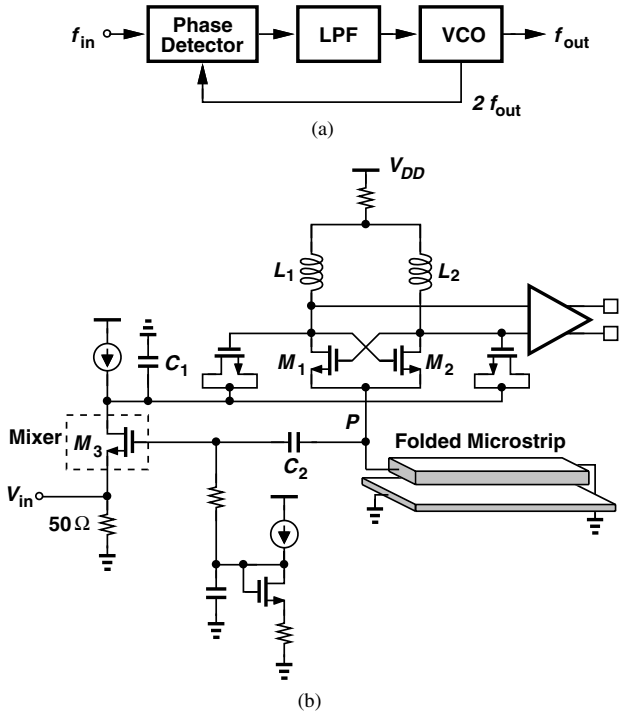

Fig. 9. (a) Phase-locked divider block diagram, (b) realization of (a).

cuit incorporates a voltage-controlled oscillator (VCO) that is phase-locked to the input while producing both $2f_{out}$ and f_{out}. This topology provides two advantages over injection-locked dividers: (1) uniform phase noise suppression across the band so long as the loop gain, specifically, the gain of the phase detector (PD) remains constant; (2) a lock range independent of the Q of the tank.

If employed in a synthesizer loop, the phase-locked divider of Fig. 9(a) must not degrade the overall settling behavior. For this reason, and to maximize the suppression of the oscillator phase noise, the loop bandwidth must be maximized. In this design, the loop bandwidth is set to 2.8 GHz.

Unlike typical PLLs, the above topology operates the phase detector at very high frequencies. To provide a constant and reliable gain, the PD transistor(s) must experience relatively complete switching at 60 GHz, thereby requiring that (1) the PD circuitry be very simple, and (2) the voltage swing provided by the VCO at $2f_{out}$ be sufficiently large (several hundred millivolts).

The above observations lead to the realization shown in Fig. 9(b). Here, a single transistor, M_3, serves as the phase detector and is sized and biased to maximize the gain according to the input level ($\approx$ 0 dBm) and the swing provided by the VCO. Employing a symmetric inductor ($L_1 + L_2$), the VCO produces $2f_{out}$ at node P. The capacitances at this node resulting from M_1, M_2, M_3, and the bottom-plate parasitic of C_2 would limit the voltage swing to less than 100 mV. Thus, a folded microstrip is tied from P to ground, creating resonance at 60 GHz and raising the swing to about 300 mV_{pp}.

The divider circuit has been fabricated in 0.13-μm CMOS technology and tested using high-speed probes with a 1.8-V power supply.[2] Figure 10 depicts the measured output spectrum. The phase noise is approximately equal to -123 dBc/Hz at 1-MHz offset (limited by the input phase noise).

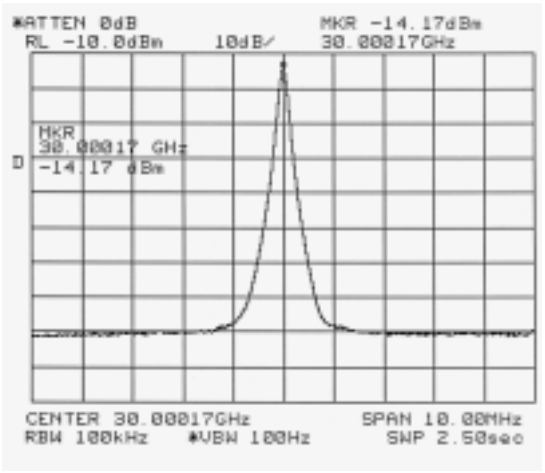

Fig. 10. Measured divider output spectrum at 30 GHz.

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REFERENCES

[1] B. Razavi, "A 60-GHz CMOS Receiver Front End," *IEEE J. Solid-State Circuits*, vol. 41, pp. 17-22, Jan. 2006.

[2] J. Lee and B. Razavi, "A 40-GHz Frequency Divider in 0.18-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 39, pp.594-601, Apr. 2004.

[3] H. R. Rategh, H. Samavati, T. H. Lee, "A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5-GHz Wireless LAN Receiver," *IEEE J. Solid-State Circuits*, vol.35, pp. 780-787, May 2000.

[2]Due to inaccuracies in the MOS varactor model, the oscillator center frequency is below 30 GHz if $V_{DD} = 1.2$ V.