A 7.1-mW 1-GS/s ADC with 48-dB SNDR at Nyquist Rate

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Abstract

A two-stage pipelined ADC employs a double-sampling residue amplifier, two interleaved precharged DACs, and a new calibration scheme to correct for residue gain error, offset, and nonlinearity. Realized in 65-nm CMOS technology and sampling at 1 GHz, the prototype exhibits an FOM of 25 fJ/conversion-step while drawing 7.1 mW from a 1-V supply.

I. Introduction

Pipelined analog-to-digital converters (ADCs) have reached gigahertz sampling rates at resolutions around 10 bits while consuming 30 to 40 mW [1, 2] and exhibiting a figure of merit (FOM) of 70 to 90 fJ/conversion-step. Most pipelined architectures avoid the use of a multi-bit *second* stage as its high input capacitance would slow down the residue generation in the first stage. However, a two-stage pipelined architecture remains attractive because it would eliminate the residue amplifiers necessary in the subsequent stages, potentially saving power.

This paper presents a two-stage pipelined ADC that employs 33 comparators and one differential amplifier in 65-nm CMOS technology to achieve a resolution of 9 bits at 1 GHz with an FOM of 25 fJ/conversion-step. A new calibration technique corrects the gain error and nonlinearity of the open-loop residue amplifier as well as the offsets of the comparators, leading to a low-power design.

Section II introduces the proposed ADC architecture and Section III describes the precision techniques employed in this work. Section IV presents the experimental results.

II. ADC Architecture

A. High-Level View

Shown in Fig. 1 (a) is a functional single-ended diagram of the system. The converter consists of a 5-bit coarse flash sub-ADC (ADC_1), two resistor-ladder DACs (sharing the same ladder), a residue amplifier, and a 5-bit fine flash sub-ADC (ADC_2). At a sampling rate of 1 GHz with realistic clock transitions and non-overlap times, the overall system must acquire and convert in about 950 ps. In order to relax the trade-off of the residue amplifier, the ADC employs three techniques: (1) a double-sampling network composed of C_{S1} and C_{S2} in the front end, (2) two interleaved resistor-ladder DACs, and (3) pipelining after the amplifier. As a result, the amplifier has one full clock period to settle. To interleave the two DACs, each coarse comparator is followed by two time-interleaved paths whose outputs drive two switches tied to one tap of the resistor ladder. One bit of redundancy accommodates comparator offsets and timing mismatches in the front end.

The timing diagram in Fig. 1 (b) illustrates the operation at a high level. In the first half cycle (from 0 to t_1), C_{S1} and the coarse sub-ADC sample the input while DAC_1 is precharged [2]. The next half cycle is entirely allocated to ADC_1's conversion, after which one ladder tap voltage is selected. . The following complete cycle (from t_2 to t_4) is dedicated to the settling of V_{DAC1} and V_{res}. At $t = t_4$, switch S_F turns off so as to freeze the residue, and ADC_2 begins to convert. Additionally, at $t = t_2$, C_{S2} and ADC_1 start sampling the input while DAC_2 is precharged. DAC_2 and C_{S2} then produce and hold the residue at the input of the amplifier for one clock cycle.[1]

B. Detailed Architecture

Figure 2 shows the ADC architecture in greater detail, highlighting the power-saving methods applied to this design. The 5-bit coarse stage utilizes a comparator as a polarity detector, allowing a twofold reduction in the number of comparators and hence their kick-back noise and power consumption. Once the sampling of the analog input is completed, this comparator is clocked and its decision slides the reference of the 15 comparators to either the top or the bottom half of the full scale, i.e., $[V_{REF1}^{+}\ V_{mid}]$ or $[V_{REF1}^{-}\ V_{mid}]$, respectively. After 100 ps, these 15 comparators are clocked and their collective decision is used to update V_{DAC1} or V_{DAC2} (which have been precharged to V_{in} during the sampling mode). In addition to reducing the power and hardware, the above reference sliding scheme also presents only half of the analog input swing to the comparators. As a result, the overall ADC can accommodate rail-to-rail input swings. These benefits accrue at the cost of 170 ps in the conversion time of the coarse ADC.

By virtue of pipelining, the fine ADC has a half cycle for conversion, and hence, first detects the polarity of the amplified residue by means of three comparators.[2] Based on this decision, either the top or the bottom bank of comparators is clocked [3]. To save power, the fine ADC shares the inter-

[1] To remove dynamic errors, a small portion of the cycle is assigned to resetting the input nodes of the residue amplifier.

[2] The use of three comparators rather than one relaxes the offset requirement.

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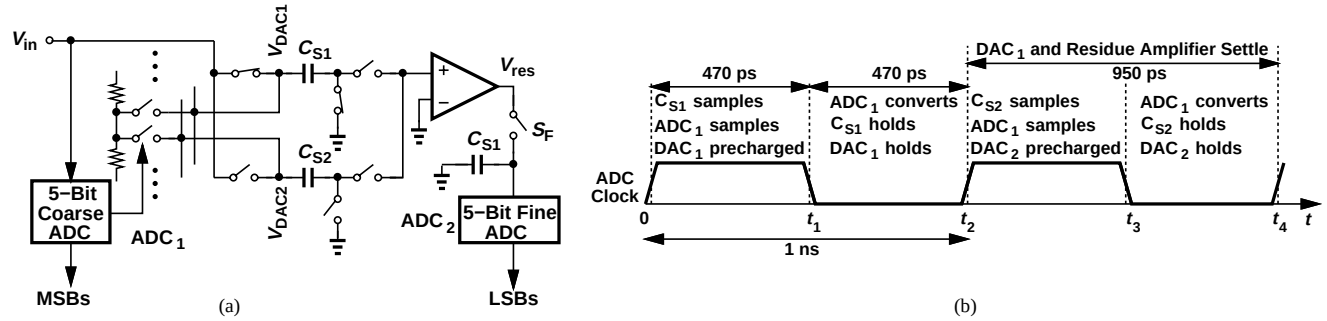

Fig. 1. ADC (a) high-level view, and (b) timing diagram.

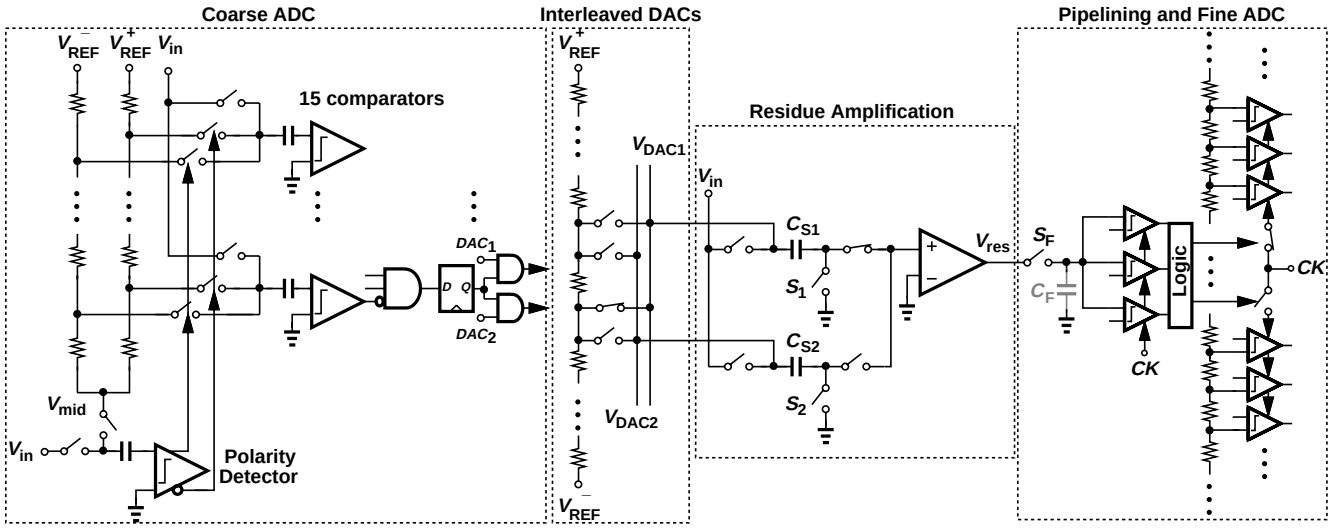

Fig. 2. Detailed ADC architecture.

leaved DACs' resistor ladder even though Fig. 2 shows two separate ones for clarity.

In order to reduce the effect of the timing mismatch between the samples taken by C_{S1} and C_{S2}, this design employs an additional clock phase within the switch bootstrapping circuits, thus reducing the mismatch to that of two switches.

III. Precision Techniques

A fast, power-efficient design naturally incorporates small, poorly-controlled devices, thus necessitating additional means to improve the precision. A key issue is the hardware and power overhead associated with such means. This section describes two techniques that ultimately lead to an SNDR of 51 dB at low input frequencies and 48 dB at the Nyquist rate with a conversion rate of 1 GHz.

A. Offset Cancellation

At a clock frequency of 1 GHz and with a response time of about 150 ps, 33 comparators can consume considerable power - unless their design is linearly scaled down to the point where their electronic noise limits the performance. However, with nearly-minimum size transistors, the offset grows quite large, demanding a proportionally wide correction range and prohibitive overhead. Additionally, the offset correction devices themselves may contribute a large noise and/or offset and slow down the circuit.

For the offset cancellation technique to negligibly degrade the speed of a comparator, it is desirable to avoid tying appendages (e.g., programmable capacitors [3, 4]) to the internal nodes. In this work, the coarse and fine ADCs employ a cancellation technique that resides entirely outside the comparator. Illustrated in Fig. 3(a), our approach calibrates comparator number j for a decision threshold of V_j as follows: (1) connect one input to V_j, (2) change the other input by means of DAC_j until the comparator output changes, and (3) freeze the DAC_j content. To minimize the effect of comparator noise on the calibration, this procedure is repeated 10 times and the average value is chosen.

The dedicated DACs in Fig. 3 (a) may appear to add great complexity. However, we recognize that DAC_j need only generate a moderate range around V_j. The DACs can therefore be embedded within the main resistor ladder as depicted in Fig. 3(b), provided that the ladder yields sufficient resolution for offset cancellation. With 64 taps and differential implementation, the offset of coarse comparators is reduced to 4 LSB. The fine ADC offsets are corrected in a similar manner.

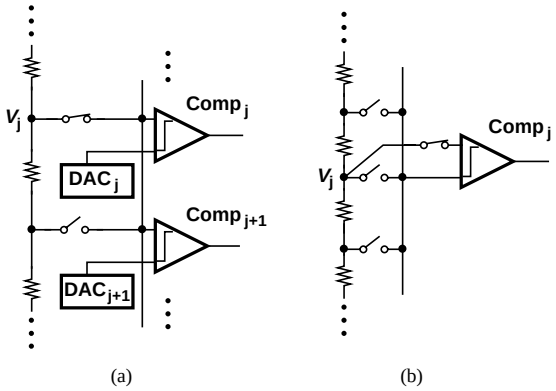

Fig. 3. (a) Conceptual offset calibration technique, and (b) actual implementation.

B. Proposed Calibration Technique

The open-loop residue amplifier in Fig. 2 introduces gain error, offset, and nonlinearity, the most critical impact of which is a residue range that does not match the full scale of ADC_2. We propose a low-complexity calibration technique that "programs" the fine stage so as to match the residue range. Depicted in Fig. 4(a), the idea is to adjust the decision thresholds of the fine ADC so as to remove comparator offsets as well as reach a full scale that is aligned with the minimum and maximum residue values.

Calibration proceeds as follows. In the sampling mode, one of the precision tap voltages produced by the resistor ladder DAC, V_k, is impressed on the top plate of C_{S1} in Fig. 2. Next, the top plate switches to zero, and the resulting voltage is amplified and applied to the fine ADC. This voltage experiences the gain error, nonlinearity, and offset of the residue amplifier [Fig. 4(b)], but, for correct operation, it must trip a known comparator, number k. Thus, the reference voltage of comparator k is iteratively adjusted by DAC_k until it trips for a sampled voltage of V_K. This procedure is repeated for all of the fine comparators, covering a total range of ± 36 LSB around the nominal voltage tap. As with the coarse ADC, DAC_k is in fact embedded within the resistor ladder [Fig. 4(c)].

IV. Experimental Results

The prototype ADC has been designed and fabricated in standard 65-nm CMOS technology in an active area of 350 μm $\times$ 280 μm. Figure 5 shows the die photograph. The foreground offset cancellation and calibration are performed off-chip, with the results returned to on-chip registers through a serial bus. The ADC has been tested in a chip-on-board assembly. All of the measurement results reported below are for a sampling rate of 1 GHz with a 1-V supply.

Figure 6 plots the differential nonlinearity (DNL) and integral nonlinearity (INL), before and after calibration, indicating maximum values of -0.87 LSB and $+1.8$ LSB, respectively.

Figure 8 shows the output spectrum for an analog input frequency of 490 MHz, demonstrating an SNDR of 48 dB and an SFDR of 58 dB at Nyquist rate. Figure 7 plots the SNDR as a function of the input frequency, revealing a low-frequency value of 51 dB. Table I summarizes the measured performance

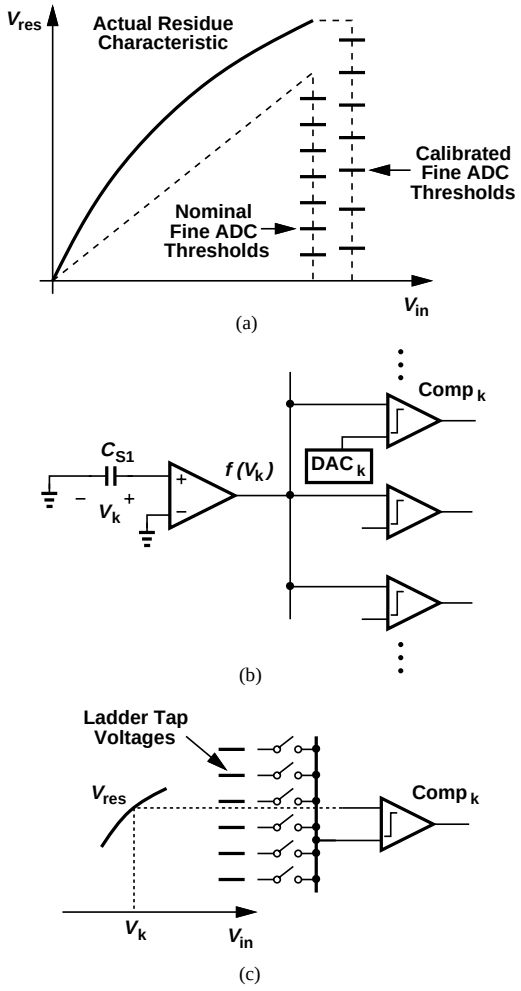

Fig. 4. (a) Calibration of fine ADC decision thresholds to correct for residue errors, (b) conceptual implementation, and (c) use of main ladder to realize voltage taps.

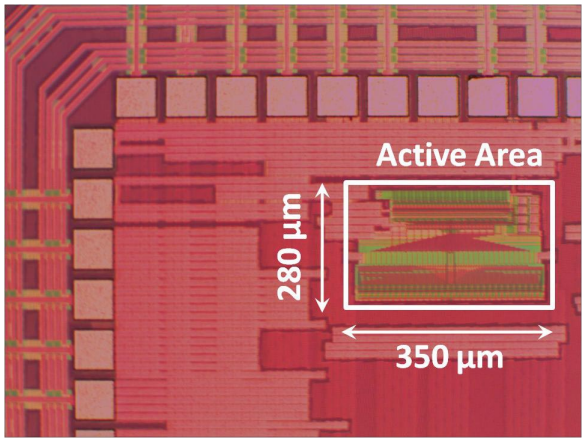

Fig. 5. ADC die photograph.

of the prototype and compares it with that of recent prior art in the range of 8 to 10 bits.

V. Conclusion

The use of a double-sampling front end, interleaved precharged DACs, and a new comparator-based calibration scheme allows

two-stage pipelined ADCs to operate at high speeds with good dynamic performance. A 60-nm 1-GHz prototype exhibits an SNDR of 48 dB at Nyquist-rate while consuming 7.1 mW.

Acknowledgment

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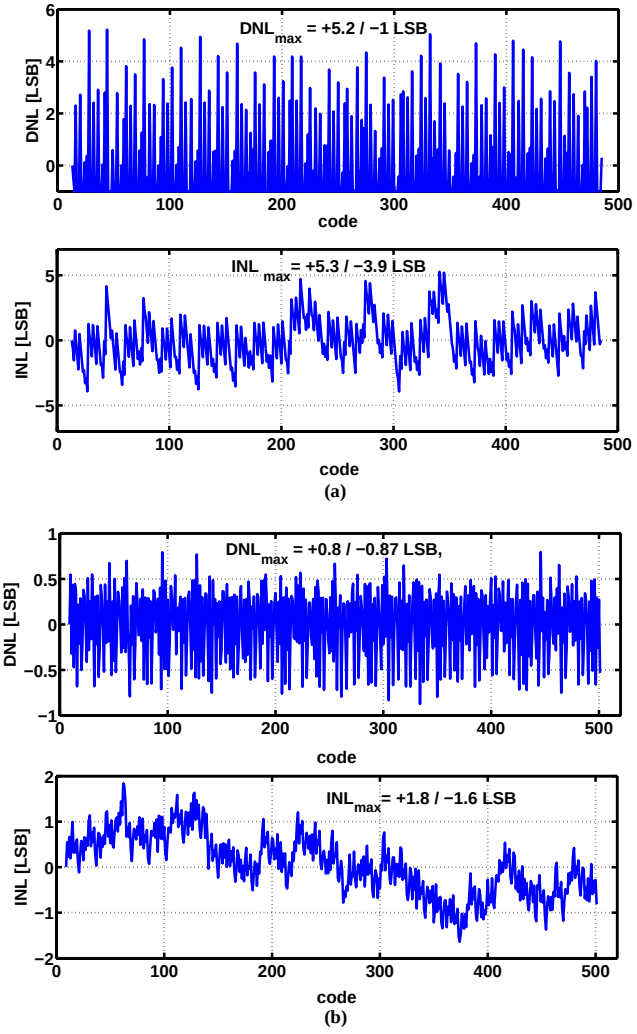

Fig. 6. Measured DNL and INL (a) before, and (b) after calibration.

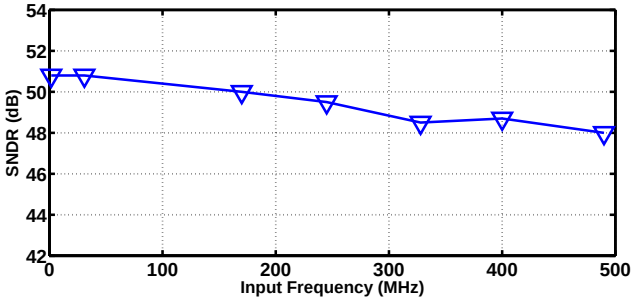

Fig. 7. Measured SNDR versus input frequency at a sampling rate of 1 GHz.

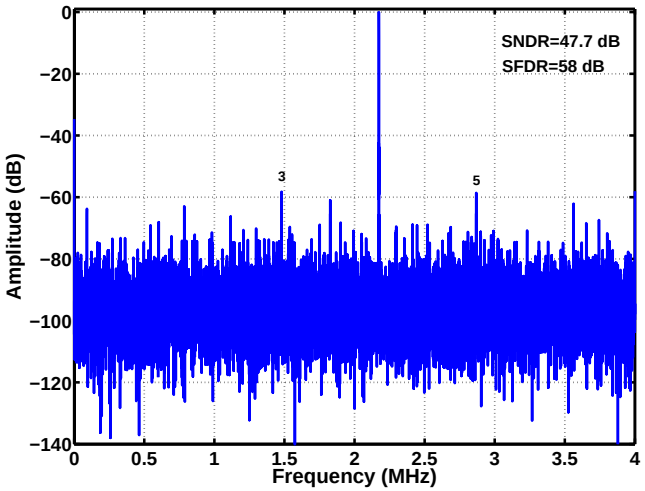

Fig. 8. ADC output spectrum at a sampling rate of 1 GHz and an input frequency of 490 MHz (downsampled by a factor of 125).

Table I. ADC PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	Sahoo VLSI 2012	Hashemi CICC 2012	Hong ISSCC 2013	Lien VLSI 2012	This Work
Resolution (bit)	10	10	9	8	9
Input Cap. (pF)	NA	0.7	0.7	NA	0.45
SNDR (dB) Low Freq./ Nyquist	56 / 52	57 / 53	54 / 51	45 / 43	51 / 48
f_S (MHz)	1000	1000	900	750	1000
Power (mW)	33	36	10.8	4.5	7.1
FoM (fJ/CS) @ Low Freq.	75	70	30	41	25
FoM (fJ/CS) @ Nyquist.	97	100	40	50	34
Technology (nm)	65	65	45	28	65
Supply (V)	1.2	1.2	1.2	1.0	1.0
Active area (mm^2)	0.225	0.175	0.038	0.004	0.1

REFERENCES

[1] B. D. Sahoo and B. Razavi, "A 10-Bit 1-GS/s 33-mW ADC," *IEEE Symp. on VLSI Circuits*, pp. 30–31, June 2012.

[2] S. Hashemi and B. Razavi, "A 10-Bit 1-GS/s CMOS ADC with FOM = 70 fJ/Conversion," *IEEE Custom Integrated Circuits Conference*, pp. 296–297, Sept, 2012.

[3] B. Verbruggen et. al., "A 2.6-mW 6b 2.2GS/s 4-times Interleaved Fully Dynamic Pipelined ADC in 40nm Digital CMOS," *IEEE Int. Solid-State Circuits Conference* , pp. 1–4, Feb. 2010.

[4] G.. Van der Plas and B. Verbruggen, "A 150 MS/s 133 μW 7 bit ADC in 90 nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol.43, No.12, pp. 2631–2640, Dec. 2008.