4.6 A 10b 500MHz 55mW CMOS ADC

Ashutosh Verma, Behzad Razavi

University of California, Los Angeles, CA

Recent work on ADCs targeting sampling rates of hundreds of MHz with resolutions in the range of 10 to 11b has faced speed limitations with a single channel [1] or employed interleaving, but with a relatively high power dissipation [2] or low SNDR [3]. This paper introduces a calibration technique that, together with a high-speed opamp topology, allows a single channel to operate at 500MHz and digitize a 233MHz input with an SNDR of 53dB. This SNDR yields a figure of merit (FOM) of 0.3pJ/conversion-step, the lowest reported for 10 and 11b ADCs running at these frequencies.

Figure 4.6.1 shows the pipelined ADC architecture. It consists of thirteen 1.5b stages and one 1b stage. The ADC also incorporates an on-chip reference DAC for calibration. The first 2 stages are calibrated for capacitor mismatch, opamp gain error, and opamp nonlinearity; the next 4 stages for capacitor mismatch and opamp gain error; and the next 7 stages for opamp gain error. In Fig. 4.6.1, w_j denotes the scaling factor for the output of each stage [ideally equal to $(1/2)^j$]. Also, α_1 and α_3 denote the coefficients of a 3rd-order polynomial that approximates the inverse function of each MDAC transfer characteristic. The LMS machine adapts the values of w_j and α_j during calibration. The first flash stage and MDAC sample the input simultaneously, avoiding a dedicated front-end sampler and its associated noise and distortion.

The calibration details are described with the aid of the conceptual diagram shown in Fig. 4.6.2, where D_{in} denotes the digital input applied to the reference DAC so as to deliver a corresponding voltage to stage j. Calibration begins with the back-end, namely, stages 7 to 14 (j=7). The reference DAC applies three levels to the input of stage 7: $\pm V_{REF}/4$ and 0, where V_{REF} is the single-ended full scale of the overall ADC. Also, the MDAC in stage 7 is configured so as to operate simply as a multiply-by-2 circuit, thereby avoiding the DAC capacitor mismatch. With path B disabled, the back-end digital value is then compared with the ideal value, D_{in}, and a single value for $w_k = w^k$, k = 7 to 14, is reached so as to minimize the error. That is, the MDAC gains in the back-end stages are assumed to match adequately. With the back-end having approached a nearly ideal quantizer, the calibration then moves to stages 3 to 6. In a similar manner, the values of w_k, k = 3 to 6 are calibrated individually by applying $\pm V_{REF}/4$ and 0 to the input of the stage under test. Moreover, DAC capacitor mismatches are calibrated by applying an input equal to $V_{REF}/2$ to stage 6 (j = 6 in Fig. 4.6.2), and operating the MDAC in the regular mode (sampling, D/A conversion, multiplication by 2). The digital output $D_7 \ldots D_{14}$ is ideally equal to zero, thus revealing the error due to DAC mismatch. With path B disabled, this error is computed, stored, and subtracted from the overall output during normal operation. The same procedure is repeated for stages 5 to 3.

The last step of calibration deals with opamp nonlinearity. With j = 2 in Fig. 4.6.2 and path A disabled, the reference DAC applies $\pm V_{REF}/2$ while stage 2 remains in the multiply-by-2 mode. That is, $D_2 = 0$ and $D_3 \ldots D_{14}$ represents the nonlinearity of the opamp. The LMS machine then adjusts the value of α_3 so as to drive this output to zero.

The ADC derives its performance from two key building blocks: the opamp and the reference DAC. Figure 4.6.3 shows the opamp topology. Employing a 2-stage configuration to maximize the output swing, the circuit avoids cascodes and hence additional poles, exhibiting a 2-pole transfer function (before compensation). It also incorporates only minimum-length transistors in the signal path to achieve a compensated unity-gain bandwidth of approximately 10GHz with a load capacitance of 0.3pF. Under these constraints, the open-loop gain is about 25.

The required high-speed settling makes it difficult to use common-mode (CM) feedback loops having multiple poles because large-signal, nonlinear CM transients degrade the differential settling behavior. Thus, the output CM level of the first stage is simply set at $V_{DD}-|V_{GSP}|$, which also defines the bias current of the second stage as a scaled replica of I_{SS} by virtue of the current mirror action between the PMOS loads of the first stage and the input transistors of the second. To establish an output CM level near $V_{DD}/2$ for the second stage, a constant current I_1 is drawn from R_{c1} and R_{c2}, thereby creating a level equal to $V_{GS7,8}+0.5I_1R_{C1,2}$.

In the first MDAC, the first stage of the opamp draws a bias current of 1.6mA and the second, 6.4mA, allowing the circuit to settle to 11b precision in about 1ns. The MDAC is scaled down by a factor of 2 in the second stage and 4 in the third stage. Stages 4 to 13 remain unscaled due to the small size of capacitors (25fF) and negligible power consumption.

The reference DAC is realized as a resistor ladder (Fig. 4.6.4). In order to improve the linearity, the ladder is formed as a single piece of non-silicided polysilicon, thereby avoiding current-carrying contacts and their resistance mismatches. Extensive measurements on this ladder indicate a consistent linearity of at least 11b. While it is tempting to utilize this ladder rather than capacitors in each MDAC, the settling proves excessively long with the required sampling capacitors. (Calibration is performed at 100 MHz).

The ADC is fabricated in standard 90nm CMOS technology and tested with the die directly attached to the board. The reference (V_{REF}) is provided externally. Figure 4.6.7 shows the die, whose active area is about 700µm x 700µm. The calibration is performed off-chip. Gate-level synthesis of the logic shows a complexity of 20,000 gates with a power consumption of 8mW at 500MHz in 90nm technology. The output data are downsampled by a factor of 16 to ease capture and testing.

Figure 4.6.5 shows the measured DNL and INL at a sampling rate of 500MHz after gain error, capacitor mismatch, and nonlinearity calibration. The uncalibrated prototype suffers from a large number of missing codes and an INL of 40 LSB. After full calibration, the DNL and INL fall below 0.4 LSB and 1 LSB, respectively.

Figure 4.6.6 plots the measured SNDR as a function of the analog input frequency with a sampling rate of 500MHz. The SNDR is equal to 53dB at an input frequency of 233MHz with a power consumption of 55mW. This translates to an FOM of 0.3pJ/conversion-step, a factor of 2 lower than those reported in [2,3].

Acknowledgment:
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References:

[1] S. Lee et. al, "A 10b 205MS/s 1mm² 90nm CMOS Pipeline ADC for Flat-Panel Display Applications," *ISSCC Dig Tech. Papers*, pp. 458-459, Feb. 2007.
[2] C. Hsu et al, "An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration," *ISSCC Dig. Tech. Papers*, pp. 464-465, Feb. 2007
[3] S. M. Louwsma et. al, "A 1.35 GS/s, 10b, 175 mW Time-Interleaved AD Converter in 0.13µm CMOS," *IEEE Symp. VLSI Circuits*, pp. 62-63, June 2007.

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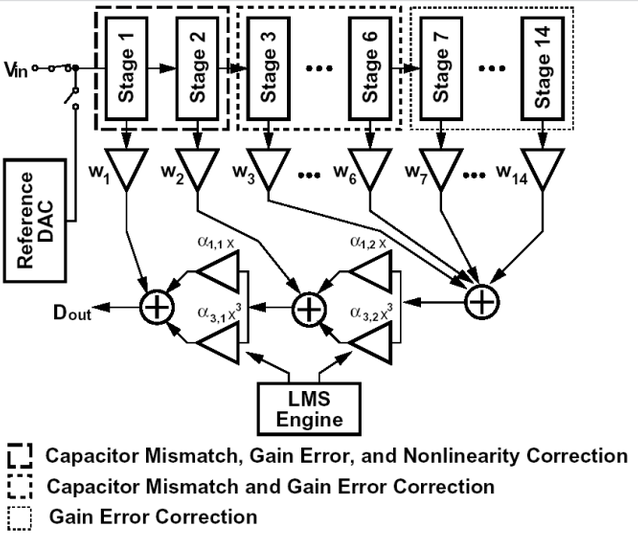

Figure 4.6.1: Pipelined ADC architecture.

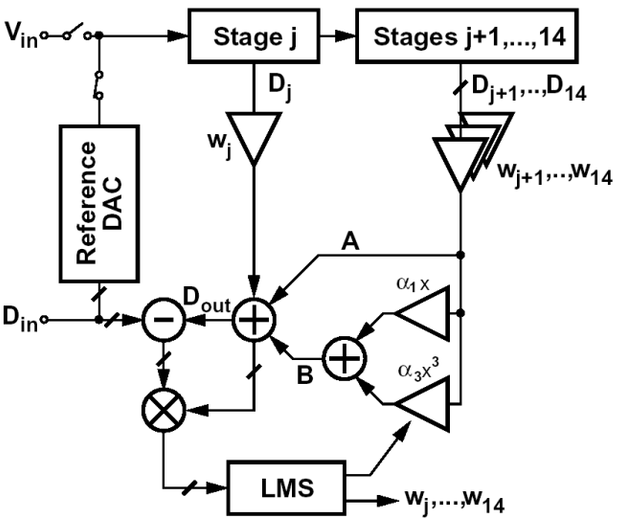

Figure 4.6.2: Digital calibration.

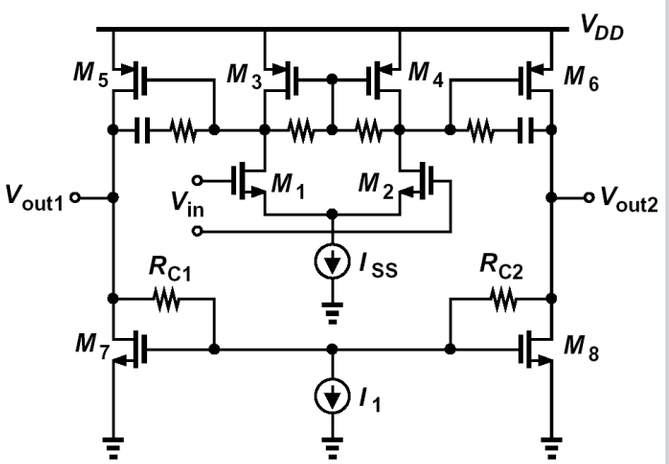

Figure 4.6.3: Opamp circuit diagram.

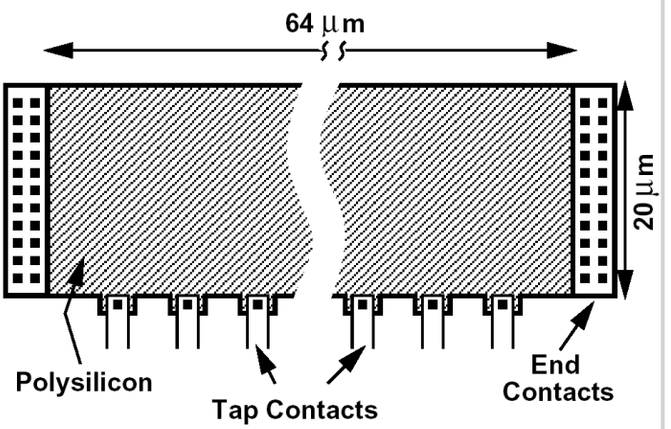

Figure 4.6.4: Reference DAC resistor ladder.

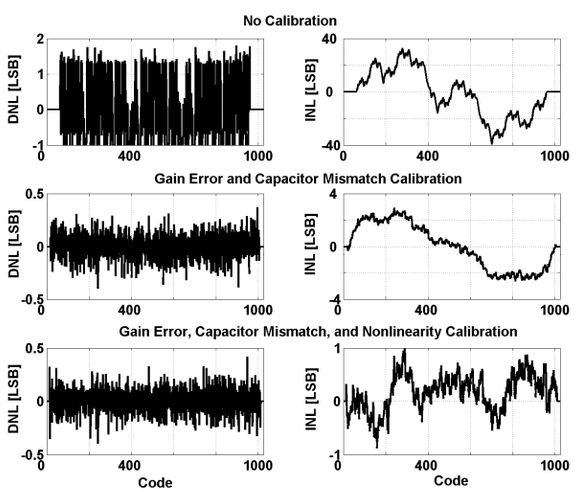

Figure 4.6.5: Measured differential and integral nonlinearity at a sampling rate of 500MHz.

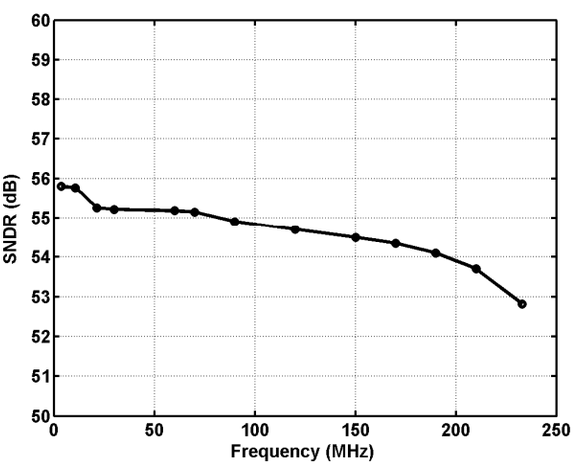

Figure 4.6.6: Measured SNDR as a function of input frequency at a sampling rate of 500MHz.

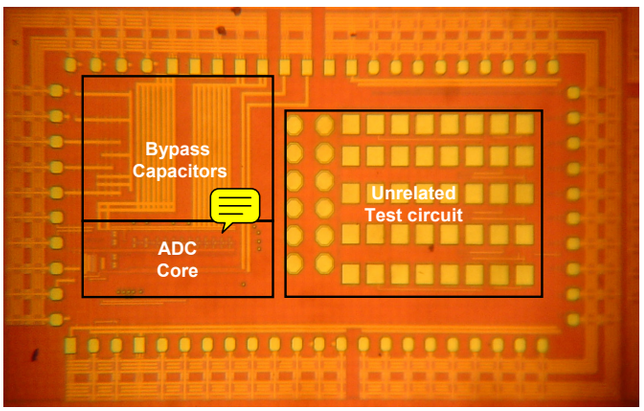

Figure 4.6.7: Die micrograph.

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