# Cognitive Radio Design Challenges and Techniques

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***Abstract*—Cognitive radios are expected to communicate across two or three frequency decades by continually sensing the spectrum and identifying available channels. This paper describes the issues related to the design of wideband signal paths and the decades-wide synthesis of carrier frequencies. A new CMOS low-noise amplifier topology for the range of 50 MHz to 10 GHz is introduced that achieves a noise figure of 2.9 to 5.7 dB with a power dissipation of 22 mW. Several multi-decade carrier generation techniques are proposed and a CMOS prototype is presented that exhibits a phase noise of −94 to −120 dBc/Hz at 1-MHz offset while consuming 31 mW.**

***Index Terms*—Broadband radios, LO harmonics, mixer spurs, software-defined radio, wideband frequency synthesis, wideband LNAs.**

## I. Introduction

THE heavy usage of the cellular and wireless local area network (WLAN) bands has made the notion of "cognitive radios" (CRs) attractive. Unlike conventional wireless transceivers, which operate in only certain preallocated bands, CRs are envisioned to utilize any unoccupied channel in a wide frequency range, e.g., from tens of megahertz to about 10 GHz. This is accomplished by sensing and detecting available channels before initiating communication [1], [2]. Recent efforts on CR design have focused on the TV bands below 1 GHz [3], but it is expected that CRs will eventually exploit a much wider spectrum.

Cognitive radios pose challenges at all levels of abstraction. This paper deals with their RF and analog design issues and describes architecture and circuit techniques that prove useful in the implementation of CRs. The paper provides a detailed treatment of some of the concepts presented in [4], [5] and also introduces a number of previously unpublished ideas.

Section II deals with the signal path design, elaborating on low-noise amplifier (LNA) issues, effect of nonlinearities, and the problem of local oscillator (LO) harmonics. Section III concerns the challenge of multi-decade carrier synthesis, offering a number of solutions, and Section IV briefly discusses spectrum sensing considerations. Section V presents experimental results for the LNA and carrier generation circuit prototypes. CR transmitter design is not discussed in this paper, but some of the principles studied here apply to transmitters as well.

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## II. Signal Path Design

For architecture and circuit design purposes, we can identify three broad categories of challenges: signal path design, carrier generation, and spectrum sensing. We address these challenges in this and following sections.

The receive signal path of a cognitive radio must deal with two issues: (1) broadband characteristics, i.e., a relatively flat noise figure (NF) and gain, and adequate input matching across two to three decades; (2) nonlinearity and local oscillator (LO) harmonics.

### A. Low-Noise Amplifier Issues

The broadband behavior of receivers is primarily determined by the front-end low-noise amplifier. As such, the LNA may appear as an extension of its counterparts in UWB or software-defined radios. Fig. 1 depicts several LNA candidates providing wideband input matching.

The CG stage of Fig. 1(a) suffers from a relatively high noise figure. If channel-length modulation and body effect are neglected and $1/g_{m1} = R_S$, then [6]

$$\mathrm{NF} = 1 + \gamma + \gamma g_{m2} R_S + \frac{4R_S}{R_D} \tag{1}$$

where $\gamma$ denotes the excess noise coefficient of MOSFETs. With a limited voltage headroom, the third and fourth terms in (1) may not be negligible.[1] Another issue in the circuit of Fig. 1(a) is that, in deep-submicron technologies, the output resistance of $M_1$ creates a tight relationship between the input resistance and the voltage gain, leading to

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{(g_m + g_{mb})r_O + 1}{2(1 + r_O/R_D)} \tag{2}$$

if $R_{\mathrm{in}} = R_S$ [5]. In a typical design, it is likely that $R_D < r_O$, yielding a voltage gain, $V_{\mathrm{out}}/V_{\mathrm{in}}$, on the order of $[(g_m + g_{mb})r_O + 1]/4$, roughly one-fourth of the transistor's intrinsic gain. This drawback can be remedied through the addition of a cascode device but at the cost of voltage headroom.

In the resistive-feedback stage of Fig. 1(b), if the output resistance of $M_1$ and $M_2$ is taken into account, then

$$R_{\mathrm{in}} = \frac{R_{\mathrm{out}} + R_F}{1 + G_m R_{\mathrm{out}}} \tag{3}$$

where $R_{\mathrm{out}} = r_{O1} \| r_{O2}$ and $G_m = g_{m1} + g_{m2}$. With the input matched

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{R_{\mathrm{out}}(1 - G_m R_F)}{2R_S(1 + G_m R_{\mathrm{out}})}. \tag{4}$$

[1]The maximum value of $R_D$ is typically set by the voltage headroom rather than bandwidth because the latter can be enhanced by inductive peaking.

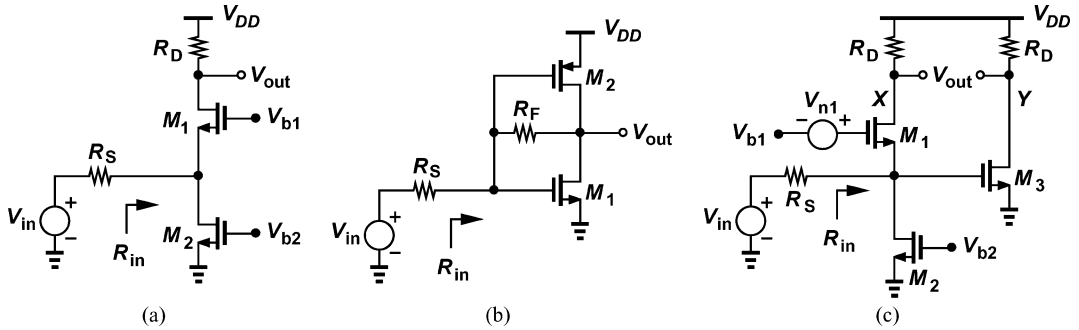



Fig. 1. (a) CG LNA, (b) resistive-feedback LNA, (c) noise-cancelling LNA.

We recognize from (3) that for $R_{\rm in} = 50\ \Omega$, $R_{\rm out} + R_F$ must remain below roughly 500 $\Omega$ if $G_m R_{\rm out} \approx 10$. If each of $R_{\rm out}$ and $R_F$ is less than several hundred ohms, i.e., if $G_m R_F$ is also on the order of 10, then the voltage gain expressed by (4) hardly exceeds 3.

In the composite common-gate/common-source stage of Fig. 1(c) [7], $M_1$ provides input matching (subject to the above limitations for the CG stage) and $M_3$, signal inversion. More importantly, since the noise of $M_1$, $V_{n1}$, is inverted by both $M_1$ and $M_3$, it can be *cancelled* at the output [7], [9]. This occurs if $g_{m3}R_S = 1$, making the noise of $M_3$ dominant and yielding

$$\text{NF} = 1 + \gamma + \gamma g_{m2} R_S + \frac{2R_S}{R_D} \tag{5}$$

if $M_3$ and $M_1$ are identical. This value is only slightly lower than the NF of the CG stage [(1)].[2]

Illustrated in Fig. 2, the principle of noise-cancelling LNAs faces two issues for decades-wide operation. (1) Relying on phase and gain matching between the two paths from $X$ and $Y$ to the output in Fig. 2, noise cancellation loses its efficacy at high frequencies. For example, the noise figure of the 65-nm design in [7] [similar to the circuit of Fig. 1(c)] exceeds 6 dB at $f > 7$ GHz—possibly because $C_{GD3}$ alters the phase at $Y$ at high frequencies. Similarly, the NF of the design in [8] rises to 5.5 dB at 7 GHz. (2) For noise cancellation to be advantageous, the auxiliary amplifier in Fig. 2 must contribute negligible noise. If enforced, this rule would require a wide transistor at the auxiliary amplifier input, inevitably leading to a low $|S_{11}|$ at high frequencies. For example, the $|S_{11}|$ of the designs in [7] and [8] falls below 10 dB at $f > 7$ GHz. The second issue becomes particularly serious in cognitive radios because the *flicker* noise of the auxiliary amplifier input transistor dominates at low frequencies. In 65-nm technology, a transistor with $W/L = 20\ \mu$m/60 nm and $I_D = 2$ mA exhibits a gate-referred noise voltage of 0.8 $\text{nV}/\sqrt{\text{Hz}}$ (corresponding to an NF of 2.5 dB) at gigahertz frequencies but 1.25 $\text{nV}/\sqrt{\text{Hz}}$ (corresponding to an NF of 4.6 dB) at 50 MHz. In fact, for a device to produce negligible flicker noise at 50 MHz, its gate area must reach 12 $\mu\text{m}^2$, presenting an input capacitance of about 200 fF.

[2]To obtain a lower noise figure, $M_3$ can be chosen to have a higher transconductance [7], [9], [10] (with a proportionally smaller drain resistance) but at the cost of a higher input capacitance.

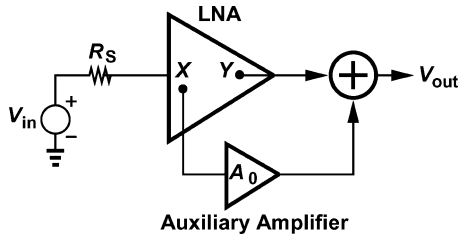



Fig. 2. Principle of noise cancellation.

### B. Proposed LNA

This paper introduces an LNA topology that inherently cancels the effect of its own input capacitance, thereby achieving a more favorable trade-off between the input matching, the noise figure, and the bandwidth than that of the prior art. Illustrated in Fig. 3(a), the idea is to exploit the inductive input impedance of a negative-feedback amplifier so as to cancel the input capacitance, $C_{\rm in}$. If the open-loop transfer function of the core amplifier is modeled by a one-pole response, $A_0/(1+s/\omega_0)$, then the input admittance is given by

$$Y_1(s) = \frac{s + (A_0+1)\omega_0}{R_F(s+\omega_0)}. \tag{6}$$

It follows that

$$\frac{1}{Re\{Y_1\}} = \frac{R_F\left(\omega^2+\omega_0^2\right)}{(1+A_0)\omega_0^2} \tag{7}$$

$$Im\{Y_1\} = \frac{-A_0\omega\omega_0}{R_F\left(\omega^2+\omega_0^2\right)}. \tag{8}$$

At frequencies well below $\omega_0$, $1/Re\{Y_1\}$ reduces to $R_F/(1+A_0)$, which can be set equal to $R_S$, and $Im\{Y_1\}$ is roughly $-A_0\omega/(R_F\omega_0)$, which can be chosen to cancel $C_{\rm in}\omega$. Fig. 3(b) illustrates the behavior of $1/Re\{Y_1\}$ and $-Im\{Y_1\}$.

The input matching afforded by the above technique holds for frequencies up to about $\omega_0$, dictating that the open-loop bandwidth of the core amplifier reach 10 GHz for CR applications. The intrinsic speed of 65-nm devices provides the gain and bandwidth required here. Note that prior work on resistive-feedback LNAs evidently has not exploited or recognized this cancellation property [9], [11].

The foregoing analysis raises two issues. First, both the real and the imaginary parts of $Y_1$ vary with process and temperature. Second, a multi-stage core amplifier may not follow a

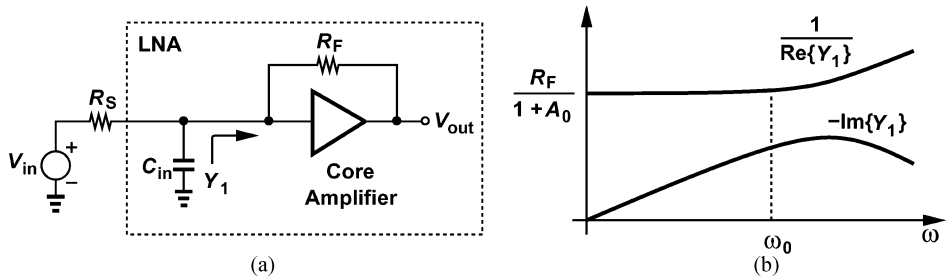



Fig. 3. (a) Proposed LNA topology, (b) behavior of components of $Y_1$ with frequency.

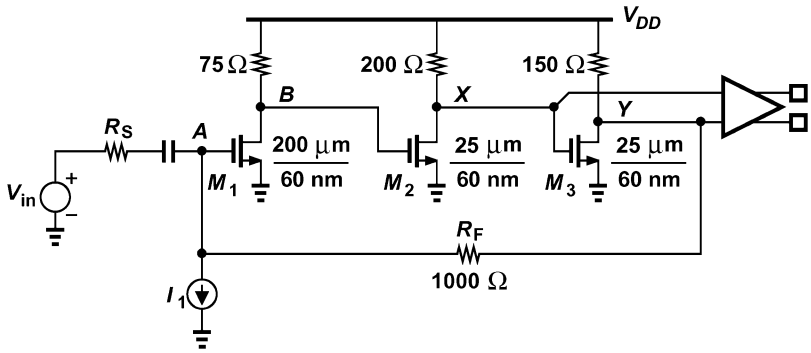



Fig. 4. Implementation of proposed LNA.

one-pole response, exhibiting a more complex cancellation behavior. We address these issues below.

Fig. 4 shows the circuit realization of the amplifier concept. Three common-source stages provide gain and allow negative feedback. Cascodes and source followers are avoided to save voltage headroom. The input transistor, $M_1$, has a large width commensurate with flicker noise requirements at 50 MHz, thus operating with a $V_{GS}$ of about 200 mV. If this voltage also appears at node $Y$, it leaves no headroom for output swings, limiting the linearity of the circuit. To resolve this issue, current $I_1$ is drawn from $R_F$ so as to shift up the quiescent voltage at $Y$ by approximately 250 mV. Since $R_F = 1$ k$\Omega$, $I_1$ need be only 200 $\mu$A, contributing negligible noise at the LNA input.[3]

With three gain stages, the LNA can potentially suffer from a small phase margin and exhibit substantial peaking in its frequency response. In this design, the open-loop poles at nodes $A$, $B$, $X$, and $Y$ lie at 10 GHz, 24.5 GHz, 22 GHz, and 75 GHz, respectively, creating a great deal of phase shift. Nonetheless, due to the small feedback factor, $R_S/(R_S + R_F) = 0.048$, simulations indicate that the circuit provides a phase margin of about 50° and a peaking of 1 dB in its closed-loop frequency response.

The multi-pole LNA of Fig. 4 contains an inductive component in its input impedance but with a behavior more complex than the above analysis suggests. Fortunately, behavioral simulations confirm that, if the poles at $B$, $X$ and $Y$ are "lumped" (by a zero-value time constant technique), then the one-pole approximation still predicts the input admittance accurately. The pole frequencies mentioned above collapse to an equivalent value of $\omega_0 = 2\pi$ (9.9 GHz), suggesting that the real and imaginary parts of $Y_1$ retain the desired behavior up to the edge of the cognitive radio band.

The LNA output is sensed between nodes $X$ and $Y$. Even though these nodes provide somewhat unequal swings and a phase difference slightly greater than 180°, the pseudo-differential sensing still increases both the gain and the $IP_2$, the latter because second-order distortion at $X$ also appears at $Y$ and is thus partially cancelled in $V_Y - V_X$.[4]

The dependence of the input matching upon process and temperature plagues most wideband LNA topologies. For example, in all of the structures of Fig. 1, $S_{11}$ depends on $g_{m1}$. In the proposed LNA, the dependence of $Re\{Y_1\}$ and $Im\{Y_1\}$ upon $A_0$ and $\omega_0$ may lead to poor input matching at the extremes of process and temperature. Simulations of the circuit in Fig. 4 reveal that the worst-case scenario occurs at the slow-slow, 75° corner with resistors 15% higher than their nominal value. At this corner and at 10 GHz, $|S_{11}|$ is around 10 dB and the phase margin around 45°.

To facilitate the testing of the LNA, two versions of the circuit have been implemented, one with a low-noise 50-$\Omega$ buffer for NF measurements [Fig. 5(a)] and another with a linear 50-$\Omega$ buffer for $IP_2$ and $IP_3$ measurements [Fig. 5(b)]. The former buffer has a voltage gain of about unity, and the latter, about $-10$ dB.

### C. Even-Order Nonlinearity

In this section, it is argued that the LNA—rather than the mixer—may become the $IP_2$ bottleneck in CRs. The effect of

[3]Alternatively, capacitive coupling can be used in the feedback path. But the large value necessary for the capacitor would introduce additional parasitics.

[4]To ensure stability in the presence of package parasitics, a capacitor of 10–20 pF must be placed between $V_{DD}$ and GND. Also, a small ESD device capacitance can be absorbed at the input.

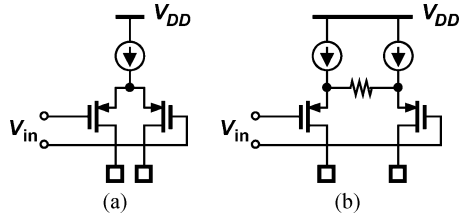



Fig. 5. (a) Low-noise and (b) linear buffers following the LNA.

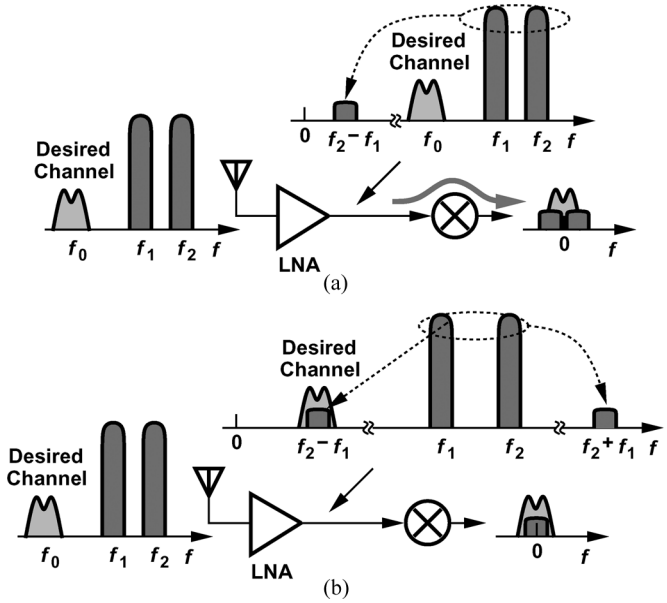



Fig. 6. Effect of even-order distortion in (a) narrowband and (b) broadband receivers.

even-order distortion becomes much more serious in cognitive radios than in narrowband RF receivers. As shown in Fig. 6(a) for a narrowband system, two interferers at $f_1$ and $f_2$ produce a low-frequency component. In the presence of asymmetries in the downconversion mixer(s) and the local oscillator waveform, a fraction of this component leaks to the baseband output, falling atop the desired channel. In this case, only the mixer limits the $IP_2$ because ac coupling of the LNA output can remove its low-frequency beats. The $IP_2$ of most receivers is therefore measured according to this scenario, and significant effort has been expended on improving the $IP_2$ of mixers [12], [13].

The problem of even-order nonlinearity assumes new dimensions in cognitive radios. As depicted in Fig. 6(b), the second-order IM products generated by the LNA itself can fall within the CR band, corrupting the desired signal even before downconversion. In this scenario, the LNA becomes the nonlinearity bottleneck. A differential topology seems attractive here, but, if the antenna is single-ended, a balun becomes necessary. Design of low-loss baluns operating across two or three decades of bandwidth presents its own challenges, but the LNA topology of Fig. 1(c) [7] proves useful here.

Since wideband LNAs suffer from both second-order and third-order nonlinearity, it is useful to have a measure indicating which of the two mechanisms limits the performance in a given signal range. Such a measure would help decide whether $IP_2$ or $IP_3$ is chosen conservatively, and which one of the two must be improved. As illustrated in Fig. 7, a "corner" level, $P_c$, can be defined as the intercept point of the output $IM_2$ and $IM_3$ plots. We may say the circuit is $IM_2$-limited for $P_{\rm in} < P_c$ and $IM_3$-limited for $P_{\rm in} > P_c$. It can be shown [5] that

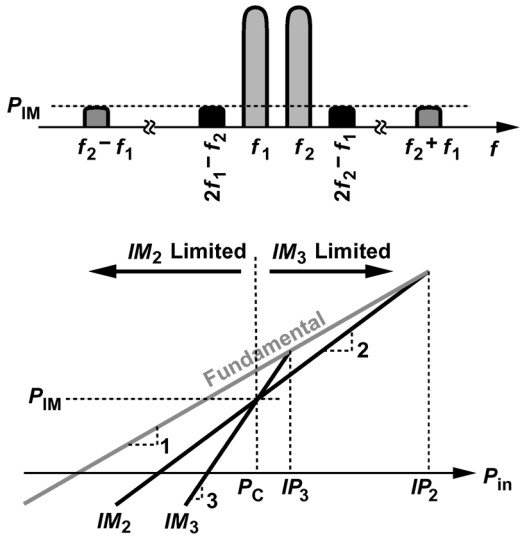



Fig. 7. Definition of "corner" input power level, $P_C$.

$$P_c = 2IP_3 - IP_2 \tag{9}$$

where all quantities are expressed in dBm.

### D. LO Harmonics

Mixers optimized for noise and gain typically exhibit sharp nonlinearity in their LO port, equivalently mixing the RF input with a square wave even if the LO waveform is a sinusoid. Thus, interferers located at the LO harmonics are downconverted to the baseband.

With a decades-wide LNA bandwidth, harmonic orders up to several tens or hundreds may prove problematic. For example, if the desired signal lies at 100 MHz, the 100-th harmonic of the LO—which is only 40 dB lower than the first harmonic[5] —readily downconverts an interferer at 10 GHz. By contrast, a radio targeting the range of 900 MHz to 5 GHz (cellular to WLAN bands) must deal with harmonics up to the fifth or sixth order. For this reason, such radios have focused on harmonic-reject mixers (HRMs) [14]–[16] derived from the original concept in [17].

Cognitive radios do not easily lend themselves to harmonic-reject mixing. Even for the third and fifth harmonics, three sets of differential LO phases must be generated and distributed, a difficult task as $f_{LO}$ approaches a few gigahertz (the maximum $f_{LO}$ whose harmonics prove troublesome). Additionally, HRMs become much more complex if seventh and higher LO harmonics must be rejected. Also, HRMs do not cancel "stray" components, e.g., those coupled through the supply line (Section IV-B).

[5]In practice, the switching within the mixer is not completely abrupt, making this estimate pessimistic.

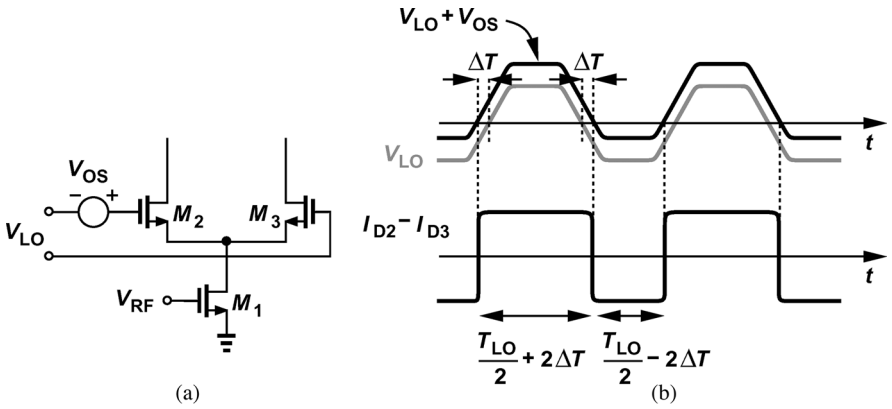



Fig. 8. (a) Mixer with offset voltage, (b) second harmonic due to offset.

Perhaps the most serious shortcoming of HRMs is that they do not remove *even* LO harmonics. Arising from random asymmetries in the mixers and LO waveforms, these harmonics can assume significant strength. As an example, consider the single-balanced mixer of Fig. 8(a), where $V_{OS}$ denotes the $V_{GS}$ mismatch between $M_2$ and $M_3$. As depicted in Fig. 8(b), the vertical shift in the LO waveform due to $V_{OS}$ distorts the duty cycle of the switching of $M_2$ and $M_3$, creating a second LO harmonic. This can be readily seen by setting the RF signal swing to zero, assuming that $M_2$ and $M_3$ switch abruptly, and examining the differential output current. To compute the second harmonic amplitude, we assume $V_{LO}(t) = V_P \sin \omega_{LO} t$ and note that each zero crossing in $V_{LO}(t) + V_{OS}$ is displaced by

$$\Delta T = V_{OS} \left( \left. \frac{dV_{LO}}{dt} \right|_{max} \right)^{-1} \tag{10}$$

$$= \frac{V_{OS}}{V_P \omega_{LO}}. \tag{11}$$

Thus, the differential current, $I_{D2} - I_{D3}$, remains high for $T_{LO}/2 + 2\Delta T$ seconds and low for $T_{LO}/2 - 2\Delta T$ seconds. The amplitude of the second harmonic of this waveform can be determined from its Fourier series and normalized to the amplitude of the fundamental, yielding

$$\frac{V_{2LO}}{V_{LO}} \approx \frac{V_{OS}}{V_P}. \tag{12}$$

For example, if $V_{OS} = 5$ mV and $V_P = 400$ mV, then the second harmonic is only 38 dB below the fundamental. Note that this effect persists even in a fully-differential RF signal path.[6]

The problem of LO harmonics (and intermodulation) may also be tackled at the network level. The spectrum sensing capability of cognitive radios can provide a snapshot of a wide range of frequencies, revealing the large interferers. The receiver may then simply avoid communication in channels that are potentially corrupted by these interferers. Such "wasteful" usage is not possible in narrowband systems if users must readily access the network but it becomes practical by virtue of the decades-wide bandwidth of CRs.

[6]At lower frequencies, e.g., as in [15] and [16], it is possible to sharpen the clock edges and reduce the second harmonic.

## III. Carrier Generation

### A. General Considerations

The generation of carrier frequencies proves difficult in CRs because they seek operation at any frequency in the band up to 10 GHz. Carrier synthesis for CRs entails the following principles:

1) The carrier must be produced in quadrature form (if a direct-conversion architecture is used and the signal has asymmetric modulation). The loss and limited bandwidth of polyphase filters makes them a poor choice for this task. That is, oscillators and dividers having quadrature outputs are preferred.
2) If a higher frequency is generated and subsequently divided to provide the carrier frequency of interest, then the speed limitations of the circuits must be taken into account. For example, as a rough rule of thumb, a node running faster than 20 GHz in 65-nm technology requires inductive peaking, leading to a complex layout and difficult routing.
3) Due to its large spurious content, SSB mixing must be avoided. Mixer mismatches and nonlinearities yield spurs that lie only 30 to 40 dB below the desired output.
4) The trade-offs between the phase noise, tuning range, center frequency, and power dissipation of *LC* oscillators typically limit the tuning range to about $\pm 15\%$ at frequencies of tens of gigahertz if a phase noise commensurate with cellular and WLAN standards must be achieved.
5) The above constraint may point to oscillator multiplexing so as to cover a wide range. However, the use of multiple inductors complicates the routing (Section IV-B) and increases the area.
6) Except for a particular case described below, division of a frequency by an odd number yields a non-50% duty cycle at the output. Thus, the result must be further divided by 4 to generate balanced quadrature phases.

### B. Examples

It is possible to perform carrier synthesis for a range of $f_1$ to $10f_1$ using a single oscillator running at $80f_1$ and a number of divider chains [5]. However, such an architecture places a heavy burden on the oscillator and the first rank of dividers. For example, if $f_1 = 10$ GHz, these building blocks must operate

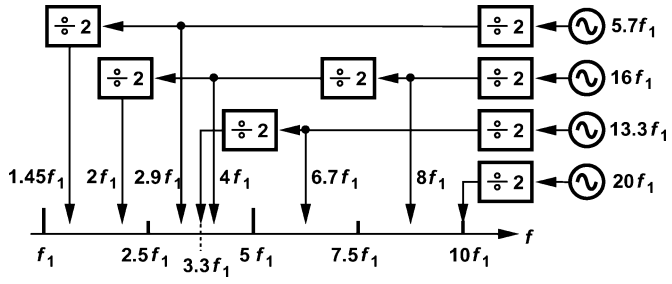



Fig. 9. Wideband synthesis using multiple LOs.

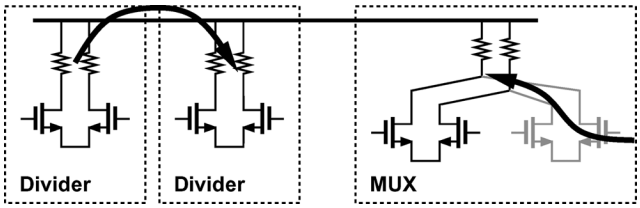



Fig. 10. Leakage through supply line and through MUX.

at 80 GHz. Fortunately, recent work on millimeter-wave CMOS circuits has demonstrated these capabilities [18]–[20]. For example, differential oscillators and ÷2 circuits operating up to about 128 GHz have been reported in 90-nm CMOS technology [20]. Nonetheless, the architecture demands the use of inductors at many of the nodes.

The high-frequency issues can be greatly alleviated if more than one oscillator is utilized. Fig. 9 depicts an example, where four oscillators operating at $5.7f_1$, $16f_1$, $13.3f_1$, and $20f_1$ are used. The fourfold reduction in the maximum oscillation and division frequencies comes at the cost of more complex, yet feasible routing.[7]

Another important and general issue that emerges from the above example is the supply coupling within divider chains. For example, if the chain producing $2f_1$ in Fig. 9 is enabled and the dividers in the chain share the same supply line, then the $4f_1$ component leaks to the $2f_1$ output. Fully-differential implementations and symmetric layouts can reduce this coupling, but perhaps not to a negligible level. A similar leakage arises in the multiplexer (MUX) that selects one of the frequencies produced by each chain: even though only one path in the MUX is enabled, the other paths' parasitic capacitances couple a fraction of the other frequencies to the output. Illustrated in Fig. 10, such leakages prove troublesome in harmonic-reject mixers.

[7]To generate quadrature phases at $10f_1$, either a $20f_1$ (differential) oscillator or a $10f_1$ quadrature oscillator is necessary. The phase noise-power trade-offs are comparable for $10f_1 \leq 10$ GHz.

### C. A Prototype

In order to arrive at another carrier synthesis approach, let us consider a quadrature *LC* oscillator followed by an inductively-loaded buffer [Fig. 11(a)]. (The need for a quadrature oscillator is explained below.) Due to the large footprint of the inductors, the routing of the signal to subsequent stages (e.g., dividers) must deal with long interconnects. We may therefore "nest" the buffer inductors within the oscillator inductors [Fig. 11(b)].[8] The subsequent stages can now be placed close to the oscillator and buffer transistors, but the mutual coupling between the nested inductors must be taken into account. Fig. 11(c) depicts the corresponding circuit representation, omitting for clarity the differential pairs that couple the two oscillators.

In addition to a more compact layout, the nesting of inductors offers another important property: the mutual coupling permits "bimodal" operation of the oscillator. First reported in [4], the oscillator in Fig. 11 resembles that described later in [21]. However, the following discussion will reveal two points that are evidently not recognized by [21]. (1) The oscillation frequency can be switched by flipping the *polarity* of the mutual coupling. (2) A one-port analysis of the circuit without the cross-coupled pair but with the output transistors can yield the oscillation frequencies and the startup condition.

That is, the oscillation frequency can be changed by changing the *polarity* of the coupling between the core and the buffer [4]. In order to study this property, we consider one of the two oscillators in Fig. 11(c) and simplify it to the circuit shown in Fig. 12(a). Here, $L_1$ and $C_1$ represent the load of the cross-coupled pair, and $L_2$ and $C_2$ the load of the buffer transistors. Resistance $R_2$ models the loss of the buffer tank, and voltage-dependent current source $G_m V_1$ denotes the action of the buffer transistors. The loss of the first tank is excluded for now and is taken into account below.

The circuit of Fig. 12(a) oscillates if the impedance $Z_{\text{in}}$ goes to infinity at an imaginary frequency. We have equation (13), shown at the bottom of the page. For $Z_{\text{in}}$ to go to infinity, both the real and imaginary parts of the denominator must be set to zero:

$$(L_1L_2 - M^2)C_1C_2\omega^4 - (L_1C_1 + L_2C_2)\omega^2 + 1 = 0 \quad (14)$$

$$\frac{L_1L_2 - M^2}{R_2}C_1\omega^2 - \left(\frac{L_2}{R_2} - G_{m2}M\right) = 0. \quad (15)$$

[8]Field simulations indicate a negligible effect on the Q due to nesting. However, since the inner inductor must have a smaller diameter, its Q is about 10% lower than the outer inductor.

$$Z_{\text{in}} = \frac{(L_1L_2 - M^2)C_2s^3 + \frac{L_1L_2 - M^2}{R_2}s^2 + L_1s}{(L_1L_2 - M^2)C_1C_2s^4 + \frac{L_1L_2 - M^2}{R_2}C_1s^3 + (L_1C_1 + L_2C_2)s^2 + \left(\frac{L_2}{R_2} - G_{m2}M\right)s + 1}. \quad (13)$$

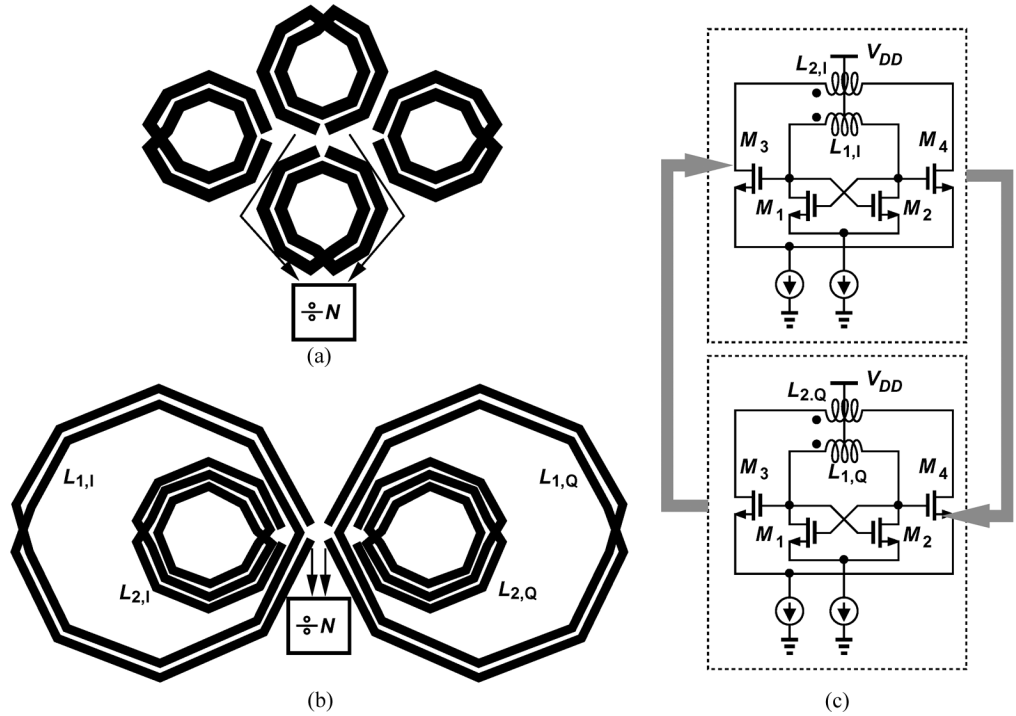



Fig. 11. (a) Layout of a quadrature oscillator with buffers, (b) simplified layout using nested inductors, (c) quadrature oscillator with mutual coupling. (Gray arrows denote the antiphase coupling required for quadrature operation.)

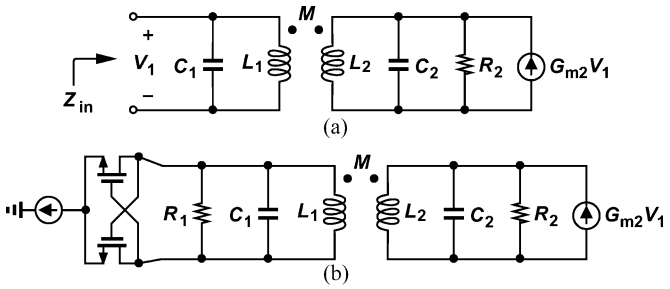



Fig. 12. (a) Simplified circuit of oscillator with mutual coupling, (b) addition of cross-coupled pair and loss of first tank.

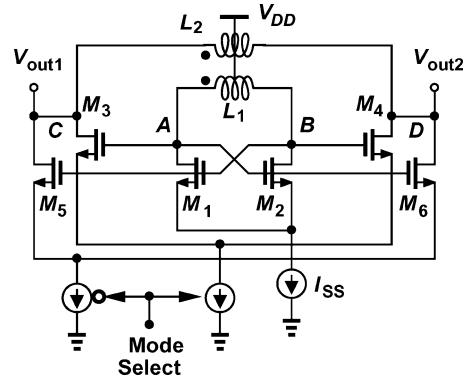



Fig. 13. Oscillator with negative and positive coupling from output buffer.

The first equation yields the oscillation frequencies:

$$\omega_{1,2}^2 = \frac{L_1C_1+L_2C_2 \pm \sqrt{(L_1C_1+L_2C_2)^2-4(L_1L_2-M^2)C_1C_2}}{2(L_1L_2-M^2)C_1C_2} \tag{16}$$

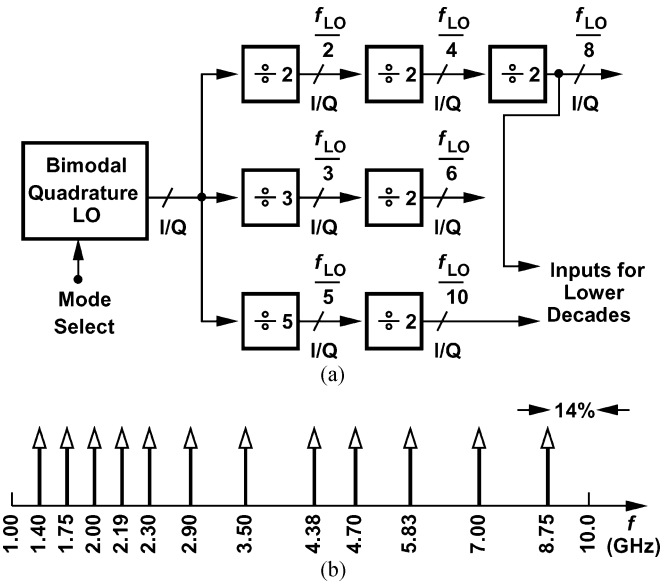



Fig. 14. (a) Wideband carrier synthesis architecture, (b) output frequencies.

and the second, the oscillation startup condition:

$$G_{m2} = \frac{L_1L_2 - M^2}{R_2M}\omega_{1,2}^2 - \frac{L_2}{R_2M}. \tag{17}$$

If $L_1 = L_2 = L$ and $C_1 = C_2 = C$ (as is approximately the case in the prototype), then,

$$\omega_1^2 = \frac{1}{(L+M)C},\ G_{m2,1} = +\frac{1}{R_2} \tag{18}$$

$$\omega_2^2 = \frac{1}{(L-M)C},\ G_{m2,1} = -\frac{1}{R_2}. \tag{19}$$

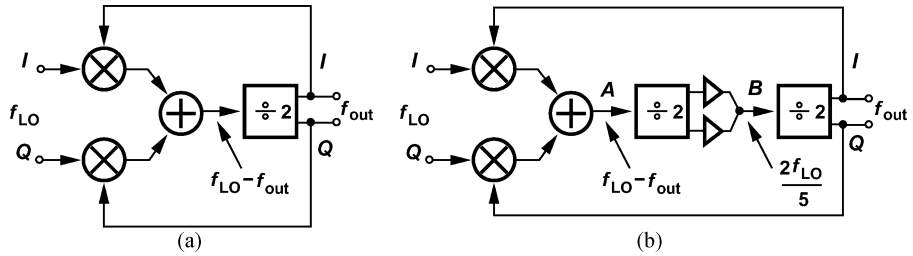



Fig. 15. Realization of (a) ÷3 and (b) ÷5 circuits.

In other words, the circuit can oscillate at one of two frequencies depending on the polarity of $G_{m2}$ (or $M$).

In addition to $G_{m2}$ (the buffer), the oscillator contains two cross-coupled transistors. We can view these devices as providing a negative resistance that cancels the loss of the *first* tank [Fig. 12(b)]. While not essential to the operation, this partitioning allows the oscillator to be analyzed as a one-port system, readily providing the startup condition and predicting that the change in the polarity of $G_{m2}$ changes the frequency. By contrast, the analysis in [21] does not appear to have recognized these properties. Fig. 13 depicts the arrangement used in this work to change the polarity of $G_{m2}$.

The bimodal quadrature oscillator developed above permits an alternative approach to multi-decade carrier synthesis. Depicted in Fig. 14(a) [4], this approach drives three divider chains by a quadrature *LC* oscillator operating at one of two frequencies (e.g., 17.5 GHz and 14 GHz). Note that all of the outputs are produced in quadrature form. Fig. 14(b) shows the frequencies generated in the prototype, indicating a worst-case tuning range of $(10\text{ GHz} - 8.75\text{ GHz})/8.75\text{ GHz} = 14\%$. Also, lower decades can be generated by repeating this architecture with $f_{LO}/8$ and $f_{LO}/10$ serving as the inputs.

The architecture of Fig. 14(a) satisfies the first five of the six broadband synthesis principles described above. The simplicity of the architecture stems from both the bimodal operation of the oscillator and the ability of each divider to generate quadrature outputs, an exception to the sixth principle. In order for the odd-ratio dividers to provide quadrature outputs, this work employs the Miller divider concept proposed in [22]. Fig. 15 shows the ÷3 and ÷5 circuit implementations. In Fig. 15(a), an SSB mixer and a ÷2 stage form a Miller divider, reaching stable operation if $(f_{LO} - f_{\text{out}})/2 = f_{\text{out}}$ and hence $f_{\text{out}} = f_{LO}/3$. Similarly, the divider of Fig. 15(b) incorporates an SSB mixer and a cascade of two ÷2 circuits, generating $f_{LO} - f_{LO}/5$ at $A$, $2f_{LO}/5$ at $B$, and $f_{LO}/5$ at the output. We recognize the need for quadrature LO inputs in these divider topologies.

In this work, the SSB mixer is realized as shown in Fig. 16. Since the common-mode level of the LO is near $V_{\text{DD}}$ (Fig. 13), nMOS switches sense the LO phases at their gates and the ÷2 outputs at their sources. The large LO swings allow the use of relatively small switches ($W/L = 2.5\ \mu\text{m}/0.1\ \mu\text{m}$). The differential pairs provide voltage gain and sufficient swings for the following ÷2 stage. The ÷2 circuits are based on conventional current-mode flipflops.

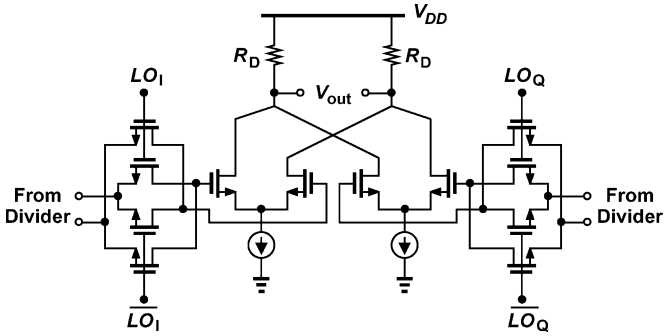



Fig. 16. SSB mixer used in dividers.

The use of SSB mixers in the foregoing dividers may appear to violate the third synthesis principle stated above. To investigate this point, we study the ÷5 circuit of Fig. 15(b) while considering the effect of two mixer imperfections, namely, I/Q mismatches and LO or RF feedthrough. As illustrated in Fig. 17(a), the unwanted sideband due to mismatches appears at $6f_{LO}/5$ at the SSB mixer output. The sideband can be viewed as the sum of AM and FM components located at $2f_{LO}/5$ and $6f_{LO}/5$. Upon experiencing the limiting action of the ÷2 input stage (a switching differential pair), the former are removed. The resulting FM waveform is then divided by 2, maintaining the sideband spacing and hence yielding sidebands at 0 and $4f_{LO}/5$ at $B$. The next ÷2 stage translates these sidebands to $\pm 3f_{LO}/5$, i.e., to the third *harmonic* of the desired output. We therefore observe that the spectra at node $B$ and at the output are free from mismatch-induced sidebands.

Now, let us consider the effect of LO feedthrough, shown in Fig. 17(b). The sideband at $f_{LO}$ results in FM components at $3f_{LO}/5$ and $f_{LO}$. The first divider thus produces sidebands at $f_{LO}/5$ and $3f_{LO}/5$, and the second translates these sidebands to 0 and $2f_{LO}/5$. In this case, the final output is still free from sidebands, but the waveform at node $B$ is not.

The above analysis reveals a serious drawback of quadrature Miller dividers realizing *fractional* ratios. For example, while node $B$ in Fig. 15(b) can be sensed as a nominal frequency equal to $f_{LO}/2.5$—as proposed in [22]—the LO feedthrough within the SSB mixer creates sidebands at this node. With typical LO feedthrough of roughly −40 dB, 6 dB of attenuation due to limiting, and 6 dB of reduction due to the first ÷2 operation, the sidebands at node $B$ may exhibit a relative level of about −50 to −55 dB, which is inadequate in many applications. In summary, such dividers provide spur-free waveforms only at outputs that are integer sub-multiples of the input frequency.

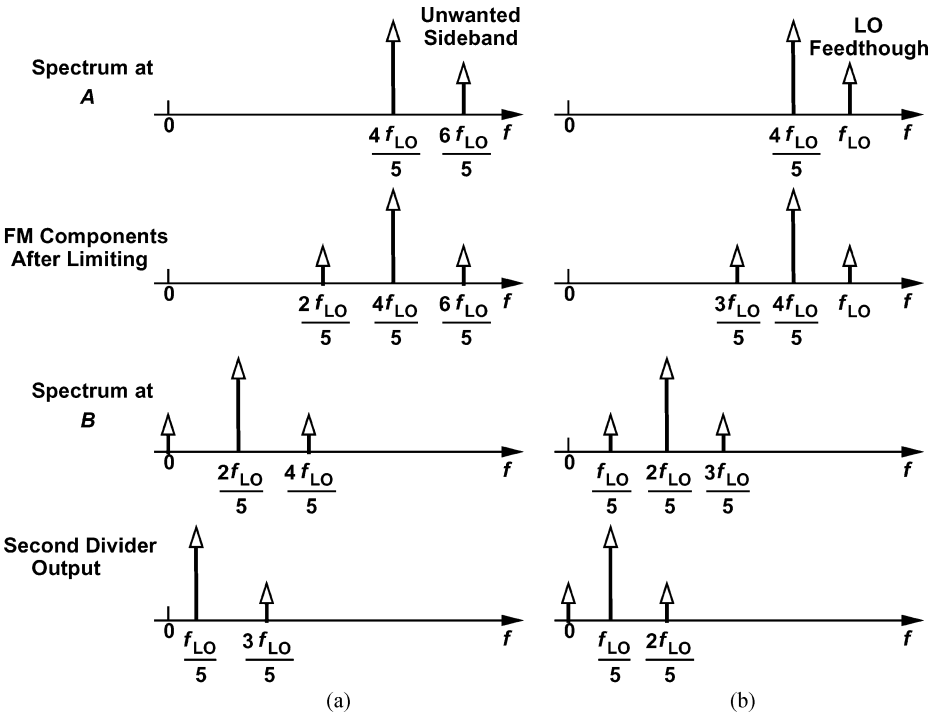



Fig. 17. Effect of (a) I/Q mismatch and (b) LO feedthrough on $\div 5$ circuit.

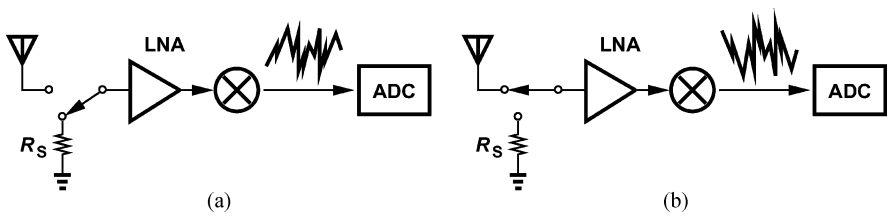



Fig. 18. (a) Receiver noise calibration, (b) energy detection.

## IV. Spectrum Sensing

The versatility of cognitive radios is derived from their ability to sense and detect available channels. To combat the "shadowing effect,", CRs must detect signal levels well *below* the sensitivities specified by wireless standards [5], [23]. In practice, a cognitive radio may define channel availability according to an SNR of $-15$ to $-20$ dB, whereas standards define the sensitivity with an SNR of $+8$ to $+25$ dB (depending on the modulation scheme).

Spectrum sensing has thus far been considered a task for only digital baseband processing, and various sensing algorithms have been developed. These algorithms, however, require a long time to detect an available channel with confidence. It is therefore desirable to seek the assistance of the receiver's RF and analog sections to speed up spectrum sensing.

### A. Sensing Techniques

Two techniques have shown promise for spectrum sensing: "energy detection" and "feature detection" [23]. Fig. 18 conceptually illustrates the principle of energy detection.[9] First, as shown in Fig. 18(a), the noise of the receiver itself is amplified, translated to the baseband, and digitized by the baseband analog-to-digital converter (ADC). This measurement assumes no input signal, dictating that the receiver input be disconnected from the antenna and tied to an equivalent source impedance. Next, as depicted in Fig. 18(b), the channel of interest is received, downconverted to the baseband along with the receiver noise, and measured by the ADC. If measured over a sufficiently long period of time, this energy exhibits a finite difference with respect to that obtained in Fig. 18(a), revealing the existence of a signal.

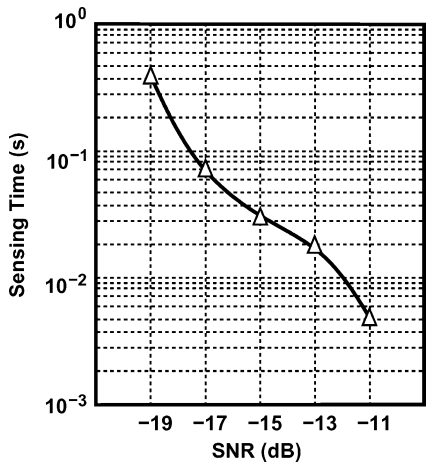



Fig. 19. Required sensing time for a 4-MHz channel.

[9] The receiver, of course, includes other basic functions such as automatic gain control, channel-selection filtering, etc.

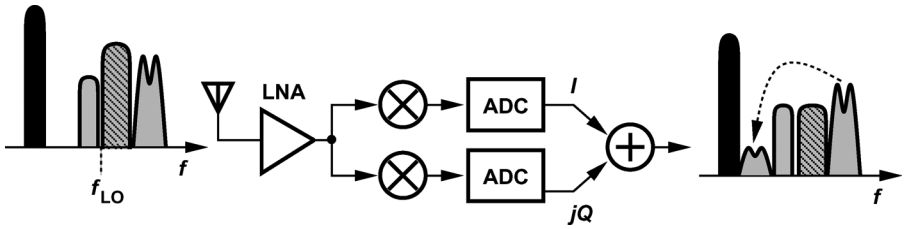
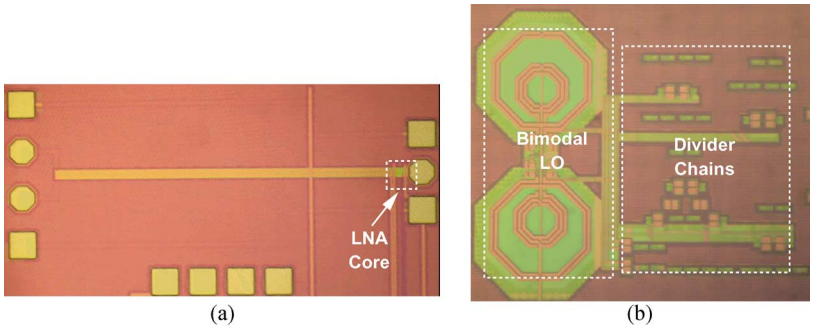



Fig. 20. Block downconversion.




(a) (b)

Fig. 21. Die photographs of (a) LNA and (b) carrier synthesis circuit.

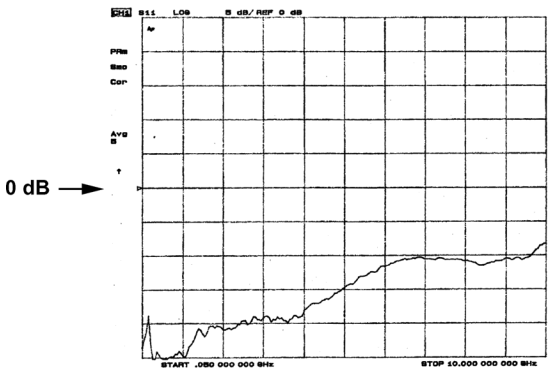



Fig. 22. Measured $S_{11}$ of LNA. (Horiz. scale: 1 GHz/div., vert. scale: 5 dB/div.)

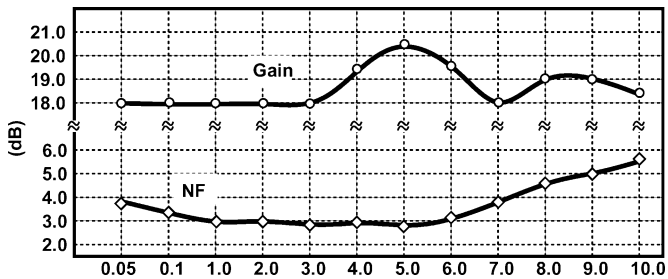



Fig. 23. Measured noise figure and voltage gain of LNA. (Nonlinear horizontal scale below 1 GHz.)

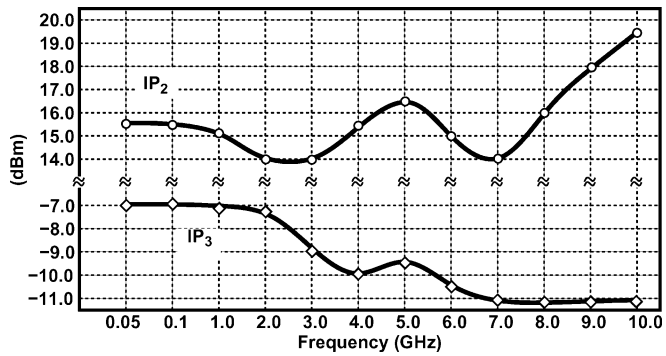



Fig. 24. Measured $IP_3$ and $IP_2$ of LNA. (Nonlinear horizontal scale below 1 GHz.)

Energy detection poses minimal burden on digital baseband processing but exacting requirements on the receive path. To understand this point, suppose the signal in the channel of interest has a power 15 dB below the noise, i.e., $P_{sig} = 0.0316P_{noise}$. Thus, the powers measured in Figs. 18(a) and (b) are equal to $P_{noise}$ and $1.0316P_{noise}$, respectively, demanding that the sensing resolve a 3.16% increase in the average power. This means that the drift in $P_{noise}$—at the ADC input—must remain well below this amount. For example, the noise and gain of the receive chain and the full-scale reference of the ADC must drift by much less than 3.16% from the measurement in Fig. 18(a) to that in Fig. 18(b), a daunting task for circuit design.

Energy detection also requires a long sensing time. As an example, Fig. 19 plots the sensing time for a 4-MHz channel as a function of the SNR [24]. Note that, for an SNR of, say, −15 dB, the sensing takes about 30 ms. Simple scaling of this value for a channel bandwidth of, say, 200 kHz, yields a sensing time of 0.6 s, suggesting an exceedingly slow operation if a CR must examine many channels before reaching an empty one.

The feature detection sensing method seeks certain "signatures" (periodic patterns) produced by modulation schemes [23]. This technique does not rely on accurate measurement of the receiver noise power, but it requires more complex digital processing. Furthermore, feature detection operates successfully only if the baseband ADC clock frequency tracks the symbol rate of the received signal, a difficult task. The sensing time in this case is roughly the same as that of energy detection.

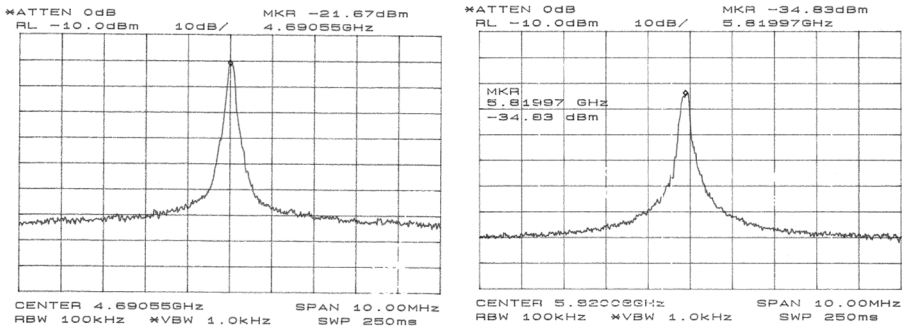



Fig. 25. Measured ÷3 outputs in the (a) low mode and (b) high mode.

### B. RF-Assisted Spectrum Sensing

A cognitive radio receiver can incorporate techniques that alleviate the sensing time problem. For example, a *block* of channels can be downconverted and the FFT of the entire block taken, thus raising the probability of finding an available channel proportionally.[10] Illustrated in Fig. 20, block downconversion places greater speed and resolution demands on the baseband ADCs and, more importantly, suffers from an image problem: if the baseband signal is constructed as $I + jQ$, then gain and phase mismatches allow a fraction of high-power channels to fall into the unoccupied channels.

The severity of this issue can be seen if we recall that the signal level in a channel of interest may be tens of decibels *below* typical receiver sensitivities, whereas the high-power channels may be 50 to 60 dB *above* the sensitivity. That is, the image rejection ratio (IRR) corresponding to $I$ and $Q$ mismatches must exceed 70 or 80 dB for the available channel to be detected properly. This level of IRR is difficult to achieve by calibration.

## V. Experimental Results

This section presents the experimental results for the LNA of Fig. 4 and the carrier synthesis circuit of Fig. 14(a). The circuits have been fabricated in 65-nm and 90-nm digital CMOS technologies, respectively. Fig. 21 shows the die photographs; the LNA occupies an active area of about $40\ \mu\text{m} \times 50\ \mu\text{m}$, and the synthesis circuit an active area of $530\ \mu\text{m} \times 550\ \mu\text{m}$. The prototypes have been tested on a probe station.

Fig. 22 plots the measured LNA $S_{11}$ from 50 MHz to 10 GHz. The high return loss at low frequencies implies that $R_F/(A_0 + 1)$ in Fig. 3(a) is close to 50 Ω. The $S_{11}$ remains below −10 dB for frequencies up to 9.6 GHz.

Plotted in Fig. 23 are the measured LNA noise figure and voltage gain. The peaking around 5 GHz is attributed to the inductance of the dc probes that provide the supply voltage to the chip.

Fig. 24 shows the measured LNA $IIP_3$ and $IIP_2$ with a tone spacing of 300 MHz. Table I compares the performance of the prototype with that of other published broadband CMOS LNAs.

[10]Note that the sensing time for a single channel is still long, but parallel processing of a block of channels—rather than serial sensing of channels—statistically reduces the time needed to arrive at an empty channel.

TABLE I
Comparison of LNA Performance

| | [7] | [9] | [23] | [24] | This Work |
|---|---|---|---|---|---|
| Bandwidth (GHz) | 0.2–5.2 | 0.5–8.2 | 3.1–10.6 | 2.7–4.5 | 0.05–10 |
| NF (dB) | 2.9–3.5 | 1.9–2.6 | 4.5–5.1 | 4.0–5.0 | 2.9–5.9 |
| $S_{11}$ (dB) | −12 | −7 | −11 | −7.5 | −10* |
| Gain (dB) | 13–16 | 22–25 | 9.8 | 18–19.6 | 18–20 |
| $IP_2$ (dBm) | >20 | NA | 10–20 | NA | 14–19.5 |
| $IP_3$ (dBm) (min/max) | >0 | −4/−16 | −6.2/−5 | −8 | −11.2/−7 |
| Power Diss. (mW) | 14 | 42 | 20 | 8 | 22 |
| CMOS Tech. | 65 nm | 90 nm | 0.18 um | 90 nm | 65 nm |

*For frequencies up to 9.6 Ghz.

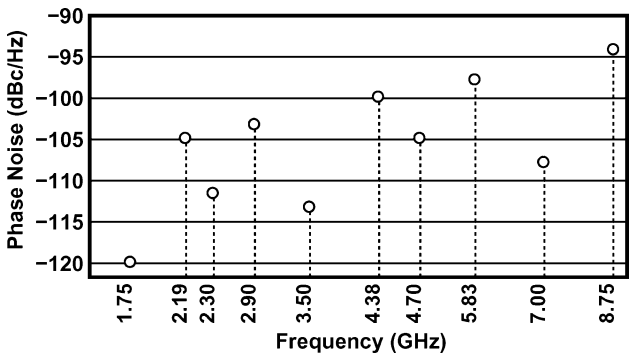



Fig. 26. Measured phase noise at 1-MHz offset.

The carrier synthesis circuit has been characterized by measuring the output spectrum (through an on-chip MUX) with the oscillator running at 14 GHz or 17.5 GHz. (Since the oscillator does not incorporate varactors in this prototype, only discrete frequencies are measured.) As an example, Fig. 25 shows the ÷3 output in the low mode and in the high mode.

Fig. 26 plots the measured phase noise of each output component at 1-MHz offset. (Due to an error in the MUX layout, the components at 1.4 GHz and 2 GHz are heavily attenuated, prohibiting a meaningful phase noise measurement.) The overall

circuit consumes the highest power (31 mW) when the top divider chain in Fig. 14(a) is enabled and the other two chains are disabled.

## VI. Conclusion

Cognitive radios present fertile grounds for research on RF transceiver and circuit design. The receive path must achieve decades-wide bandwidth with high linearity and adequate input matching while suppressing the effect of LO harmonics. The LO path must provide a carrier frequency spanning two or three decades. Also, the receiver architecture must be chosen to reduce the spectrum sensing time. This paper proposes a number of techniques that address some of these issues. An LNA topology is presented that cancels the input capacitance by means of inductive behavior provided by negative feedback. In addition, a carrier synthesis technique using a bimodal oscillator is described that can cover multiple decades. It is suggested that RF-assisted spectrum sensing by block downconversion can increase the probablity of finding an available channel.

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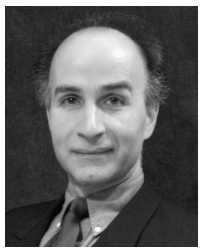


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