

# LO Generation Techniques for Millimeter-Wave Receivers

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**Abstract**—Millimeter-wave radios hold promise for supporting high data rates in wireless communication. A key challenge in the development of these radios relates to the generation of the local oscillator waveform(s) necessary for upconversion and downconversion. This paper presents a number of such techniques in the context of four receivers operating at 28 GHz, 140 GHz, and 300 GHz. The proposed concepts focus on fundamental-mode LO synthesis and high-speed inductorless frequency dividers. New methods of LO phase shifting for beamforming applications are also introduced. The prototypes have been fabricated in 28-nm CMOS technology and exhibit rms jitter values ranging from 106 fs to 640 fs.

**Index Terms**—Terahertz radios, millimeter-wave radios, PLLs, synthesizers, oscillators

## I. INTRODUCTION

Millimeter-wave (mm-wave) radios operating in the range of 30 GHz to 300 GHz prove attractive for wireless communication at high data rates. Considerable work in this area has advanced the field in the past decade [1]–[12], relying on beamforming arrays to overcome the high path loss. It has been recognized that power consumption and cost play a key role in the commercial success of such products.

Among the challenges facing mm-wave radios, local oscillator (LO) generation has been particularly difficult and power-hungry. This paper describes several LO generation schemes that have been incorporated in receivers (RXs) ranging from 28 GHz to 300 GHz, aiming to reduce the power [2], [3], [9], [11]. Realized in 28-nm CMOS technology, the prototypes exhibit LO jitter values from 106 fs<sub>rms</sub> to 640 fs<sub>rms</sub>. The techniques are equally applicable to transmitters as well.

Section II provides the background for this work, and Section III deals with phase noise and spur requirements. Section IV describes two methods in a 28-GHz direct-conversion RX environment. Sections V and VI present two other techniques for heterodyne receivers at 140 GHz and 300 GHz, respectively. Section VII summarizes the experimental results.

The simulation results reported in this paper correspond to post-layout extraction, including all of the parasitics. Inductors and long interconnects are modeled by Cadence's EMX or Ansoft's HFSS.

We should also remark that the prototypes described here have been developed over the course of several years and reflect how our thought process has evolved. That is, the design choices in one may appear different or in conflict with those in another.

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## II. GENERAL CONSIDERATIONS

The prior art has generally shied away from phase-locked loops (PLLs) that directly operate at mm-wave frequencies. Several reasons account for this reluctance. First, generation of quadrature LO phases (Q-Gen) at high frequencies is difficult. Typical topologies, e.g., quadrature voltage-controlled oscillators (QVCOs), divide-by-2 circuits, and polyphase filters, must deal with their own issues. Second, the quality factor ( $Q$ ) of varactors and programmable capacitors falls at higher frequencies, degrading the phase noise (PN) of VCOs. Third, the high-speed frequency dividers necessary for such PLLs require inductors and/or suffer from a narrow lock range, thus posing a risk to the entire system. Fourth, the *distribution* of quadrature LO phases also becomes problematic.

For these reasons, some mm-wave systems begin with a slower PLL and multiply its output frequency by doublers or triplers. Such stages, however, typically deliver only a single-ended output, requiring additional phase splitters for differential quadrature LO generation. Thus formed, these cascades incur a high loss and demand power-hungry inductively-peaked stages so as to deliver acceptable voltage swings to the downconversion mixers. For example, the 300-GHz RX in [13] uses an external 44-GHz LO and draws about 200 mW in its multiplier and buffer stages. Also, the D-band RX in [14] assumes an external 5.8-GHz LO and uses an on-chip PLL followed by frequency triplers, consuming 60 mW in this network. Moreover, the D-band RX in [15] drains 210 mW in its LO path. Similarly, the work in [16] draws 90 mW in its RX LO chain. Our work demonstrates that fundamental-mode LO generation achieves less power consumption despite the lower varactor  $Q$ .

Another critical issue in mm-wave RX design arises from the need for beamforming. Systems employing phase shift networks in the LO path face the high loss and large footprint of such circuits.

## III. PHASE NOISE AND SPUR REQUIREMENTS

In general RF receivers, the LO phase noise must satisfy two conditions: (1) minimal reciprocal mixing in the presence of a large blocker, and (2) minimal corruption of the desired signal constellation. The high path loss at mm-wave frequencies and the inevitable use of beamforming attenuate blockers significantly, making the second condition dominant. We must therefore determine how the integrated PN affects the bit error rate (BER).

A detailed treatment of this phenomenon is beyond the scope of this paper, but we intuitively expect that the LO's rms jitter should remain much less than the symbol period

for the highest data rate carried by the signal. For example, to support a data rate of 40 Gb/s, one can employ a 16QAM signal with a symbol period of 100 ps. In such a scenario, an rms jitter of 1 ps negligibly affects the BER, encouraging us to target values below this bound. For a detailed treatment, the reader is referred to [17] and [18].

The matter of reference spurs also assumes a different nature here from those in general RF receivers. While in the latter, spurs can downconvert blockers, in mm-wave receivers, the principal concern relates to how much a spur corrupts the desired signal itself. This is because, typically, the PLL reference frequency is less than half of the RF channel bandwidth. As illustrated in Fig. 1, a direct-conversion RX translates the desired signal spectrum to center frequencies equal to zero and  $\pm f_{REF}$ . Thus, the spur level need only be low enough to ensure the power in the two offset copies of the signal spectrum is negligible. For common modulation schemes, therefore, a spur level of  $-30$  dBc suffices.

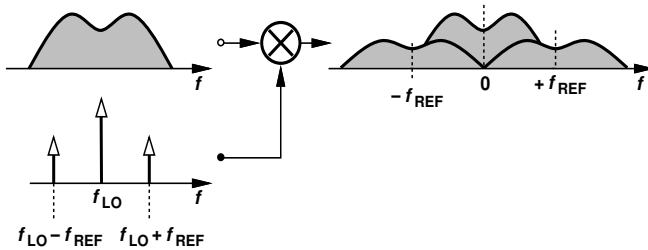


Fig. 1. Effect of LO spurs on desired signal.

#### IV. LO GENERATION FOR 28-GHz RADIOS

##### A. 56-GHz Synthesizer and $\div 2$ Stage

In the first generation of our 28-GHz direct-conversion system with eight beamforming elements, we opted for quadrature generation by frequency division [2], [19]. Such a scheme offers two advantages over QVCOs. First, it exhibits a more favorable PN-power trade-off than do QVCOs even though the  $\div 2$  circuit consumes 4.7 mW. Second, the 56-GHz differential VCO occupies a smaller footprint, lending itself to simpler integration within the beamforming array.

Depicted in Fig. 2, the integer-N synthesizer consists of a sampling phase detector (PD), a VCO, a  $\div 8$  prescaler, and a multimodulus divider (MMD). For greater flexibility in the overall system's floor planning, it was decided to place the Q-Gen circuit *outside* the synthesizer, as explained below.

Based on a complementary cross-coupled topology, the VCO incorporates a 50-pH inductor with three switched capacitors to achieve a total tuning range of 5 GHz while drawing 4.2 mW. The tank Q drops from 25 to 15 when all of the capacitors are switched into the circuit.

The design of the  $\div 8$  prescaler in Fig. 2 proves challenging in 28-nm technology, especially if it must avoid inductors so as to maintain a small footprint. Shown in Fig. 3(a) is the first  $\div 2$  stage [23], consisting of two dynamic latches ( $S_1$  and  $Inv_1$ , and  $S_2$  and  $Inv_2$ ) and a third inverter,  $Inv_3$ . To improve the performance, we introduce an unlocked feedforward path

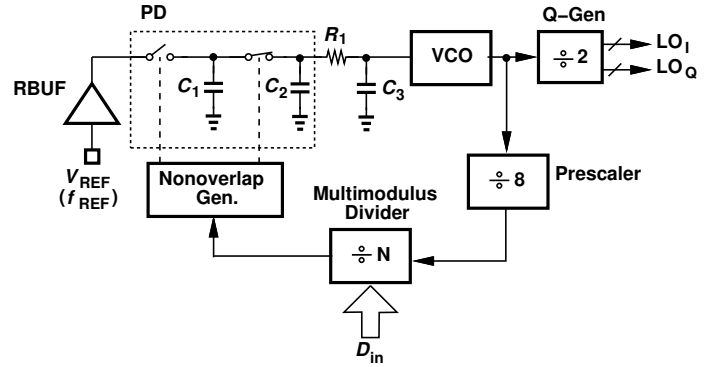
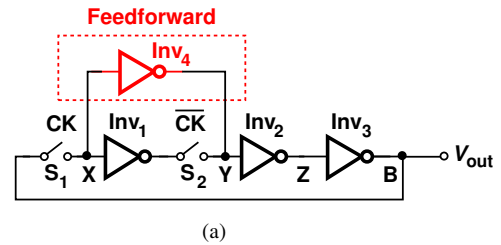


Fig. 2. PLL operating at 56 GHz and followed by a  $\div 2$  circuit.

from  $X$  to  $Y$  so that the signal partially bypasses  $Inv_1$  and  $S_2$ . The state arriving at  $Y$  thus initiates a change before  $S_2$  turns on.



(a)

| Process Corner | Input Freq. (GHz) |      |
|----------------|-------------------|------|
|                | Min.              | Max. |
| TT             | 43                | 68   |
| SS             | 37                | 59   |
| FF             | 53                | 78   |

(b)

Fig. 3. (a) Divider with feedforward path, and (b) its lock range across corners.

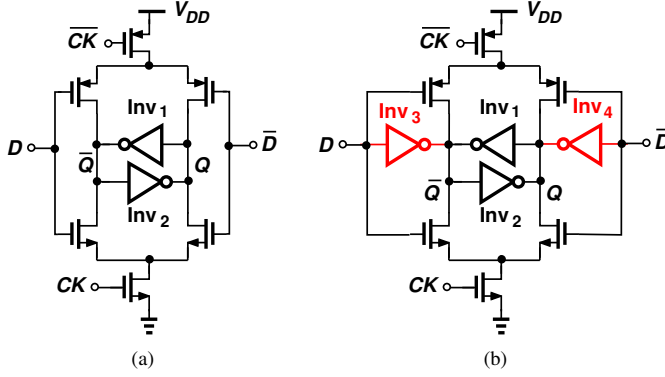
Feedforward extends the upper end of the lock range at the cost of the lower end because  $Inv_4$  begins to overwhelm  $Inv_1$  and  $S_2$  at low clock frequencies. We must therefore scale  $Inv_4$  properly with respect to the main path. As presented in Fig. 3(b), the worst case occurs in the slow-slow corner, providing a lock range from 37 GHz to 59 GHz. Without feedforward, the speed would be limited to 45 GHz in this corner.<sup>1</sup> The circuit dissipates 1.8 mW at 56 GHz. The next two stages in the prescaler are similar.

The Q-Gen circuit in Fig. 2 necessitates a  $\div 2$  topology that produces in-phase (I) and quadrature (Q) outputs, a property absent in the structure of Fig. 3(a). We still wish to avoid inductors in this circuit as well. We expect that two identical differential latches must form the divider. While current-mode logic (CML) readily yields such a configuration, buffering and distributing its moderate voltage swings prove problematic. In

<sup>1</sup>In a commercial product, the divider would need to satisfy other PVT corners as well, requiring some tunability or a more advanced process node.

other words, we prefer a realization with rail-to-rail inputs and outputs.

We begin with the differential clocked CMOS ( $C^2$ MOS) latch depicted in Fig. 4(a), where (weak) inverters  $Inv_1$  and  $Inv_2$  ensure that the overall divider loop does not find a “degenerate” state, i.e., it does not latch up. Nevertheless, a divider using this structure fails around 40 GHz.



(c)

Fig. 4. (a)  $C^2$ MOS latch, (b) addition of feedforward, and (c) divider lock range across corners.

We now introduce a feedforward path, as realized by inverters  $Inv_3$  and  $Inv_4$  in Fig. 4(b). As in the previous  $\div 2$  topology, this unclocked path carries  $D$  and  $\bar{D}$  to the output nodes of the latch and begins to write the state before the main branches are enabled, thus improving the maximum speed. The relative strength of  $Inv_3$  and  $Inv_4$  offers a trade-off between how much the upper end of the lock range is elevated and how much the lower end rises. Presented in Fig. 4(c), the simulation results indicate operation from 30 GHz to 58 GHz in the slow-slow corner. The divider consumes 4.7 mW at 56 GHz.

The distribution of the I and Q phases of the 28-GHz LO poses its own issues. With four beamforming elements on each side of the chip, these phases must travel about 300  $\mu\text{m}$  in the north and south directions. Thus, a total of 20 self-biased inverters act as repeaters in these paths. These inverters collectively consume 25 mW, a significant fraction of the overall power and a drawback of using a central synthesizer. The Q-Gen divider and the repeaters add 15 fs of rms jitter to the LO.

With a loop bandwidth of about 10 MHz, the synthesizer of Fig. 2 displays the simulated phase noise contributions plotted in Fig. 5. We observe that the VCO dominates.

### B. 28-GHz synthesizer with DLL

In the second generation of our 28-GHz RX development, we pursued two new concepts. First, we surmised that each

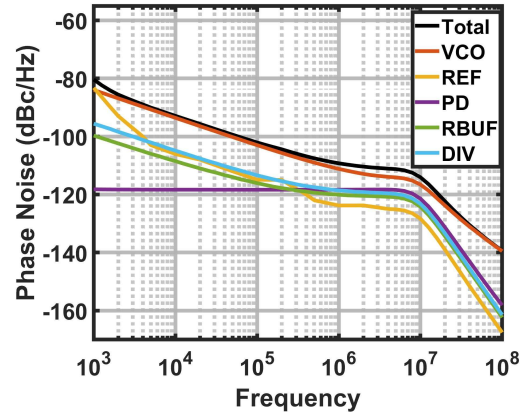


Fig. 5. Simulated phase noise components of the PLL.

beamforming element can employ a *dedicated* synthesizer, thereby obviating the need for LO distribution across the chip. Depicted in Fig. 6(a), such a system requires only  $f_{REF}$  ( $= 250$  MHz) to be distributed, greatly simplifying and modularizing the design. We predicted that this approach would still consume less power than the system studied in the previous section. Second, we explored the possibility of I/Q generation by means of a delay-locked loop (DLL) [3], thus allowing the synthesizer to operate at 28 GHz [Fig. 6(b)]. The motivation here is that the prescaler consumes less power and the DLL's power should also fall below that of the 56-GHz divider shown in Fig. 4(b).

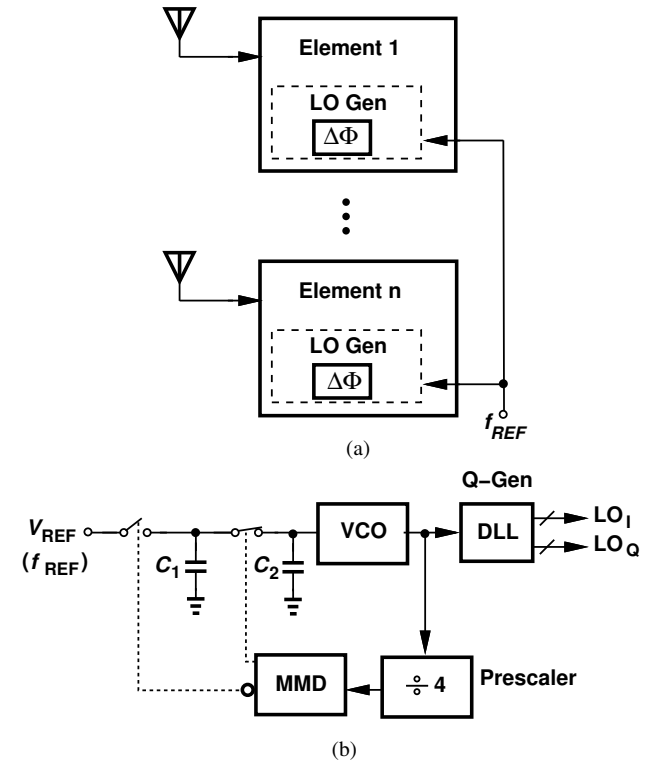


Fig. 6. (a) Beamforming RX with dedicated synthesizers, (b) 28-GHz PLL followed by a DLL.

To fulfill the first prediction, we introduce a current reuse

technique for the two most power-hungry blocks of each RX element, namely, the low-noise amplifier (LNA) and the VCO. Illustrated in Fig. 7(a), the idea is to stack the two structures while avoiding a cascode device in the former [3]. The circuit therefore consumes a headroom equal to two gate-source voltages—as in a CMOS inverter. Moreover, the common-mode level at  $X$  and  $Y$  is approximately equal to  $V_{DD}/2$ , maximizing the tuning range of the varactors. This stack draws 2.5 mW, and the remainder of the PLL in Fig. 6(b), 1.5 mW.

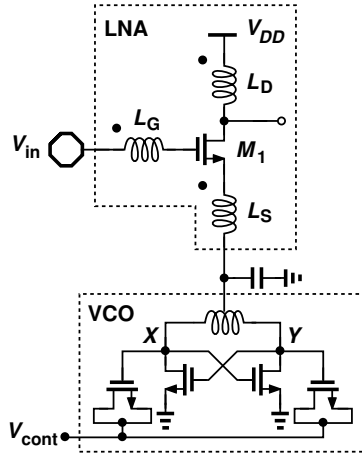


Fig. 7. Stacked LNA and VCO.

Shown in Fig. 8, the DLL incorporates two paths to generate  $LO_I$  and  $LO_Q$ . The phase difference between the two is detected by a symmetric mixer, and the result controls the lower path with a high loop gain. The DLL then settles such that the two mixer inputs bear a phase difference of approximately  $90^\circ$ . The circuit consumes 2.4 mW and contributes an rms jitter of 50 fs.

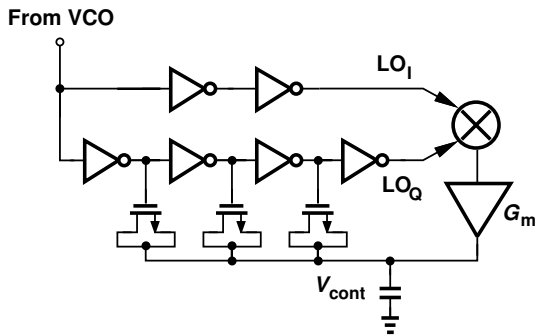


Fig. 8. DLL generating I and Q phases.

As reported in [3], this beamforming RX system achieves a per-element power consumption of 7.3 mW, a factor of 2.5 less than that of the array in the previous section.

The per-element synthesizer concept also offers new prospects for beamforming. Specifically, rather than insert a (lossy) phase-shift network in the 28-GHz LO path, we explore the possibility of varying the PLL output phase by adding a programmable dc voltage to the VCO control. As conceptually illustrated in Fig. 9(a), we add  $V_{DAC}$  and note

that  $V_{PD} \neq V_{cont}$  if  $V_{DAC} \neq 0$ . Since, for a given LO frequency,  $V_{cont}$  is fixed, varying  $V_{DAC}$  causes  $V_{PD}$  to change, thus adjusting the phase difference between  $V_F$  and  $V_{REF}$ . By exploiting this property of type-I PLLs, we can create a wide range of phase shift at the VCO output with a high resolution, the latter limited by only that of the DAC. For example, if  $V_{REF}$  has rise and fall times equal to 40 ps, the PD characteristic [Fig. 9(b)], remains linear for roughly  $T_1 = 40$  ps. That is, the phase difference,  $\Delta T$ , can vary by this amount, which translates to  $(40 \text{ ps} \times 28 \text{ GHz}) \times 360^\circ \approx 400^\circ$ .

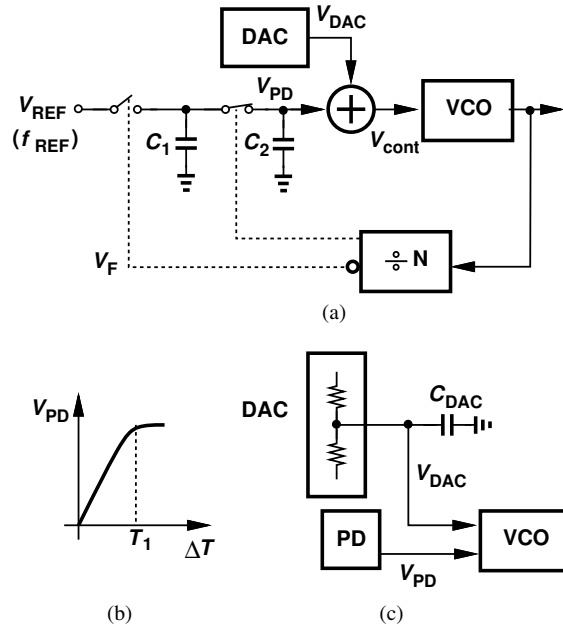


Fig. 9. (a) PLL using voltage addition to create output phase shift, and (b) PD characteristic, and (c) actual implementation.

In our work, the DAC is realized by a resistor ladder, providing a range of  $400^\circ$  with a resolution of  $10^\circ$  and negligible power consumption.

We should make two remarks about the topology of Fig. 9(a). First, the summation of  $V_{DAC}$  and  $V_{PD}$  is, in fact, implemented by two separate VCO controls [Fig. 9(c)], with the gain in the DAC path set to about 50% of that in the main path. This is accomplished by decomposing the varactors in Fig. 7 into two sets and using one for  $V_{PD}$  and the other for  $V_{DAC}$ . Second, capacitor  $C_{DAC}$  bypasses the resistor ladder's thermal and supply noise, ensuring that beamforming is obtained at nearly no cost.

## V. LO GENERATION FOR 140-GHz RADIOS

### A. Direct Conversion Issues

A direct-conversion RX operating in the 140-GHz band would face several serious issues. First, it would require a QVCO or passive polyphase filters for I/Q generation, both power-hungry solutions. Second, such a PLL would still rely on a 140-GHz  $\div 2$  circuit in its feedback path, a difficult block to design even if it need not provide quadrature outputs. Third, a 1-ps mismatch between the interconnects carrying 140-GHz I and Q phases would translate to  $50^\circ$  of phase mismatch. For these reasons, we prefer I/Q separation at lower frequencies and hence a heterodyne architecture.

## B. RX Architecture

Shown in Fig. 10 in simplified form, the heterodyne RX mixes the RF input with a 94-GHz first LO, and applies the intermediate-frequency (IF) signal to quadrature mixers driven by a 47-GHz second LO [9]. As with the system depicted in Fig. 6(a), this work adopts a per-element LO synthesis approach to avoid distribution of high frequencies to multiple elements.

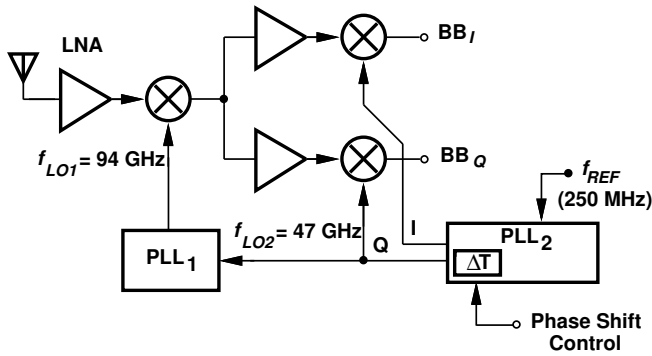


Fig. 10. 140-GHz RX architecture.

The LO network in Fig. 10 merits several remarks. First, unlike typical sliding-IF receivers, this architecture doubles the second LO frequency by means of a subsampling PLL (PLL<sub>1</sub>) rather than divide the first one by 2. This method avoids dividers operating at 94 GHz. Second, the phase-shift network necessary for beamforming is realized within PLL<sub>2</sub>, drawing less than 0.5 mW. Third, the PLLs and mixers are codesigned and so positioned in the floor plan as to avoid any (inductively-peaked) buffers. As shown in Fig. 11, the outputs of PLL<sub>1</sub>'s VCO travel directly to the RF mixer. The interconnects lower the quality factor by about 10% but the wide loop bandwidth still suppresses the phase noise. This

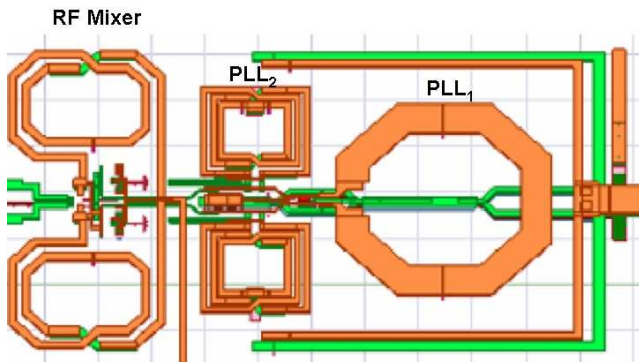


Fig. 11. 140-GHz RX floor plan showing the connection of PLL<sub>1</sub> to the RF mixer.

leads to both power savings and a compact design with short interconnects.

## C. 47-GHz PLL

PLL<sub>2</sub> in Fig. 10 is similar to those depicted in Figs. 2 and 6(b). As shown in Fig. 12(a), the loop incorporates a programmable phase shifter,  $\Delta T$ , in its feedback path at 250 MHz. If  $\Delta T$  varies by about 12 ps, then the phase of LO<sub>2</sub> ranges by 180°. (Another 180° can be obtained by swapping the differential baseband signals.) Illustrated in Fig. 12(b), the  $\Delta T$  network simply consists of inverters with switched capacitors, achieving a resolution of 7° and contributing an rms jitter of 15 fs. PLL<sub>2</sub> consumes 11 mW.

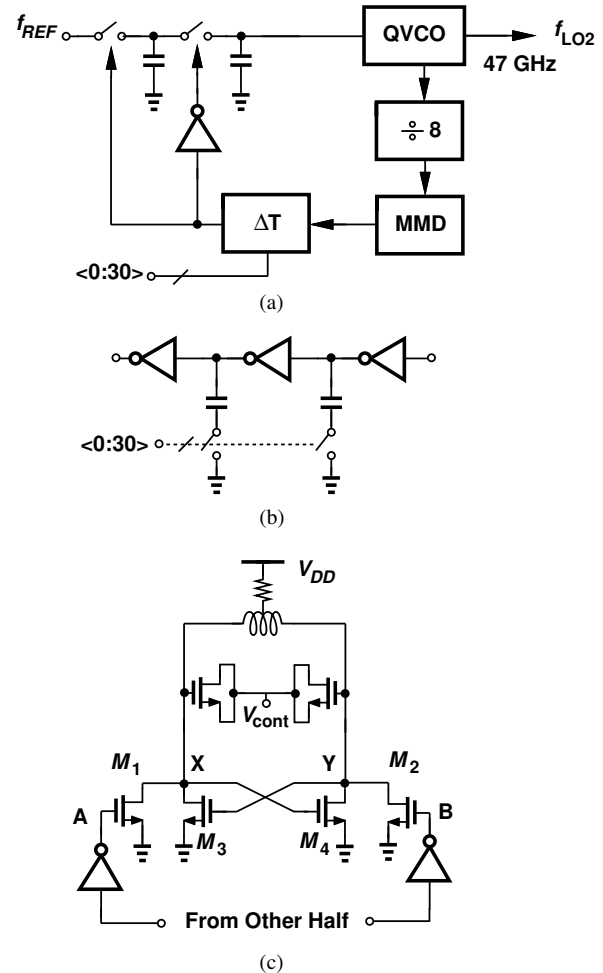


Fig. 12. (a) 47-GHz PLL with I/Q generation and phase shifter, (b) phase shifter realization, and (c) QVCO topology.

The 47-GHz PLL directly delivers quadrature LO phases to the IF mixers. This is accomplished by a new QVCO topology, shown in Fig. 12(c) [9]. The inverters inserted in the coupling path between the two cores introduce additional phase shift, thus forcing the oscillation frequency closer to the tanks' resonance frequency. As a result, the phase noise falls by 6 dB while the mode ambiguity observed in the conventional QVCO [24] is eliminated.

## D. 94-GHz PLL

PLL<sub>1</sub> in Fig. 10 simply serves as a frequency doubler. Its principal advantage over other doublers is the ability to provide large, differential voltages to the RF mixer with no

intervening buffers. To avoid a 94-GHz  $\div 2$  circuit, the loop employs subsampling (Fig. 13). The PD senses the differential outputs of the VCO for symmetric loading and a higher gain, and amplifier  $A_1$  converts the result to a single-ended control.

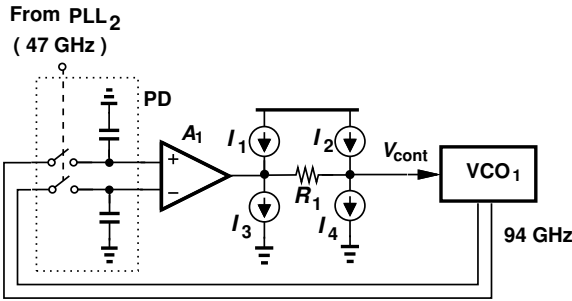


Fig. 13. 94-GHz PLL.

The capture range of PLL<sub>2</sub> is limited by the output voltage range of  $A_1$ , which in turn constrains the tuning range of the VCO. For this reason, we interpose a voltage level shifter between  $A_1$  and VCO<sub>1</sub>, as realized by equal current sources,  $I_1, \dots, I_4$ , and  $R_1$ . That is, if the loop aims for a high  $V_{cont}$ , we enable  $I_2$  and  $I_3$ , thereby creating an upward shift equal to  $I_2 R_1$ . Conversely, if a low  $V_{cont}$  is necessary,  $I_1$  and  $I_4$  are activated. In this prototype, these current sources are controlled through a serial bus.

With varactor and discrete tuning, the  $Q$  of VCO<sub>1</sub> falls to 15, yielding a free-running phase noise of  $-108$  dBc/Hz. Fortunately, however, a reference frequency of 47 GHz accommodates a loop bandwidth of 700 MHz, making this PLL's jitter contribution negligible. This PLL draws 6 mW.

## VI. LO GENERATION FOR 300-GHZ RADIOS

The issues outlined in the previous section for 140-GHz systems become more severe in 300-GHz radios. Direct conversion proves even less feasible, and the use of frequency multipliers demands greater power consumption.

Direct LO generation for a frequency of 300 GHz (for direct conversion) or slightly lower (for heterodyning) faces three formidable challenges. First, the low  $Q$  of MOS varactors prohibits their use here. According to [20], the  $Q$  falls to single digits at these frequencies. Consequently, a VCO using such varactors may simply fail to oscillate. Second, even our proposed VCO topology (Section VI.C) exhibits a high phase noise. Third, the reference phase noise contributes significant jitter, making it difficult to optimize a single PLL's bandwidth for suppressing the VCO PN. For example, a 450-MHz crystal oscillator (Crystek CRBSVS-01-450) with a phase noise of  $-168$  dBc/Hz at offset frequencies above 200 kHz produces a high jitter at 300 GHz. These issues are greatly alleviated through the use of cascaded PLLs in this work.<sup>2</sup>

<sup>2</sup>A crystal frequency of 450 MHz may appear arbitrary. However, most mm-wave LO generators published to date assume external references that are convenient to their designs, e.g., 2.82 GHz in [7], 44 GHz in [13], 5.8 GHz in [14].

### A. RX Architecture

Shown in Fig. 14 is the heterodyne RX architecture, illustrating the roles of three cascaded PLLs for LO generation [11]. The RF input signal is mixed with a 270-GHz LO, yielding an IF component at approximately 27 GHz. Two quadrature mixers,  $MX_I$  and  $MX_Q$ , then downconvert the signal to baseband.

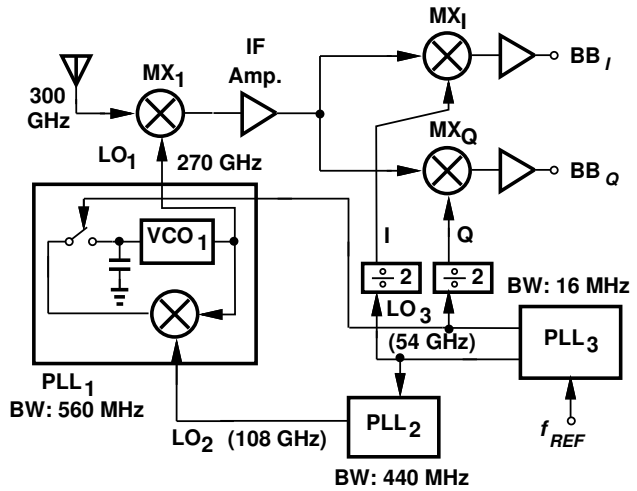


Fig. 14. 300-GHz RX architecture.

Governed by the issues described above and the speed limitations of 28-nm technology, the LO generation network is implemented by three PLLs. PLL<sub>3</sub> multiplies  $f_{REF} = 450$  MHz to 54 GHz. To produce 27 GHz, we use the  $\div 2$  stage proposed in Fig. 3(a). Since this structure does not offer quadrature outputs, we incorporate two copies, with their  $CK$  and  $\overline{CK}$  swapped.

The 54-GHz output of PLL<sub>3</sub> must be multiplied up to 270 GHz for LO<sub>1</sub>, a noninteger ratio. We first double  $f_{LO3}$  by means of PLL<sub>2</sub> and then employ offset-mixing and sub-sampling in PLL<sub>1</sub> to realize a 270-GHz output. The reason for selecting three PLLs and their frequencies becomes clear below.

We should make two remarks. First, the PLL bandwidths shown in Fig. 14 reveal one advantage of cascading. PLL<sub>3</sub> benefits only moderately from  $BW_3 = 16$  MHz, as dictated by its reference and VCO PN, and, therefore, burns 12 mW in its VCO. PLL<sub>2</sub> and PLL<sub>3</sub>, on the other hand, operate with 440-MHz and 560-MHz bandwidths, respectively, thus suppressing the PN of their VCOs considerably. We elaborate on these concepts in the next section.

Second, while this work does not offer a provision for beamforming, it can incorporate any of the phase shift techniques in the previous sections in a per-element LO synthesis architecture.

### B. Benefits of Cascaded PLLs

The frequency plan of Fig. 14 avoids terahertz frequency dividers, lossy doublers, and passive I/Q separation. We surmise that the three PLLs still consume less power than the prior art's LO generation networks. We quantify some of the advantages of cascading here.



As explained in [21], cascaded PLLs can outperform a single loop under certain conditions. Consider the synthesis of a given frequency,  $Mf_{REF}$ , from a crystal oscillator operating at  $f_{REF}$  with a fairly flat PN of  $S_{REF}$ . Displayed in Fig. 15(a), a single loop containing  $VCO_a$  is optimized by first equating the VCO PN,  $S_{\phi na}(f)$ , to the “amplified” reference PN,  $M^2S_{REF}$  and finding the intersection frequency,  $f_1$  [Fig. 15(b)]. The loop BW is then chosen approximately equal to  $f_1$ .

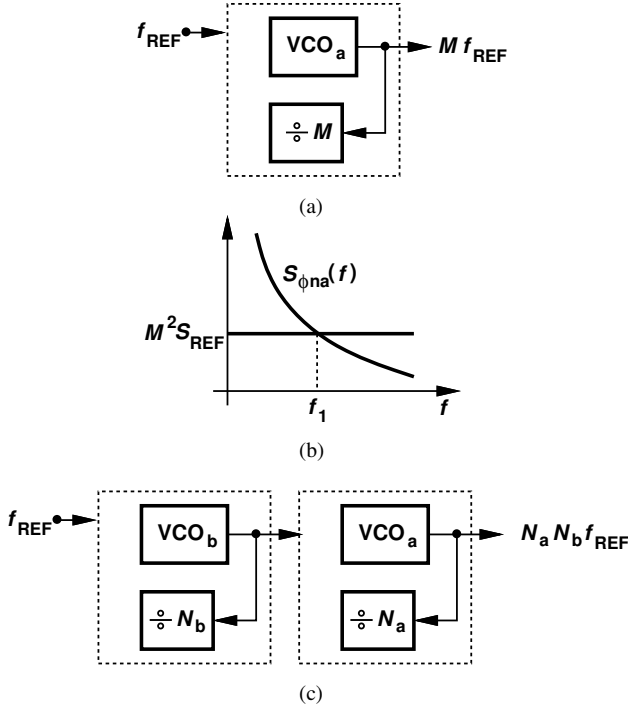


Fig. 15. (a) Single loop generating  $Mf_{REF}$ , (b) optimum loop bandwidth calculation, and (c) cascaded PLLs generating  $Mf_{REF}$ .

Alternatively, we can write  $M = N_a N_b$  and cascade two loops with divide ratios of  $N_a$  and  $N_b$  [Fig. 15(c)]. For cascading to be advantageous, the PN of  $VCO_b$  must satisfy this relation [21]:

$$N_b^2 S_{\phi nb}(f) < S_{\phi na}(f). \quad (1)$$

As discussed below, a 270-GHz 2.5-mW VCO exhibits  $S_{\phi na}(f = 40 \text{ MHz}) = -107 \text{ dBc/Hz}$ , whereas a 54-GHz 11.8-mW VCO displays  $S_{\phi nb}(f = 40 \text{ MHz}) = -138 \text{ dBc/Hz}$ . If the latter is raised by  $10 \log(270/54)^2 = 14 \text{ dB}$ , it is still 17 dB lower than the former, suggesting that cascading proves beneficial here.

The designs of PLL<sub>2</sub> and PLL<sub>3</sub> are similar to those in Figs. 13 and 6(b), respectively. We therefore focus on PLL<sub>1</sub> here.

### C. 270-GHz PLL

With an  $f_{max}$  of about 450 GHz, 28-nm technology poses severe challenges to phase-locking at 270 GHz. For example, consider a simple subsampling PLL for multiplying up a frequency to 270 GHz [Fig. 16(a)]. The difficulty here is that the on-resistance of  $S_1$  climbs as  $V_{REF}$  falls [Fig. 16(b)] and as  $V_{VCO}$  makes several cycles. Consequently, the last

cycle reaching  $C_1$  is heavily attenuated, providing little phase information. This effect leads to a low PD gain. The simulation results in Fig. 16(c) reveal that the gain drops by about one order of magnitude as the fall time of the LO driving  $S_1$  increases from zero to 4 ps. The subsampling PLL thus fails to lock.

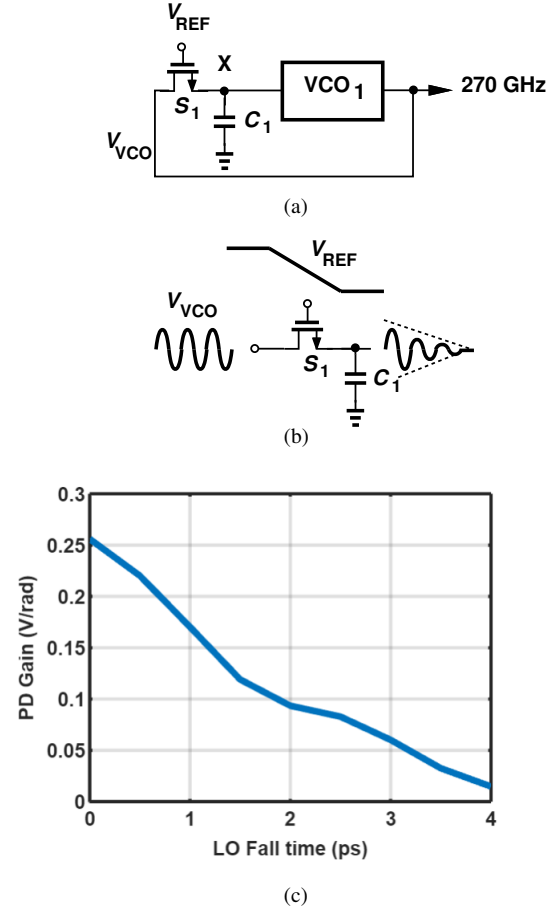


Fig. 16. (a) Simple subsampling PLL, (b) effect of switch resistance on sampled signal, and (c) resulting PD characteristic.

The above effect can be alleviated if the feedback frequency sensed by the PD is reduced, a task accomplished by heterodyning (offset-mixing) so as to avoid frequency dividers. Illustrated in Fig. 17 [11], the idea is to downconvert  $f_{VCO}$ , by means of mixing it with  $f_{LO2} = 108 \text{ GHz}$ . The result is then sampled by  $S_1$  at a rate of 54 GHz. According to simulations, the 65% reduction in the frequency sensed by the PD raises the gain by about one order of magnitude. Noting that the conversion gain of mixer  $MX_0$  affects the loop gain, we realize this circuit as an active double-balanced topology to obtain a single-ended output swing of 420 mV [11]. The input capacitance of  $MX_0$  loads the VCO and is minimized by choosing small transistors ( $W = 1.2 \mu\text{m}$ ) for this port.

We now appreciate the choice of the PLL frequencies in Fig. 14. PLL<sub>3</sub> yields both 27 GHz for the IF mixers and 54 GHz for the frequency-doubling PLL<sub>2</sub>. The resulting 108-GHz output drives the offset mixer in PLL<sub>1</sub> while the 54-GHz waveform serves as its reference.

Figure 18 plots the simulated responses of PLL<sub>1</sub> from the input phase and from the VCO phase to the output, revealing

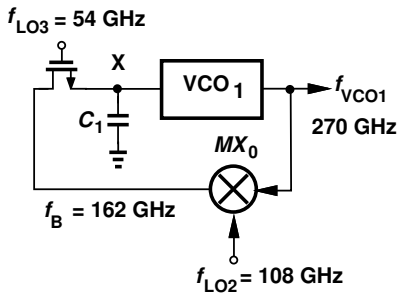


Fig. 17. Subsampling PLL with offset-mixing.

a bandwidth of about 560 MHz. The loop suppresses the VCO PN by more than 30 dB up to 10-MHz offset.

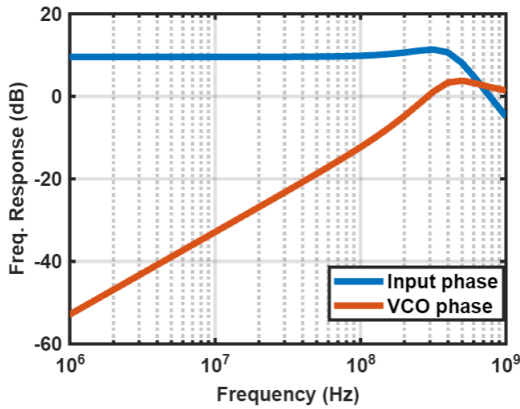


Fig. 18. Simulated responses of 270-GHz PLL.

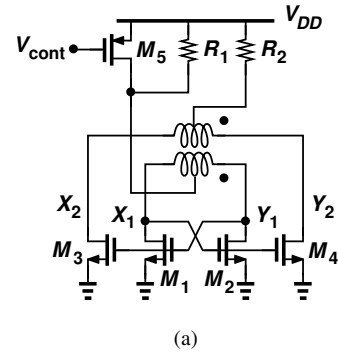
The 270-GHz VCO in PLL<sub>1</sub> still proves challenging. As mentioned previously, the low  $Q$  of MOS varactors at these frequencies encourages us to seek other methods of tuning. Shown in Fig. 19(a), the proposed VCO is based on the topology reported in [22] but with  $M_5$  added [11]. Frequency tuning is achieved by recognizing that the gate-source capacitance of  $M_1$ – $M_4$  rises as the CM level at  $X_1$ ,  $Y_1$ ,  $X_2$ , and  $Y_2$  climbs. Transistor  $M_5$  adjusts this level between 0.5 V and 0.9 V. The output voltage swing decreases at lower CM levels, but we design the circuit for an acceptable swing in the worst case.

Figure 19(b) depicts the simulated oscillation frequency and single-ended output swing at  $X_2$  and  $Y_2$  as a function of  $V_{cont}$ , indicating a tuning range of about 12 GHz and a worst-case swing of 0.72 V.

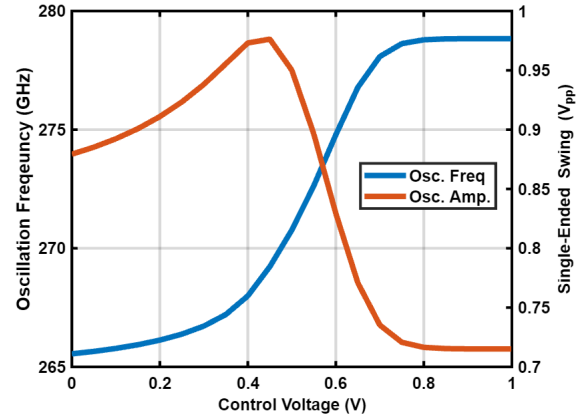
The VCO's coupled inductors are implemented as shown in Fig. 19(c), each having a linewidth of 3.3  $\mu\text{m}$  and with diameters equal to 26.7  $\mu\text{m}$  and 33  $\mu\text{m}$ . According to HFSS simulations, the  $Q$  is about 16.

The flicker noise of  $M_5$  in Fig. 19(a) directly modulates the oscillation frequency, potentially producing substantial phase noise. Large dimensions are chosen for this device to ensure less than 1% contribution.

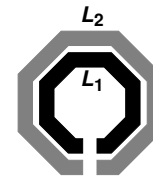
Drawing a total bias current of 2.5 mA, the VCO exhibits the phase noise plotted in Fig. 20, revealing flicker noise upconversion from  $M_1$ – $M_4$  up to about 10-MHz offset. At this offset,  $\text{PN} = -94 \text{ dBc/Hz}$ . Nonetheless, the wide loop bandwidth makes this contribution negligible even in a type-I PLL.



(a)



(b)



(c)

Fig. 19. (a) 270-GHz VCO topology, (b) its simulated characteristics, and (c) implementation of coupled inductors.

## VII. EXPERIMENTAL RESULTS

In this section, we report the LO-related experimental results for the two 28-GHz receivers and the 140-GHz and 300-GHz receivers. The prototypes have been fabricated in TSCM's 28-nm technology.

### A. LO Generation for 28-GHz Receivers

Figure 21 shows the die photograph of the RX described in Section IV.A. The PLL output spectrum is measured at the output of the  $\div 8$  stage and is plotted in Fig. 22(a). The reference spur level at 250-MHz offset is at  $-58 \text{ dBc}$ , translating to  $-40 \text{ dBc}$  at the VCO output. Presented in Fig. 22(b), the phase noise profile yields an integrated rms jitter of 155 fs from 1 kHz to 40 MHz.

Figure 23 depicts the die photograph of the RX studied in Section IV.B. The LO performance is evaluated by applying a 28-GHz input to the receiver and observing the baseband output. Plotted in Figs. 24(a) and (b) are the resulting spectrum and PN profiles, respectively. Aliased from negative frequencies, the reference spur resides at 130 MHz and has a level of



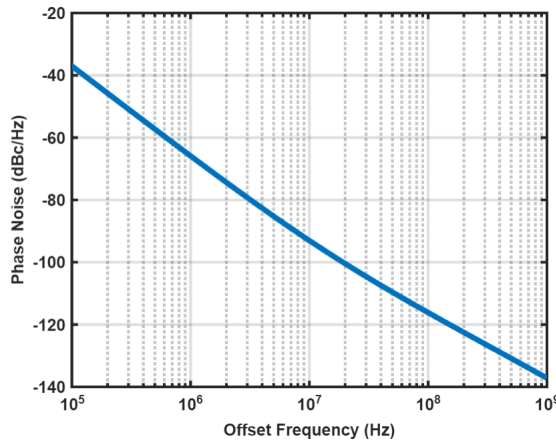


Fig. 20. Simulated phase noise of 270-GHz VCO.

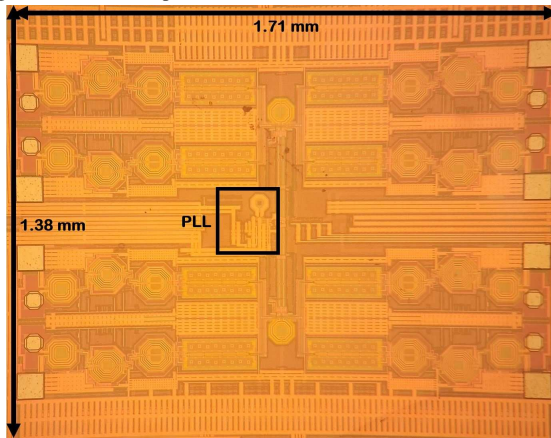


Fig. 21. Die photograph of the first 28-GHz RX.

−41 dBc. The rms jitter integrated from 10 kHz to 100 MHz amounts to 640 fs.

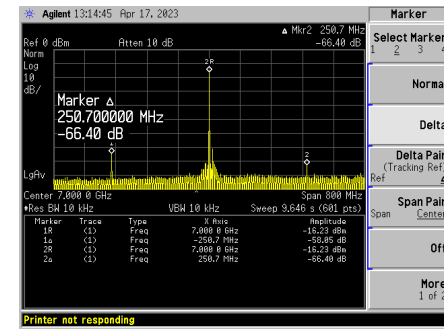
The beamforming phase shift method proposed for this RX in Section IV.B is characterized by stepping the DAC input in Fig. 9(c) from 00...0 to 11...1 and measuring the phase shift in the baseband output. Figure 25 plots this result, indicating a range of 400°.

This 8-element beamforming system employs as many PLLs, raising concern about injection-pulling between them. However, since all of the loops operate at the same output frequency, no corruption occurs. We merely expect a change in the output *phase* of one PLL when an adjacent one is activated. This effect proves negligible, as demonstrated by the two plots in Fig. 25, where an adjacent element and its PLL are turned on and off.

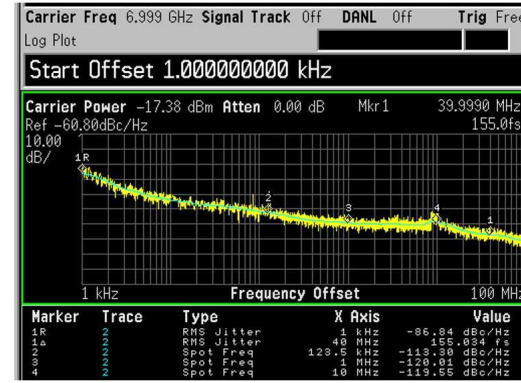
### B. LO Generation for 140-GHz Receiver

The die photograph of this RX is shown in Fig. 26. The baseband output spectrum in Fig. 10 is plotted in Fig. 27(a). The reference spur is at −42 dBc. Figure 27(b) displays the PN at the output of the ÷8 stage in Fig. 12(a). The integrated jitter from 10 kHz to 100 MHz is equal to 126 fs<sub>rms</sub>.

The PN of PLL<sub>1</sub> in Fig. 10 cannot be measured directly, but, by applying a 140-GHz input to the RX and examining the



(a)



(b)

Fig. 22. (a) Spectrum, and (b) phase noise measured at the ÷8 stage output.

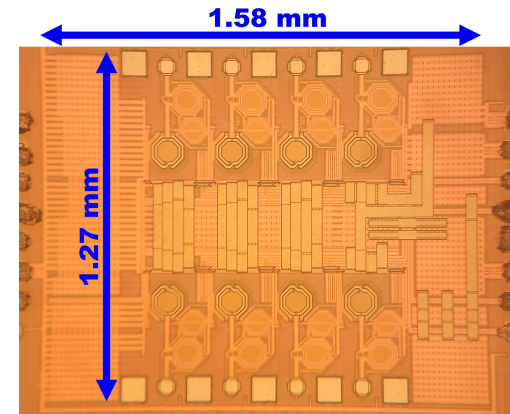


Fig. 23. Die photograph of the second 28-GHz RX.

baseband output, we can assess the combined contributions of PLL<sub>1</sub> and PLL<sub>2</sub>. Plotted in Fig. 28, the result reveals a jitter of 9.14 ps for the downconverted 2.052-GHz baseband frequency and hence 134 fs<sub>rms</sub> at 140 GHz. We then estimate a jitter of  $\sqrt{134^2 - 126^2} \approx 60$  fs for PLL<sub>1</sub>. This estimate incurs some error because the PN of PLL<sub>1</sub> is correlated with that of PLL<sub>2</sub>.

### C. LO Generation for 300-GHz Receiver

Shown in Fig. 29 is the die photograph of this RX. The performance of the LO generation network in Fig. 14 is measured on a separate chip that excludes this RX path. An on-chip mixer driven by an external LO at  $f_{ext} \approx 89.579$  GHz

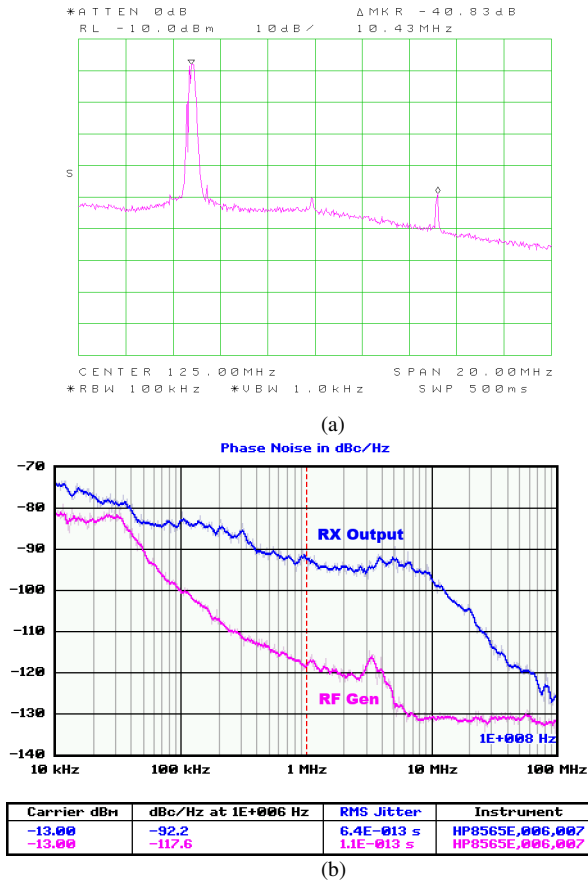


Fig. 24. (a) Spectrum, and (b) phase noise measured at the  $\div 8$  stage output.

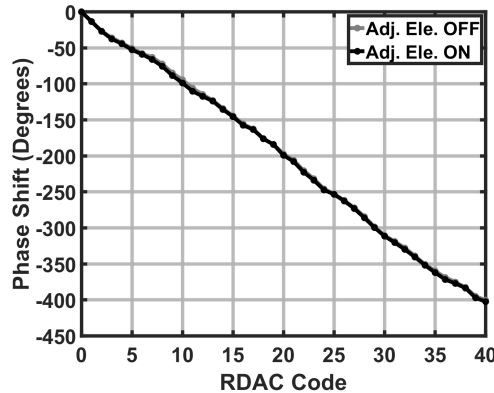


Fig. 25. Phase shift characteristics of 28-GHz system.

senses the 270-GHz PLL output. Upon mixing with  $3f_{ext}$ , we obtain the downconverted output spectrum shown in Fig. 30(a) and the PN profile plotted in Fig. 30(b). Integrated from 10 kHz to 10 MHz, the rms jitter amounts to 106 fs. This value arises from all three PLLs in Fig. 14.

The PN of PLL<sub>3</sub> in Fig. 14 is monitored at the output of its feedback divider, i.e., after division by 120. Displayed in Fig. 30(c), the result implies an integrated jitter of 34 fs<sub>rms</sub> from 10 kHz to 10 MHz.

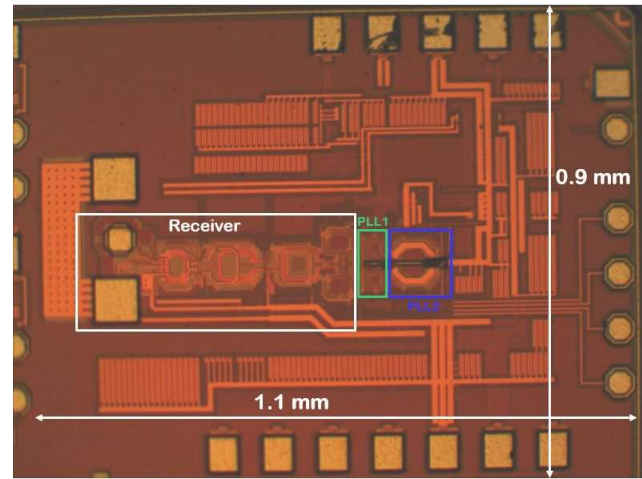


Fig. 26. Die photograph of 140-GHz RX.

## VIII. CONCLUSION

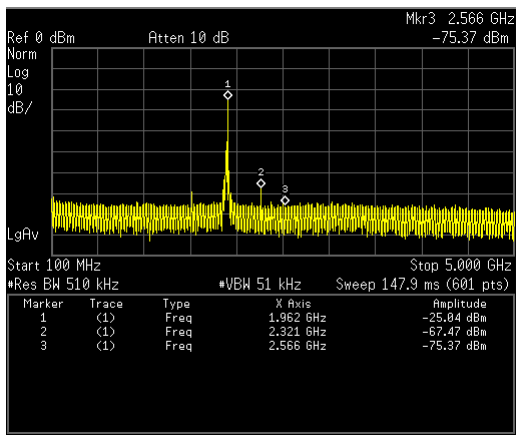
This paper addresses the challenges facing LO generation for mm-wave radios. A number of techniques are proposed and demonstrated in the context of receivers operating at 28 GHz, 140 GHz, and 300 GHz. The prototypes have been fabricated in 28-nm CMOS technology.

## IX. ACKNOWLEDGMENT

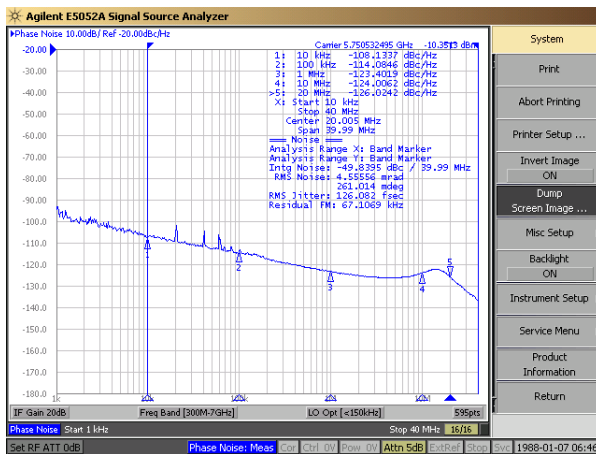
This research was supported by Realtek Semiconductor. The author gratefully acknowledges the TSMC University Shuttle Program for chip fabrication.

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(a)



(b)

Fig. 27. (a) Spectrum, and (b) phase noise measured at the  $\div 8$  stage output.

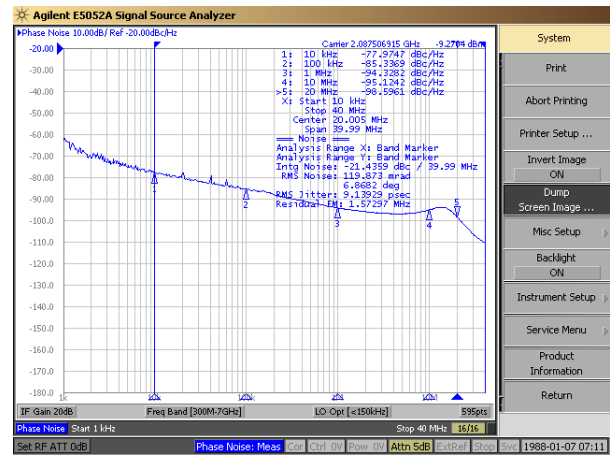


Fig. 28. Downconverted signal phase noise.

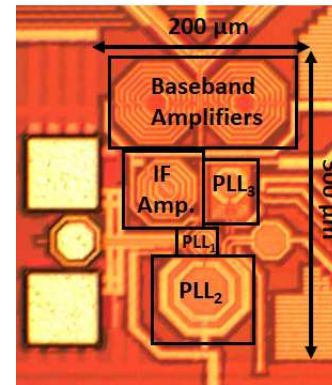
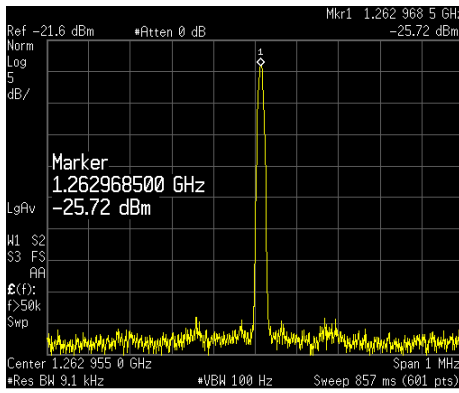
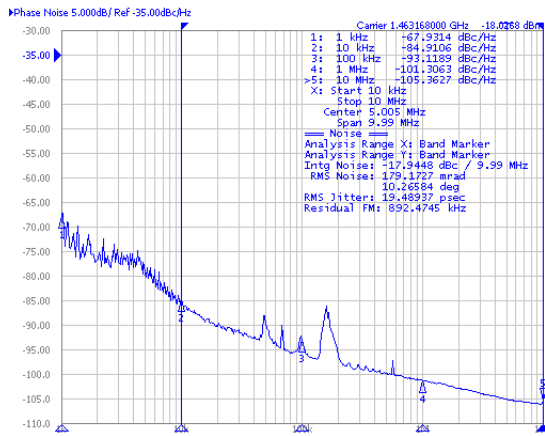


Fig. 29. Die photograph of 300-GHz RX.

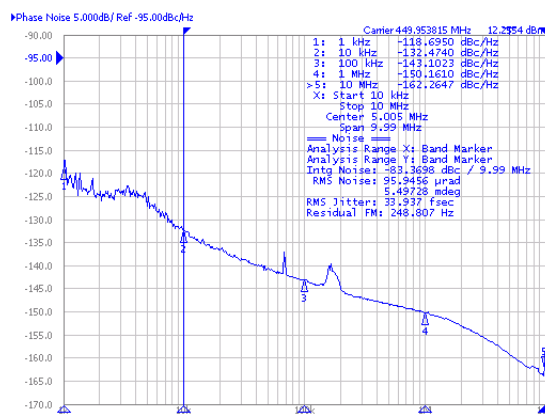
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(a)



(b)



(c)

Fig. 30. (a) Downconverted signal spectrum, (b) its phase noise, and (c) phase noise at the output of  $\div 8$  stage in 54-GHz PLL.