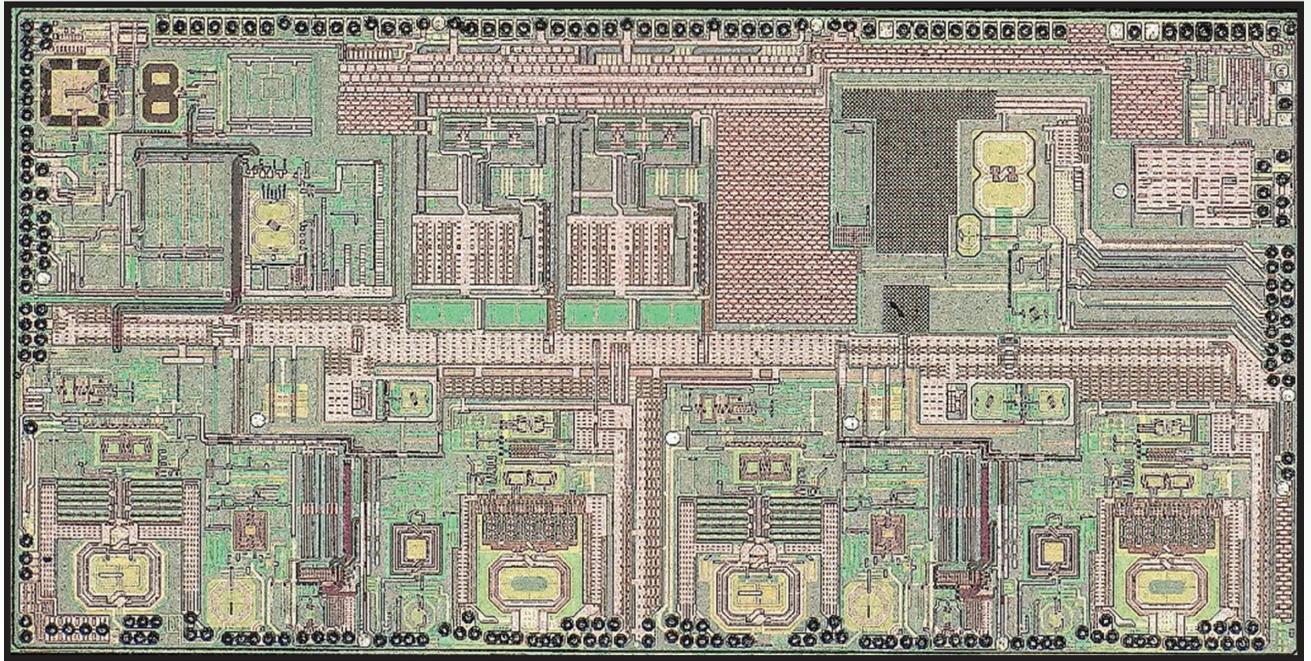


75 Years of RF Design



Highlights and Paradigm Shifts

Radio-frequency (RF) circuits came into existence decades before the invention of the transistor. The First World War motivated great advances in wireless communications and radar design—all based on vacuum tubes. Then came the notion of public radio and television, driving RF circuits into the consumer market. By the mid-1940s, when the bipolar transistor was conceived at Bell Laboratories, vacuum-tube RF design had become fairly mature [1]. Of course, the products drew high power and failed frequently. Based

on electron transport in a vacuum, these components could operate as only “n-type” devices, a stark contrast to what bipolar and MOS technologies would offer decades later.

The migration from tubes to transistors took some years but subsequently accelerated due to three advantages of the latter: product lifetime, power consumption, and cost. The much smaller form factor was an additional bonus. In this article, we briefly review advances in RF circuits since then. The article does not intend to offer a linear or comprehensive history. Rather, our ambition is to 1) understand how RF designers’ mentality has evolved and 2) identify some of the concepts that have stood the test of time and still play a key role in modern radios.

Vacuum Tubes Versus Transistors

While they had been under development for decades, vacuum tubes faced some fundamental drawbacks.

- 1) They required supply voltages of 100–400 V.
- 2) They consumed high power and produced a great deal of heat.
- 3) They had a short lifetime.
- 4) They occupied a large volume (about several cubic centimeters).
- 5) They were expensive to manufacture.

The transistor by far outperformed (or was projected to outperform) the tube in all these respects.

Another advantage of bipolar technology that would eventually materialize was the ability to provide both

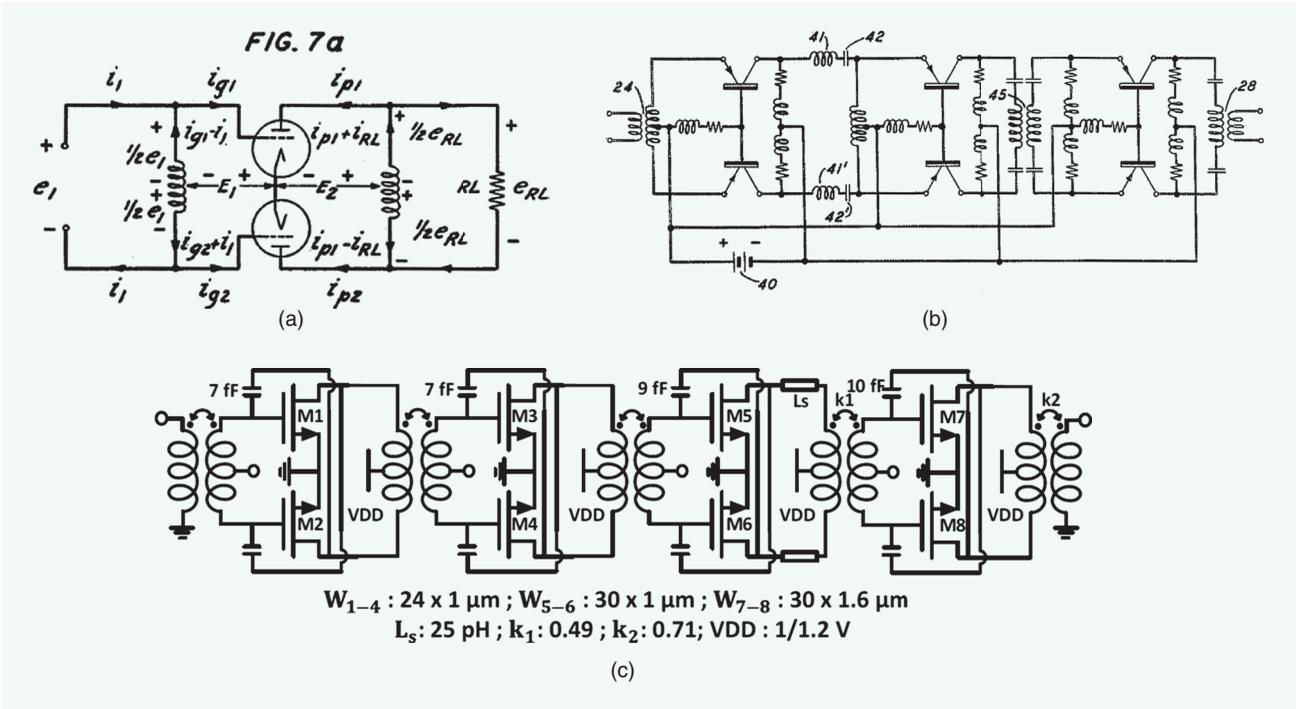


FIGURE 1: (a) A vacuum-tube amplifier [3], (b) its multistage transistor counterpart [3], and (c) a modern example [4].

n-type and p-type devices. Also interesting is that the early generations included only *pnp* germanium transistors, and it was in the 1960s that *npn* silicon components became practical. The use of complementary devices in RF circuits would nevertheless have to wait until CMOS took over.

One drawback of the bipolar transistor was its low input impedance as compared to its megaohm tube counterpart. While affecting bias network design, this issue did not prove serious in RF circuits.

Transistorization

Having recognized the enormous potential of the bipolar transistor, companies such as Bell Laboratories and Radio Corporation of America (RCA) swiftly embarked upon “transistorization” [2]. The small form factor pointed to portable applications such as AM/FM radios, and the low cost motivated usage in television electronics.

As we examine the work reported in the 1950s, we observe that most of the early transistorization efforts simply replaced vacuum tubes with bipolar devices. Indeed, the vast knowledge of electronic design developed in

previous decades was almost directly applicable to transistor circuits. Basic amplifier stages, for example, could follow a simple mapping from tubes to transistors (but with different biasing schemes), and functions such as mixing and oscillation were based on the older topologies as well.

Tube-transistor mapping is evident in the push-pull class-B amplifier disclosed in a patent filed in 1950 by Bell Telephone Laboratories [3]. Shown in Figure 1(a) and (b) are the two implementations, both remarkably similar to today’s structures in Figure 1(c) [4].

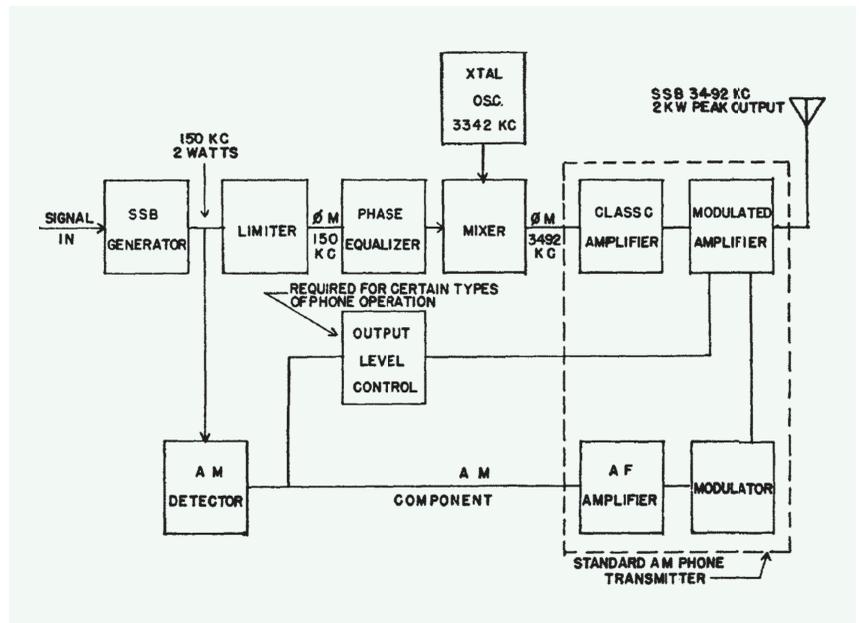


FIGURE 2: Kahn’s polar modulation system [5]. AF: audio frequency; KC: kilocycles per second (kHz); Osc.: oscillator; XTAL: crystal.

1952: Polar Modulation Is Born

As the oldest modulation scheme, AM had naturally created a demand for linear transmitters (TXs) and power amplifiers (PAs), leading to numerous linearization techniques. The principal difficulty with most of these methods was that they required some PA linearity even before correction was applied. In 1952, Kahn introduced "envelope elimination and restoration," later called *polar modulation* [5]. As depicted in Figure 2, the idea is to separate the envelope and phase components, amplify them independently, and "combine" them in the last stage. The high-power output stage,

in principle, requires no linearity, thus achieving great efficiency.

The complexity of polar modulation did not allow its widespread use at the time, especially in (cost-sensitive) consumer products. But the idea reemerged four decades later and found its way into mobile devices [26], [27].

1954: Mixer-First Receivers Are Introduced

Frequency limitations of early transistors prohibited gain at RF, dictating that the received signal be immediately downconverted. This was accomplished by either 1) an oscillator into which the RF input was

injected or 2) a mixer transistor that received both the input and the local oscillator (LO) waveforms. Figure 3 shows an example of the latter for "pocket" AM radios [6]. Here, the top left transistor senses the antenna signal at its base and the LO at its emitter, thus operating as a mixer. The transistor on the bottom left employs transformer feedback to serve as the LO. The intermediate-frequency (IF) output is then applied to a number of gain stages before it is detected. Another example was reported by [2].

An interesting issue recognized by [6] was that the emitter path of the mixer transistor in Figure 3 presented

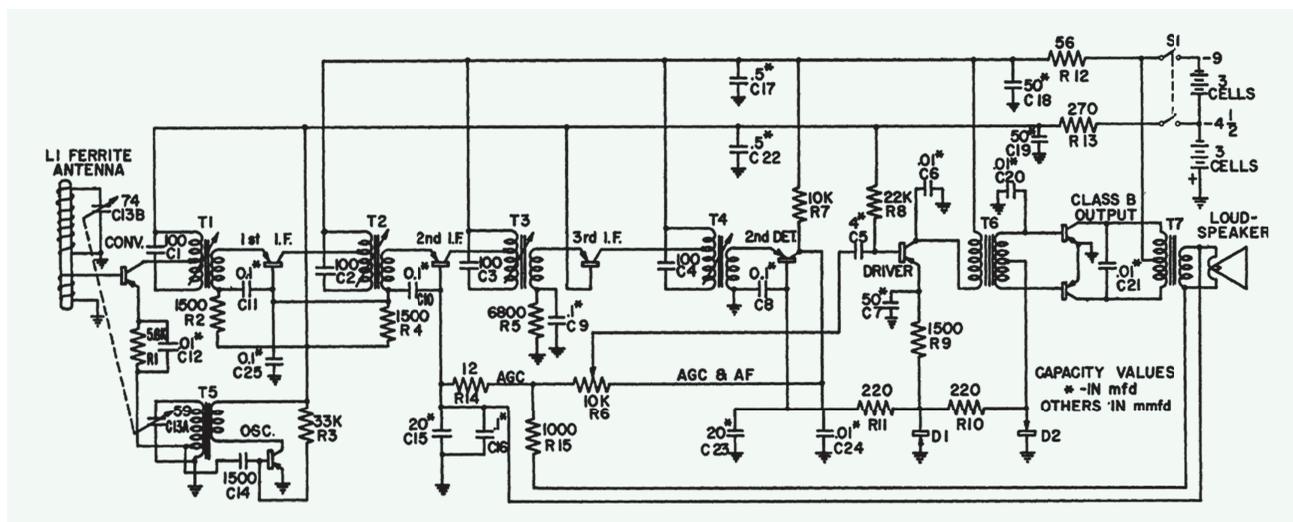


FIGURE 3: A mixer-first RX from 1954 [6].

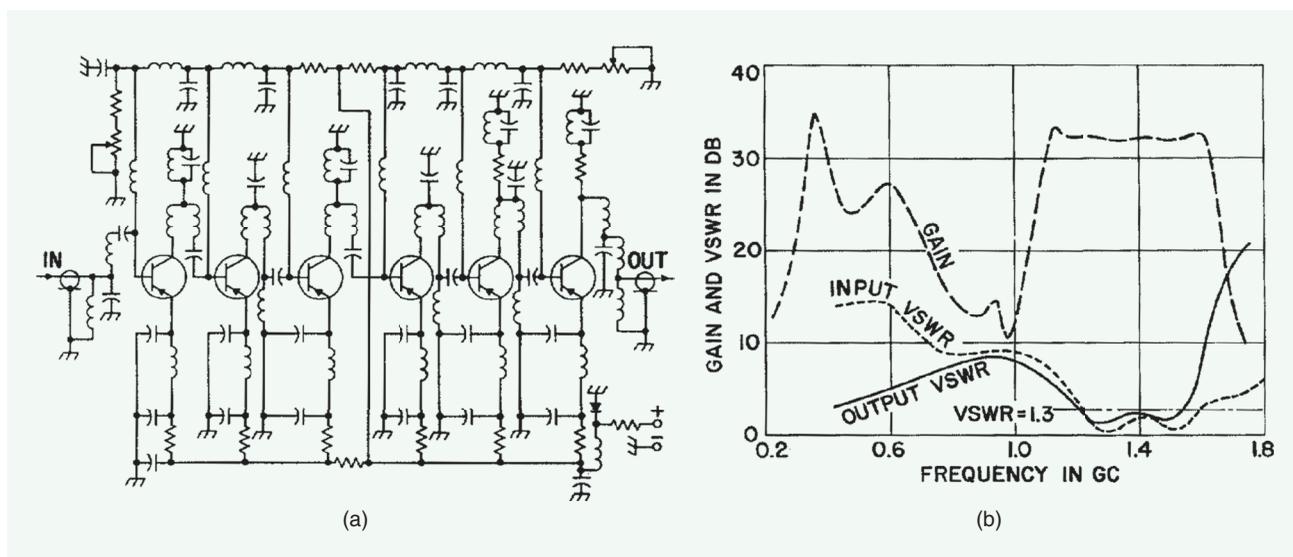


FIGURE 4: (a) A gigahertz amplifier from 1963 [7] and (b) its frequency response. GC: gigacycles per second (GHz).

a low impedance to the LO, thereby degrading the quality factor. Cost and/or frequency limitations evidently prohibited the use of a buffer between the two.

1963: The Gigahertz Barrier Is Conquered

As transistor manufacturing advanced, it was possible to improve its high-frequency characteristics. In the 1950s, radios operating up to 150 MHz were reported. But it was in the 1960s that “microwave” transistor circuits began to appear. (The definition of the “microwave” frequency range has changed over the years.) Among the earliest is the six-stage amplifier shown in Figure 4(a) [7]. Incorporating a transistor type that exhibits 5 dB of gain at 2 GHz, the circuit relies on stripline structures for interstage matching (shown by inductor symbols). Also, the resistors in the top and bottom rails ensure low-frequency stability. As demonstrated in Figure 4(b), the prototype provides a flat gain of about 32 dB from 1.1 GHz to 1.6 GHz. The author reports a noise figure (NF) of 6.2–8 dB in this range. Another example operating up to 1.7 GHz was presented in 1965 [8].

1968: An Integrated Bipolar RX Is Reported

By the late 1960s, bipolar technology had matured enough to accommodate tens of devices on the same chip. Using a process with $f_T = 1$ GHz and a minimum transistor geometry of $6 \mu\text{m}$, [9] reported in 1968 the FM RX shown in Figure 5. The stages consisting of Q_1 , Q_2 , and their feedback devices act as a transimpedance amplifier (TIA) according to today’s understanding. Moreover, Q_5 serves as a mixer and receives the LO through Q_6 . Interestingly, [9] first constructed a breadboard prototype of the RX to identify potential problems before proceeding with chip fabrication.

1966–1969: RF CMOS Is Born

The use of MOSFETs for RF applications is not as recent as one might think. In 1966, a master’s thesis from

the U.S. Naval Postgraduate School describes a MOS PA [10]. As depicted in Figure 6, the PMOS class-C stage is analyzed, and an efficiency of 57% is predicted for a 15-mW output.

In 1968, two developments brought MOSFETs farther into RF design. Rafuse proposed the double-balanced mixer shown in Figure 7(a) [11], demonstrating a 40-dB improvement in the dynamic range over the conventional diode topology. The mixer achieved a sensitivity of -120 dBm in a 1-kHz bandwidth with a signal-to-noise ratio of 10 dB. This result corresponds to an NF of 14 dB. Moreover, Ikeda reported the oscillator shown in Figure 8(a),

which was “designed to use integrated circuit fabrication techniques” [12]. Ikeda viewed the topology as a Colpitts structure wherein transistor T_2 replaces the capacitor that would be tied between the drain and source of T_1 . Alternatively, we recognize T_1 and T_2 as a cross-coupled pair if we include another tank in the drain of the latter. Presented in Figure 8(b) is a similar arrangement reported in the 1990s [13].

One may argue that the foregoing examples do not represent true RF CMOS circuits as they incorporate discrete transistors. But, in 1969, under a contract with the U.S. Army,

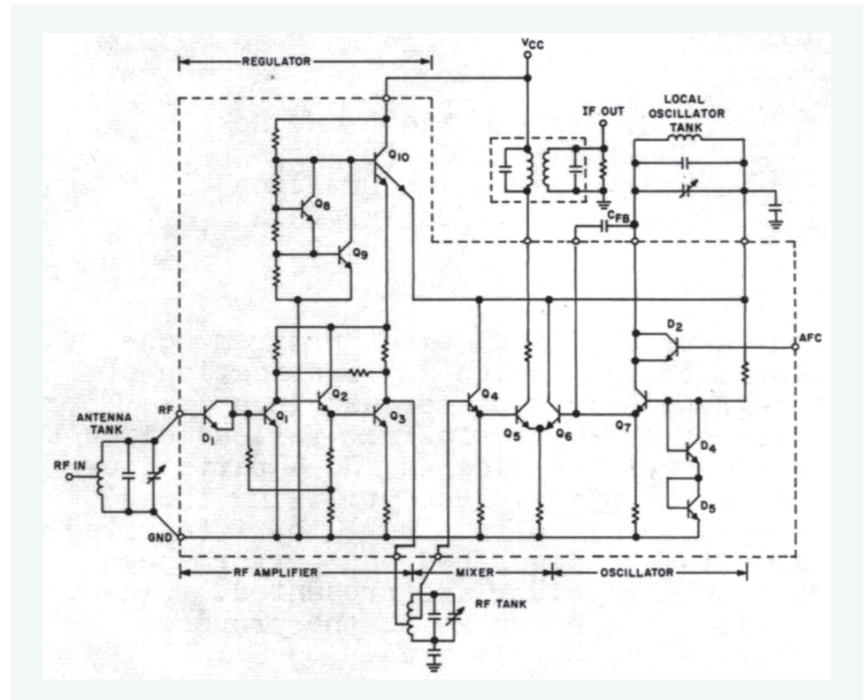


FIGURE 5: An integrated RX from 1968 [9]. GND: ground.

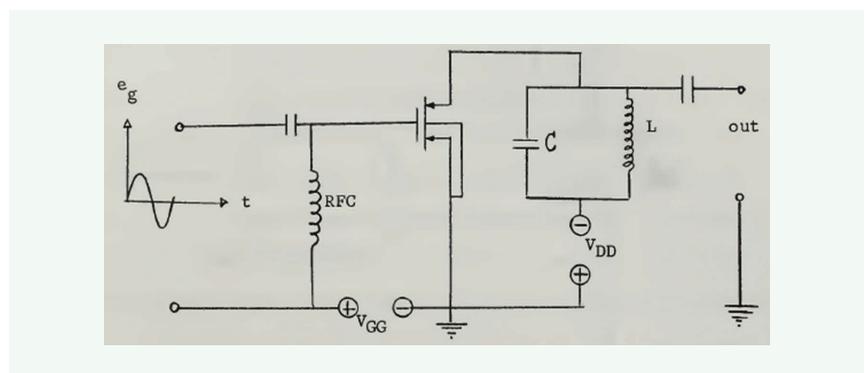


FIGURE 6: A CMOS PA from 1966 [10]. RFC: radio-frequency choke.

RCA developed the RX shown in Figure 9(a), where dual-gate PMOS transistors Q_1 – Q_7 were grown on the same substrate [14]. Transistor Q_1 acts as a cascode low-noise amplifier (LNA), and Q_2 as a mixer. Figure 9(b) shows the chip photograph. Targeting military FM radios in the range of 30–76 MHz, the chip takes advantage of diode-connected transistors Q_3 – Q_7 to define the bias points of Q_1 and Q_2 . (Note that V_S is a positive supply voltage.) In fact, a closer examination reveals that Q_6 and Q_2 form a current mirror. RCA’s report also recommends that the LO be integrated

on the same chip in future work. Unfortunately, RF CMOS would lie dormant for about two decades.

Mixing: Nonlinearity Versus Time Variance

Much of the early work on RF systems considered mixing as the time-domain multiplication of two waveforms in a nonlinear circuit. Approximated by a polynomial of the form $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots$, the characteristic would sense the sum of the RF signal and the LO and generate their product through even-order nonlinearity.

In 1963, however, Read proposed that “any device in which mixing occurs can be represented by a linear network with time-varying components” [17]. In fact, Read assumed that a transistor’s current resembled a square wave and hence computed the conversion gain.

The significance of “time-variant” mixers was not appreciated until later in that decade. Over the years, it was discovered that 1) the RF port of a mixer must be linear to withstand blockers or at least preserve the information in an AM signal and 2) the LO port must switch abruptly and completely so as to provide a high gain and low NF. One could argue that the dual-gate mixer in Figure 9(a) exemplifies such an implementation, but [14] does not teach these principles. These points emerged only as the spectrum became more crowded and RF interferers more abundant. The need for a mixer with one linear port and one switching port was fulfilled by Bilotti and Pepper [18], as explained in the next section.

Bilotti Versus Gilbert

In an article published in 1967, Bilotti and Pepper present the circuit depicted in Figure 10(a), recognizing the need for complete switching in the LO path [18]. They assume a small signal level arriving at the top transistors and apply the LO to the bottom pair. In the 1968 International Solid-State Circuits Conference (ISSCC), Bilotti reports the same topology but with the top devices acting as switches and the bottom ones degenerated for high linearity [Figure 10(b)] [19]. At the same conference, Gilbert offers the topology shown in Figure 10(c), where both ports are linear [20]. We note that Bilotti upholds the two principles described in the previous section and should be credited for the double-balanced active mixer used today. Bilotti also explains that the double-balanced arrangement cancels the LO component at the output.

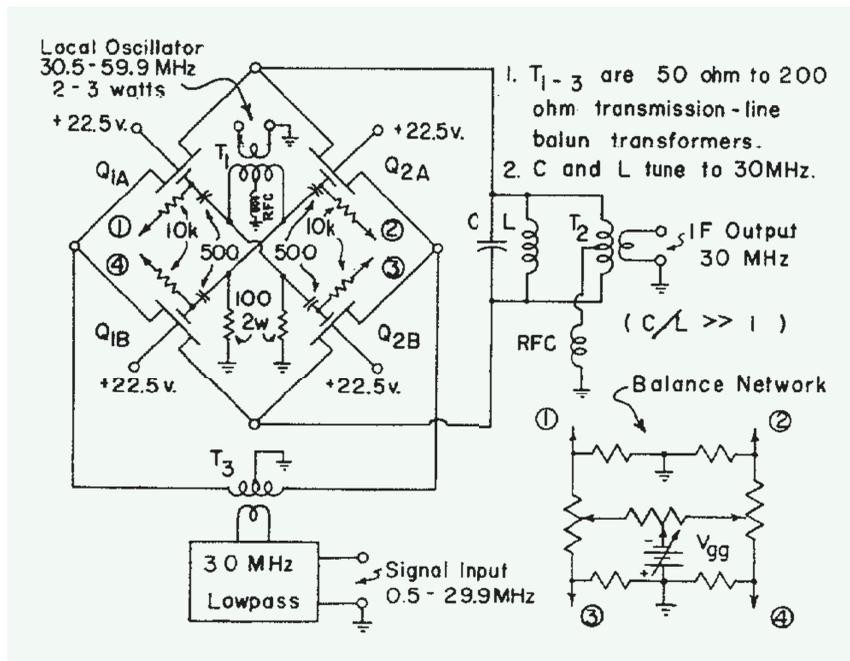


FIGURE 7: A CMOS mixer from 1968 [11].

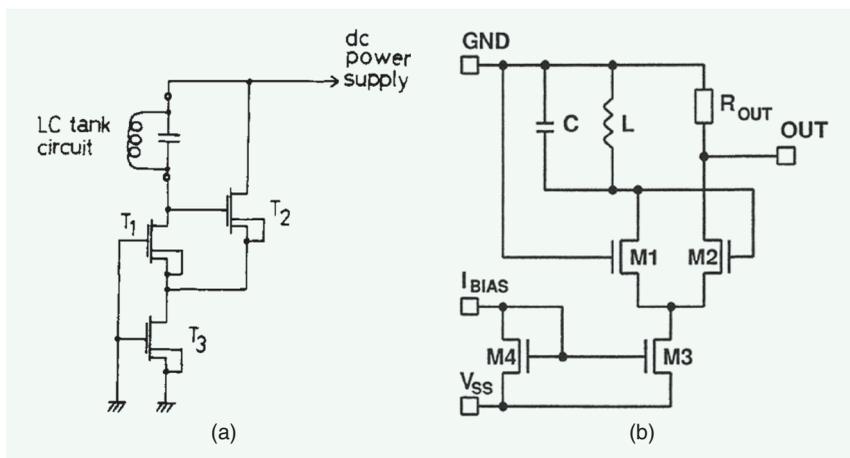


FIGURE 8: (a) A CMOS oscillator from 1968 [12] and (b) its counterpart from 1994 [13].

1970: SPICE Is Born

The development of SPICE at the University of California, Berkeley, in 1969 and 1970 has had a profound and long-lasting impact on the semiconductor industry. In addition to eliminating guesswork and tweaking from “breadboard” implementations, SPICE also changed the designers’ empirical mindset to a methodical and rigorous approach.

While analog designers welcomed SPICE, traditional RF and microwave engineers did not readily embrace it and preferred tools such as COMPACT [15] for analysis and design [16]. Nonetheless, SPICE would eventually lead to a paradigm shift in RF design; the reproducibility afforded by extensive SPICE simulations meant that the stages in an RF chain did not need to (and should not) be individually

matched and optimized, a point to which we return later.

1975: Class-E PA Is Born

Recall that polar modulation relies on an efficient nonlinear PA. Even if the input of such a stage is driven by a square wave, the output suffers from slow transitions and resembles a sinusoid because it delivers a current to an RLC tank. Thus, it is difficult

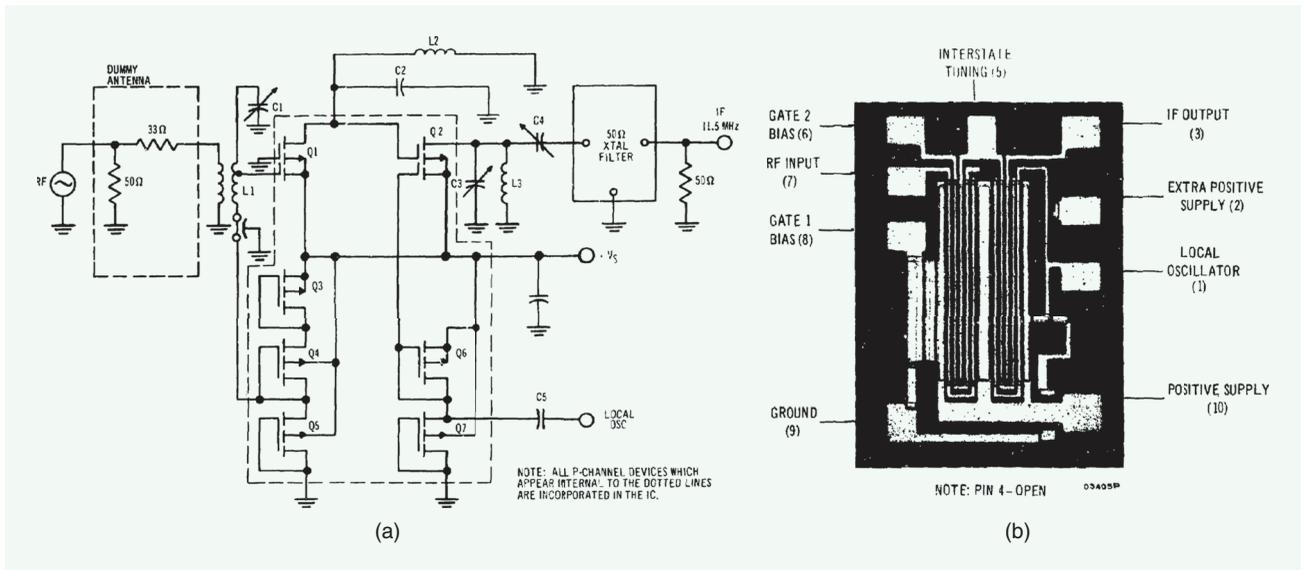


FIGURE 9: (a) A CMOS RX from 1969 [14] and (b) its die photograph.

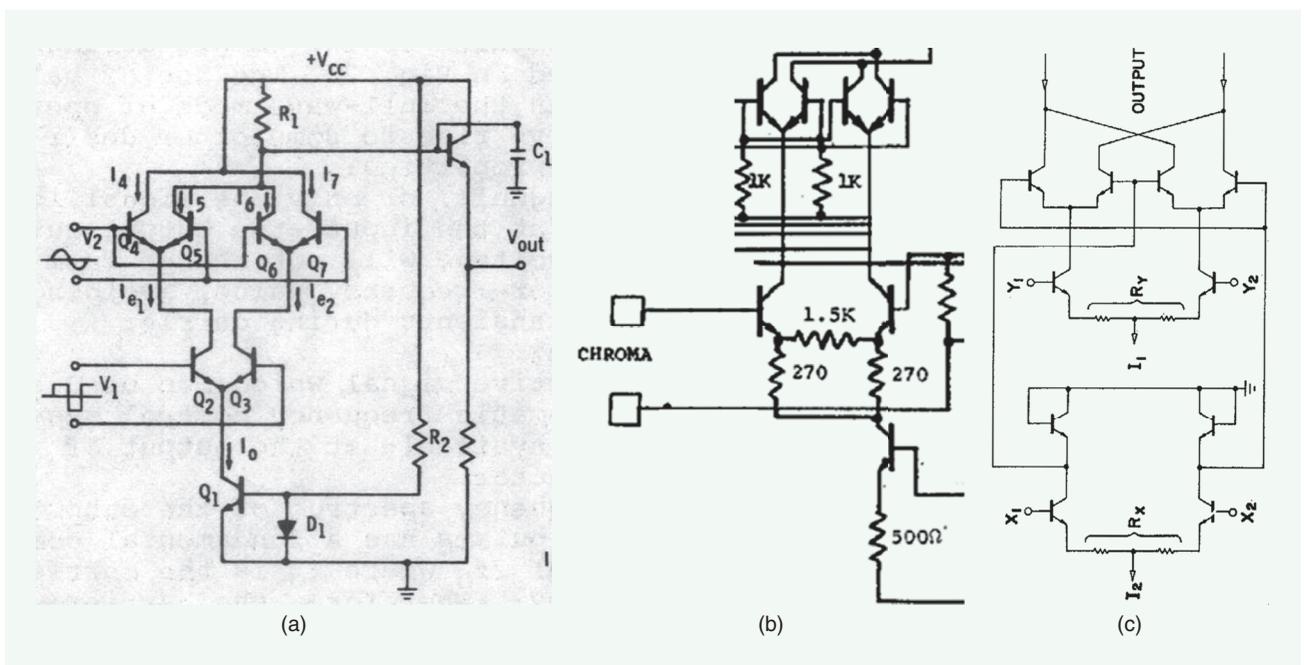


FIGURE 10: (a) A mixer reported by Bilotti and Pepper [18] in 1967, (b) an improved mixer reported by Bilotti [19] in 1968, and (c) a multiplier proposed by Gilbert [20] in 1968. (Parts of diagrams omitted for clarity.)

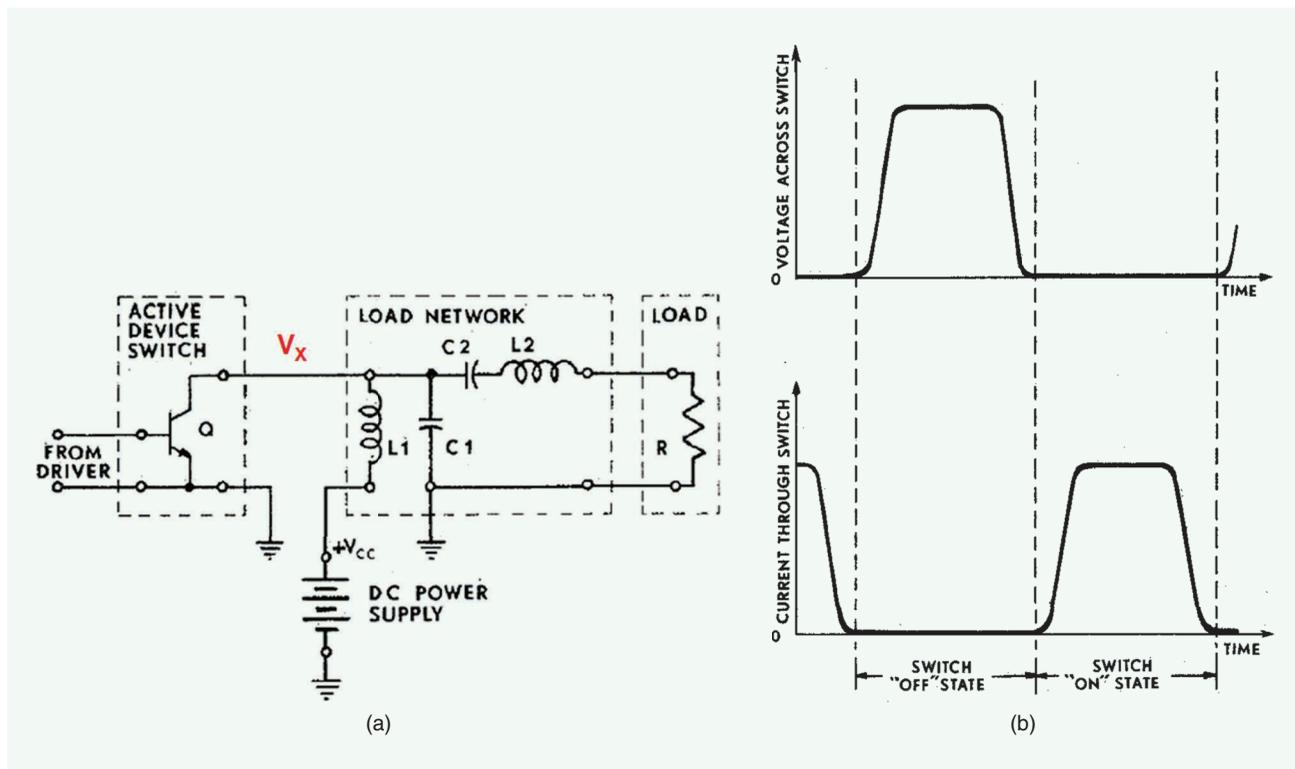


FIGURE 11: (a) The class-E stage proposed by Sokal and Sokal [21] and (b) its nonoverlapping current and voltage waveforms. (Red text added for illustration.)

to ensure that the PA transistor dissipates minimal power.

In 1975, Sokal and Sokal proposed the class-E PA topology for efficient switching [21]. As depicted in Figure 11(a), the circuit strives for nonoverlapping current and voltage waveforms [Figure 11(b)] and deals with finite input and output transition times by proper load design. The output network is selected such that V_x satisfies three conditions.

- 1) As the switch turns off, V_x remains low long enough for the current to drop to zero.
- 2) V_x reaches zero just before the switch turns on.
- 3) dV_x/dt is also near zero when the switch turns on.

The class-E stage achieves a theoretical efficiency of 100%, a considerable advantage over other nonlinear PA topologies. The circuit has been used extensively [22], [23], [24] [25].

1980: An Integrated Direct-Conversion RX Is Reported

Direct-conversion receivers date back to the 1950s [88] but had faced severe practical issues. In 1980, Vance described the RX shown in Figure 12, which was integrated in an 800-MHz bipolar process [34]. Targeting FM reception, the chip consists of quadrature signal paths, each containing its own LNA, an oscillator followed by a passive 90° phase shift network, and a dual-modulus frequency divider. This chip is followed by external passive channel-select filters and then by another chip that performs detection and further processing.

Vance makes a profound prediction: "the combination of direct conversion and large-scale integration is a very powerful means for future development of radio receiver techniques." Vance also addresses direct-conversion issues in great detail and explains, for example, that 1) differential RF paths minimize LO leakage to the antenna, 2) a quadrature phase error of 10° is maintained, and 3) no significant interaction is observed

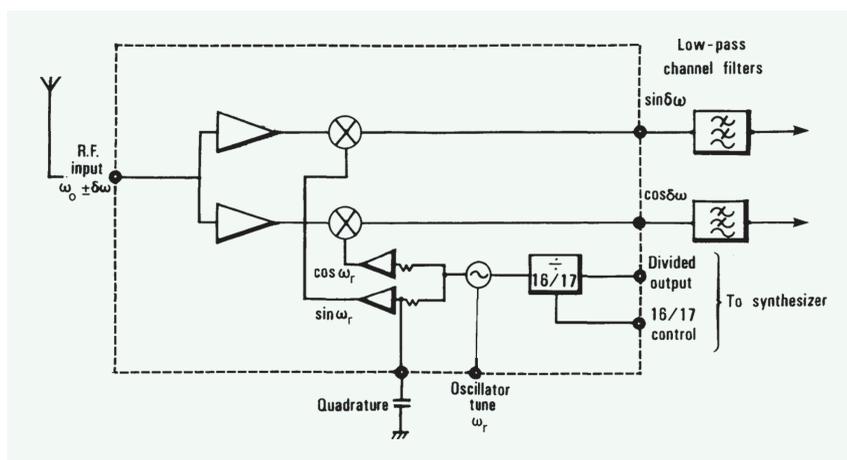


FIGURE 12: An integrated direct-conversion RX from 1980 [34].

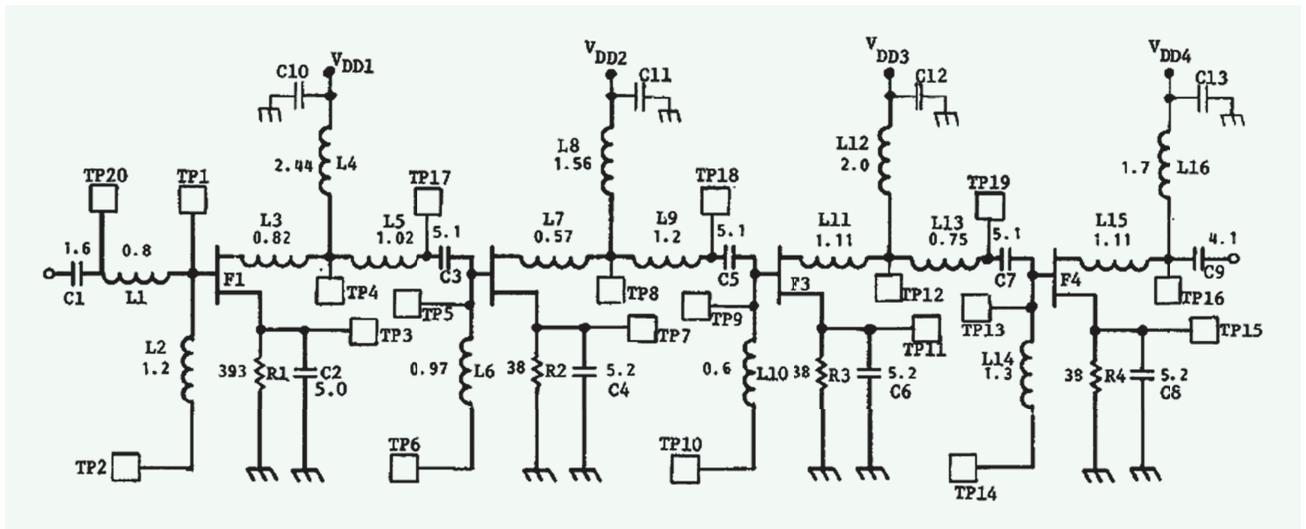


FIGURE 13: An LNA with interstage matching [35]. TP: test point.

between the analog and digital portions of the chip.

Invasion of Analog Designers

As the mobile phone began to find popularity in the late 1980s, manufacturers focused on its cost, form factor, and power consumption. Traditional RF design in the gigahertz range had relied upon various factory trims and adjustments and was ill-prepared for mass production of low-cost chips. Concerns such as process, voltage, and temperature (PVT) variability were not addressed, and the low yield of III-V (e.g., GaAs) wafers exacerbated the problem. As an example, consider the integrated LNA shown in Figure 13 and targeting a 2-GHz band around 7 GHz [35]. We observe a number of issues here.

- 1) The bias currents are not established by current mirrors and can vary substantially with PVT.
- 2) The circuit draws more than 700 mW.

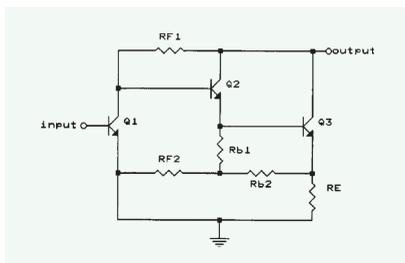


FIGURE 14: An integrated 1-GHz LNA from 1989 [36]

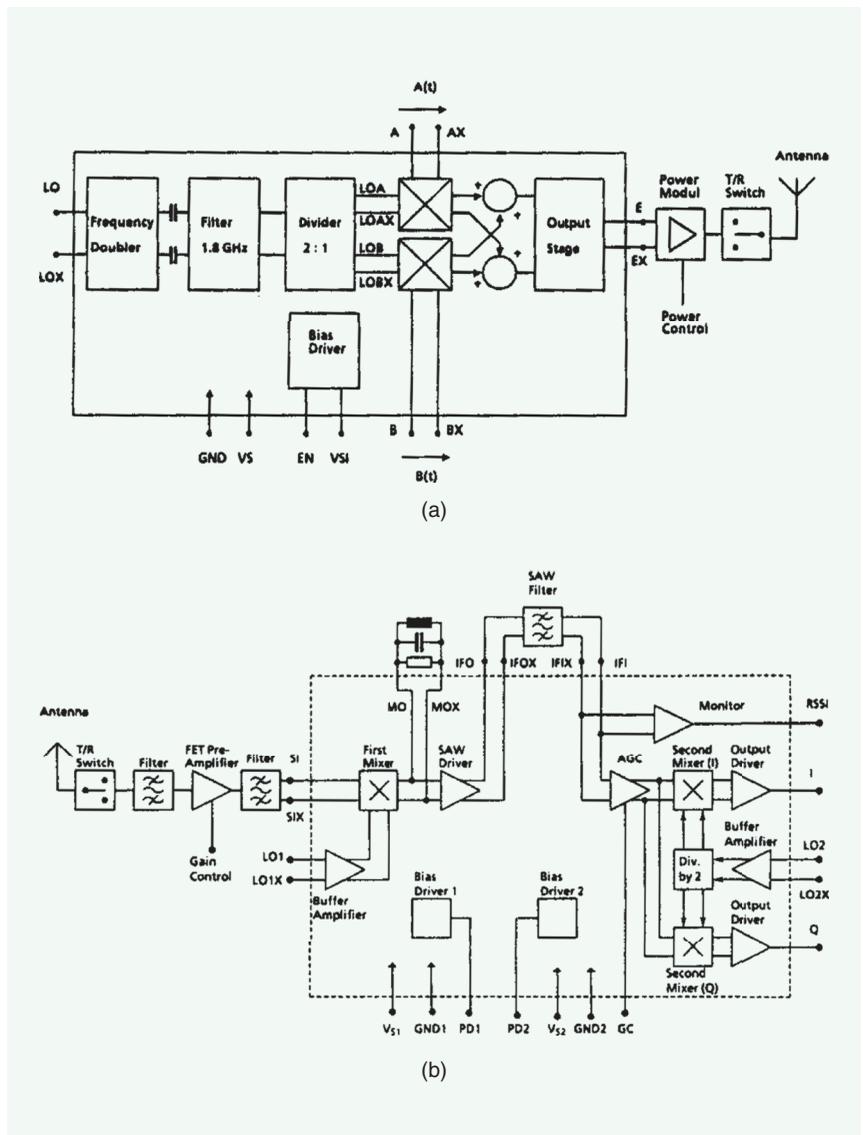


FIGURE 15: Siemens's 1990 (a) TX and (b) RX paths [41]. Div.: divider.

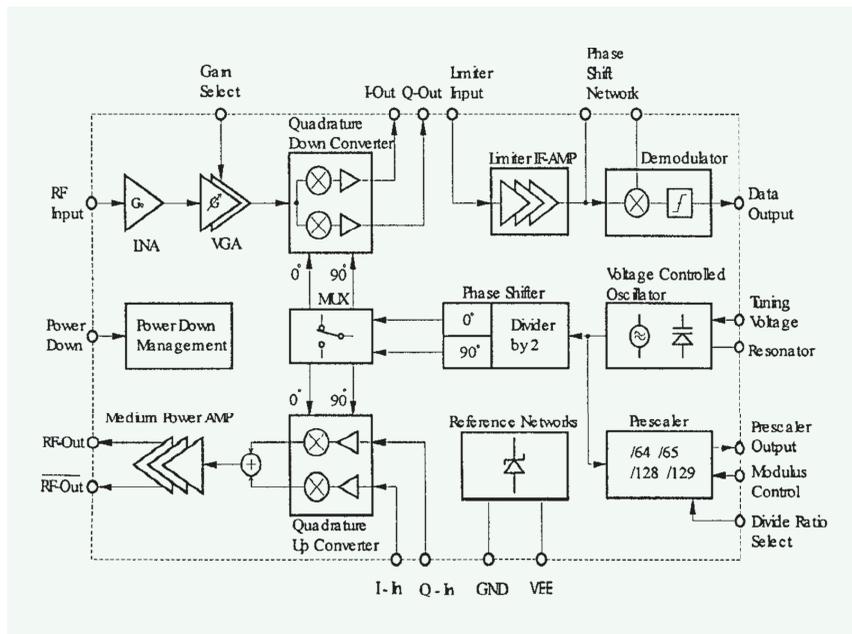


FIGURE 16: Siemens' 1994 direct-conversion transceiver [42].

3) The authors explain that “the impedance match at the input and output of an amplifier must be reasonably good” and hence apply matching between every two stages.

It was against this backdrop that analog designers became interested in RF systems. Having dealt with the mass production of fairly complex bipolar and CMOS circuits—albeit operating at lower frequencies—they were trained to aim for a high yield and tackle PVT issues by on-chip techniques such as bandgap references, current mirrors, differential operation, etc. They furthermore relied on SPICE for simulations.

Facing the low quality of spiral inductors in silicon processes, analog designers also wondered whether

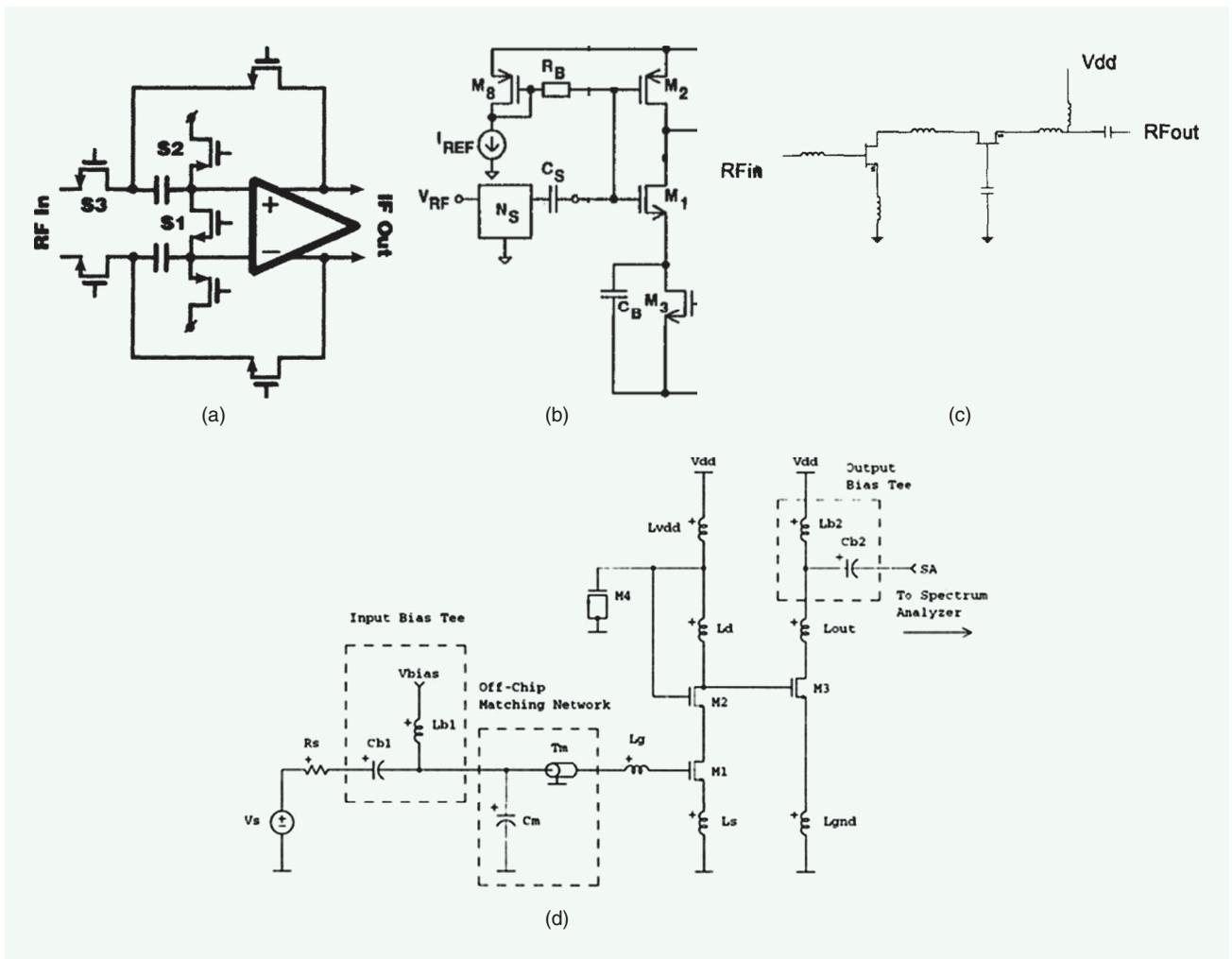


FIGURE 17: (a) A CMOS mixer from 1993 [43], (b) an inverter-based LNA from 1996 [44], (c) a MESFET LNA from 1993 [45], and (d) a CMOS LNA from 1996 [46]. (Parts of diagrams omitted for clarity.)

interstage matching was necessary in RF transceivers. One can observe some of this mentality in the integrated receivers of Figures 5 and 9. Shown in Figure 14 is another example of LNA design without matching (except at the input) [36], achieving an NF of less than 3 dB at 1 GHz. As explained later, modern RF receivers have completely departed from interstage matching and prefer a *high* output impedance for the LNA and a *low* input impedance for the downconversion mixers.

1986–1988: RF CMOS—Again

With the integration abilities of MOS processes on the rise, RF MOS circuits were revisited in 1986 and 1987. Song reported mixers and phase shift networks realized in 1.75- μm CMOS technology [37]. Additionally, Jindal described an NMOS LNA with gain control that exhibited an NF of about 11 dB at 1.5 GHz [39]. Moreover, Toh et al. proposed an NMOS amplifier achieving a bandwidth of 760 MHz and an NF of 6.7 dB [38]. Also, a balanced modulator was disclosed by Garverick and Sodini [40]. RF CMOS still failed to find traction with the market.

1990s: High Integration and RF CMOS—Third Time Is a Charm

The 1990s witnessed explosive growth in RF design, primarily fueled by the cellular and cordless phone market. High integration levels naturally led to a lower cost and smaller form factor, but these radios' exacting performance requirements presented numerous difficulties. RX dynamic range and blocker rejection, TX output power, and synthesizer phase noise were among the daunting challenges.

An early example of such endeavors was reported by Siemens in 1990 [41]. Shown in Figure 15 are the 900-MHz direct-conversion TX and the heterodyne RX. Designed for both linear and nonlinear modulation schemes used in cellular standards such as Global System for Mobiles (GSM) and Advanced

Mobile Phone System (AMPS), the radio still relied on external LOs.

Siemens followed this work with a direct-conversion transceiver in 1994 [42]. As depicted in Figure 16, the bipolar radio includes an on-chip LO but employs external channel-select filters. In the same time frame, AT&T

Bell Labs reported a bipolar GSM radio as well [86], and so did Philips [87].

While product development grappled with cellular radios' stringent demands, research turned its attention to RF CMOS. A slew of building blocks were introduced that demonstrated the potential of CMOS technology.

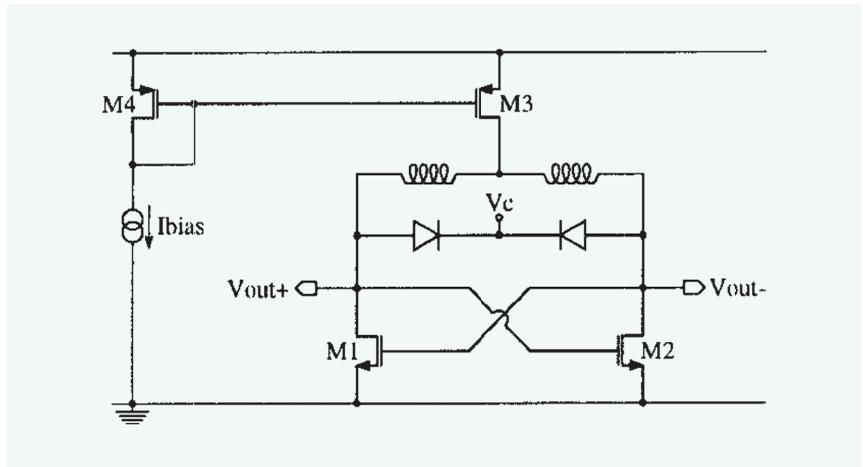


FIGURE 18: A CMOS LC VCO from 1996 [47].

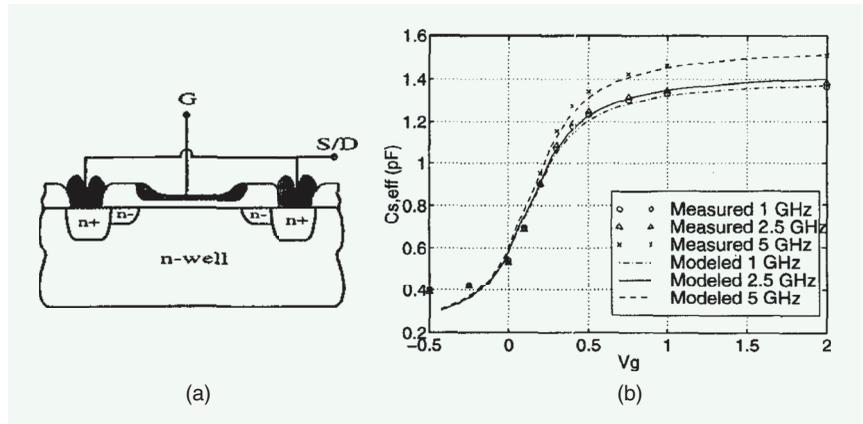


FIGURE 19: (a) The MOS varactor structure and (b) its characteristics [48].

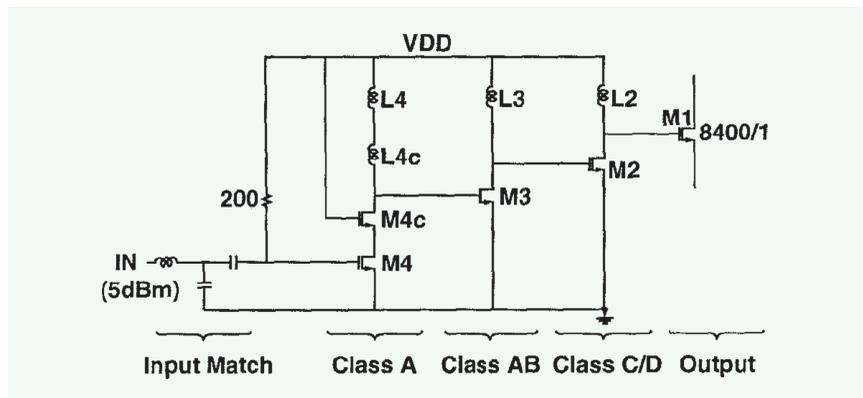


FIGURE 20: A CMOS PA from 1997 [49].

Illustrated in Figure 17(a) is a 900-MHz subsampling mixer reported in 1993 [43] achieving a third-order intercept point of +27 dBm and an NF of 18 dB. Figure 17(b) shows a 900-MHz inverter-based LNA with NF = 2.2 dB [44]. A cascode LNA structure using inductive degeneration had been reported in MESFET technology in 1993 [45] [Figure 17(c)]. A CMOS counterpart followed in 1996

[46] [Figure 17(d)]. Another example was reported in [28].

Low-noise LC voltage-controlled oscillators (VCOs) were also of great interest, motivating extensive work both on their circuit topologies and on improving the quality factor of inductors. Figure 18(a) shows a VCO using *pn*-junction diodes for tuning [47]. The phase noise is -116 dBc/Hz at a 600-kHz offset with a power

consumption of 6 mW. This work recognizes that inductors reach a higher *Q* if their shape approaches a circle, offering octagonal geometry as an approximation. Also important is the authors' observation that the inner turns of a spiral degrade the *Q* due to the skin effect while contributing little inductance. We follow both of these principles in today's inductor designs.

A key development in this decade was the invention of the MOS varactor in 1998 [48]. As shown in Figure 19(a), the device is formed by placing an NMOS transistor within an n-well so as to obtain a monotonic capacitance-voltage (*C-V*) characteristic [Figure 19(b)]. A key property here is that the *C-V* plot scales with the technology (i.e., the gate oxide thickness), allowing low-voltage design. This stands in contrast to the unscalable behavior of *pn*-junction varactors.

Other RF building blocks materialized in CMOS technology as well. In 1994, 1.6-GHz dual-modulus prescalers were reported [84], and in 1995, they reached a speed of 1.8 GHz [85]. In 1997, the 2.5-V 1-W PA shown in Figure 20 was reported [49]. Implemented in a 0.8- μm process, the 850-MHz prototype exhibits a small-signal gain of 30 dB and a power-added efficiency of 42%. Only the matching network driven by M_1 is off chip.

RF CMOS design has owed a considerable part of its success to the extensive device modeling efforts undertaken in that time period (and later). The noise behavior of MOS devices and loss mechanisms in inductors and varactors were among the critical effects that eventually lent themselves to accurate models.

The next phase in RF CMOS research dealt with system design, namely, receivers, transmitters, and synthesizers. Figure 21(a) depicts a 900-MHz RX example employing a low-IF topology [50] achieving a total gain of 9.2 dB and an NF of 24 dB. Figure 22 shows a 900-MHz TX delivering an output power of +5 dBm [51]. A 1.8-GHz synthesizer was also described in [52].

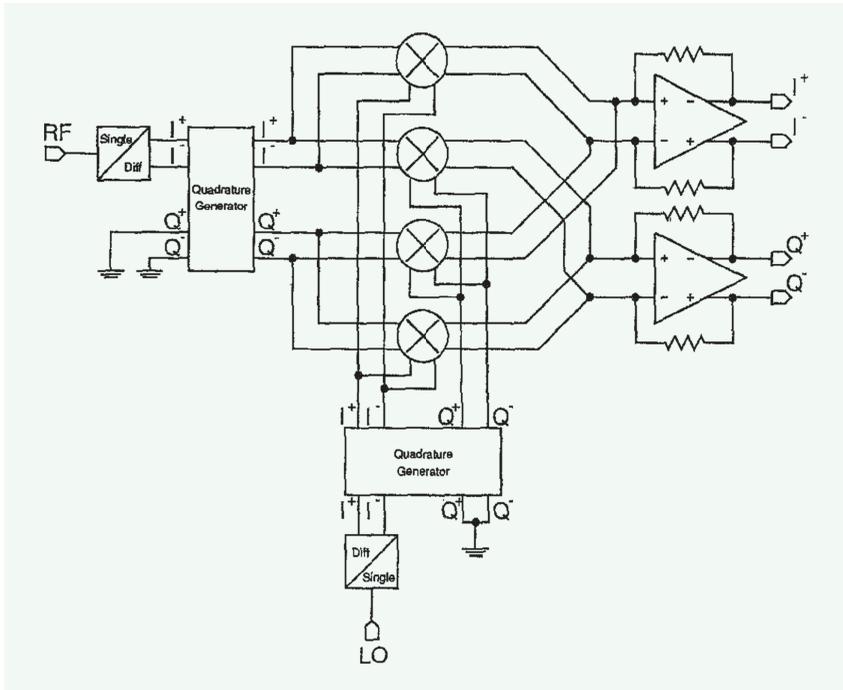


FIGURE 21: A CMOS RX from 1995 [50].

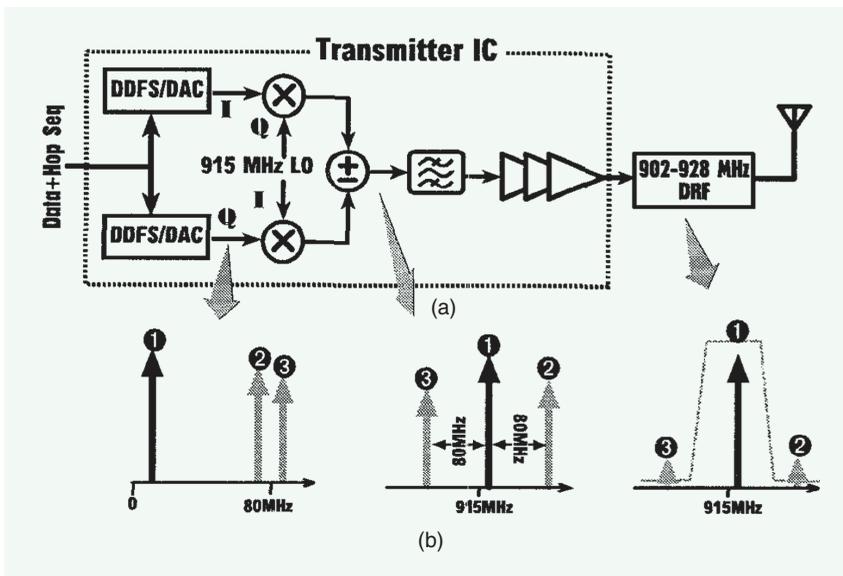


FIGURE 22: A CMOS TX from 1996 [51]. Seq.: sequence.

1993: The $\Delta\Sigma$ Fractional- N Synthesizer Is Born

An inflection point occurred in RF synthesis when Riley et al. introduced the use of $\Delta\Sigma$ modulators for the randomization and noise shaping of a synthesizer's feedback divide ratio [53]. In contrast to previous analog-intensive fractional- N techniques, this approach offered a robust and elegant means for fine frequency control (Figure 23). Here, the divider generates an output frequency given by

$$f_d(t) = \frac{f_0}{N} \quad (1)$$

$$= \frac{f_0}{n + b(t)} \quad (2)$$

where $b(t)$ is a random noise-shaped stream generated by the $\Delta\Sigma$ circuit. The idea swiftly found its way into CMOS synthesizer design [54], [55] [56]. Today's phase-locked loops (PLLs) must often rely on this concept so as to achieve a high-frequency resolution and/or operate with different crystal frequencies.

Direct Conversion in CMOS

Owing to various issues plaguing direct conversion [57], [58], early

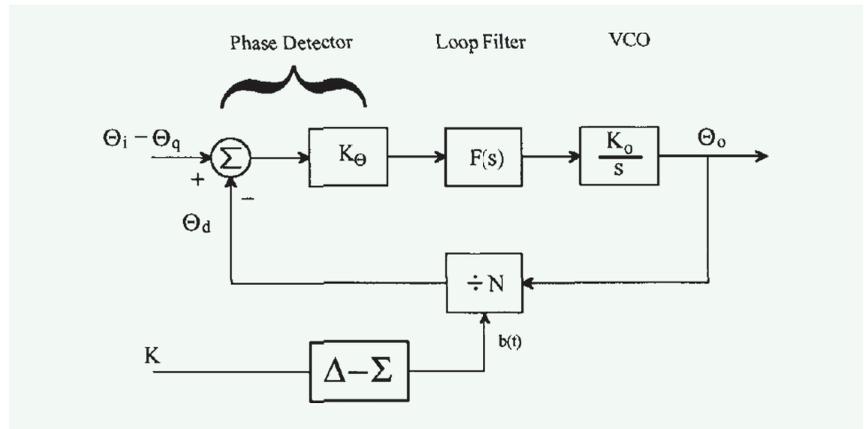


FIGURE 23: The $\Delta\Sigma$ modulator proposed by Riley et al. [53].

CMOS RXs were based on the heterodyne architecture [50], [59], [60], [61]. Flicker noise in the baseband, generation of quadrature LO phases at high frequencies, and LO leakage to the antenna were among the chief challenges. In 1997, a 900-MHz direct-conversion RX in 0.6- μm CMOS technology was introduced [62]. Shown in Figure 24(a), the system includes an LNA, downconversion mixers, baseband amplifiers, a 1.8-GHz LC oscillator, and a $\div 2$ stage providing quadrature LO phases. The design suppresses the baseband flicker noise by including a gain of 35 dB in

the LNA and the mixers. As illustrated in Figure 24(b), the RX front end applies capacitive coupling between the mixer's transconductor (M_4) and switching pair (M_5 and M_6) so as to allow a greater voltage headroom for the former and hence improve its linearity. The RX exhibits an NF of 4 dB, a voltage gain of 55 dB, and an LO leakage of -65 dBm.

Direct conversion continued to flourish, appearing again in 1998 [64] and in 1999 [65], [63]. Shown in Figure 25 is the 900-MHz transceiver reported in [63] for cordless phones. It incorporates channel-selection

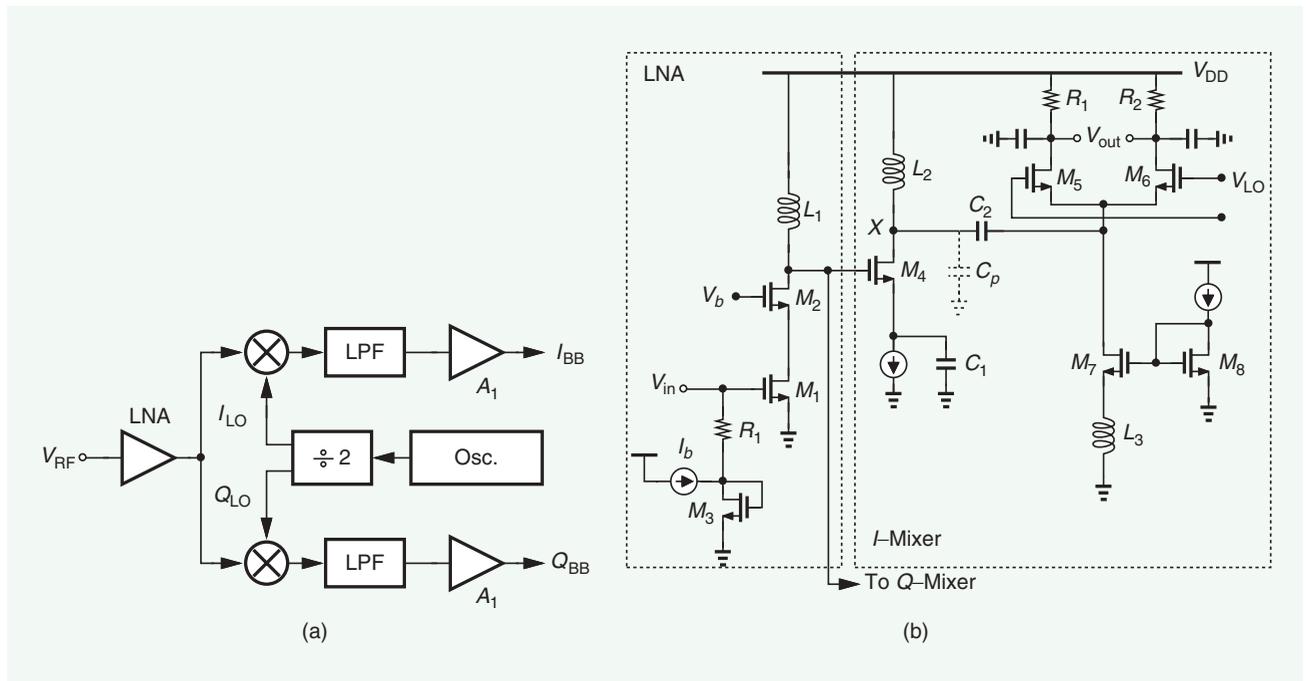


FIGURE 24: (a) A direct-conversion CMOS RX from 1997 [62] and (b) its front-end implementation.

filtering and offset cancellation in the RX path. It also directly modulates the synthesizer output and applies

the signal to an on-chip PA. The RX offers an NF of 4.5 dB, and the TX delivers an output power of +14 dBm.

1995: Cadence Introduces a Noise Simulator for Time-Variant Circuits

As explained earlier, RF mixers were eventually viewed as linear time-variant circuits. Unfortunately, SPICE lacked the ability to analyze noise in such structures. A similar situation arose as we discovered that LC oscillators benefit from complete switching of their cross-coupled transistors. The analysis and design of mixers and oscillators thus proved difficult. While tools such as EESOF's TOUCHSTONE offered nonlinear noise analysis by means of harmonic balance techniques, none had the ability to deal with CMOS circuits.

In 1995, Cadence Systems responded to this need by introducing SpectreRF [66], [67]. The tool computed the circuit's large-signal periodic steady-state properties and, through another routine called *periodic noise (pnoise)*, determined how much noise was injected by the devices at each point on a waveform. SpectreRF took the guesswork out of mixer and oscillator design, making it possible for RF engineers to explore new topologies and quantify their performance tradeoffs.

2000s: Direct Conversion Matures

With the confidence gained by designers in the abilities of CMOS technology—and their desire to avoid off-chip components—a new wave of work was undertaken in the 2000s to make direct conversion manufacturable. Great efforts were expended on understanding and correcting this architecture's imperfections [68], [69], [70], [71]. Particularly noteworthy from this era are two papers that advocate the use of current-driven passive mixers followed by TIAs [72], [73]. As exemplified by the topology shown in Figure 26 [73], such mixers exhibit much lower flicker noise and, by virtue of the TIA's virtual-ground inputs, much higher linearity. This structure has formed the foundation for today's RX design.

Work toward high integration continued as well. Several code-division

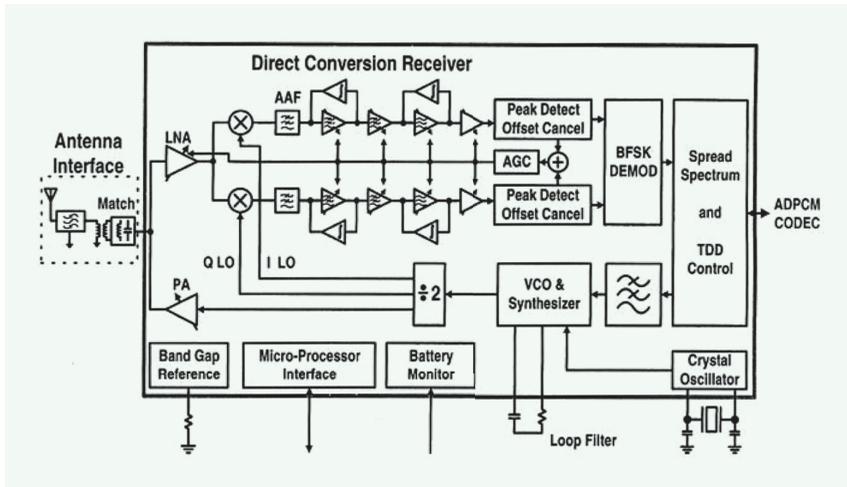


FIGURE 25: A CMOS direct-conversion transceiver reported in 1999 [63]. Demod.: demodulator.

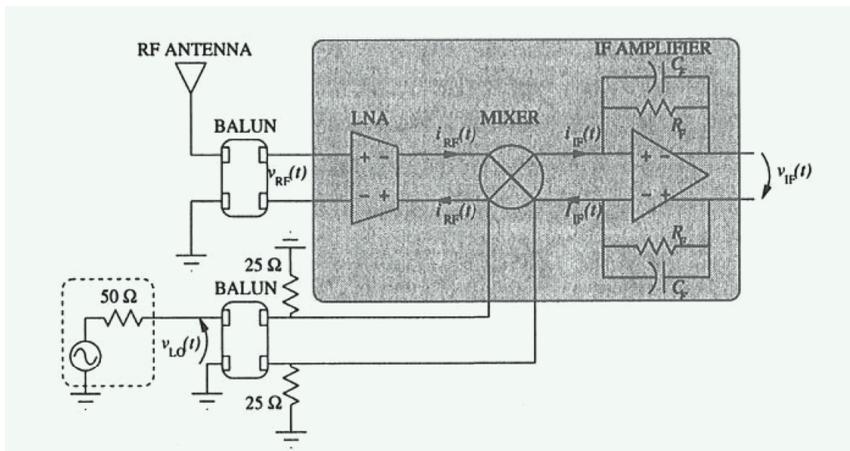


FIGURE 26: An RX chain consisting of a current-mode mixer and a TIA from 2003 [73].

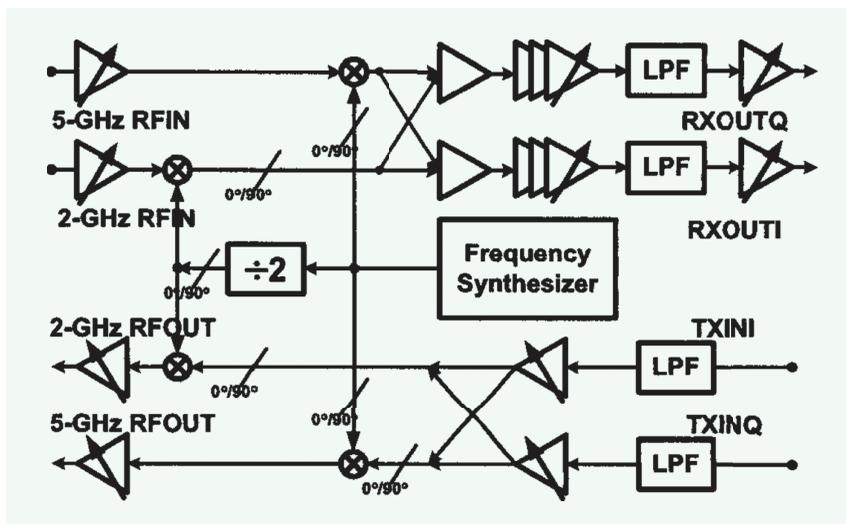


FIGURE 27: A 2.4-GHz/5-GHz direct-conversion transceiver reported in 2004 [78].

multiple access (CDMA) CMOS transceivers were reported [74], [75], [76], [77]. Similarly, direct conversion was applied to 2.4-GHz and 5-GHz wireless local area networks (WLANs) (called *Wi-Fi* today) [79], [80], [81]. In 2002, two highly integrated 5-GHz direct-conversion radios including on-chip synthesizers were reported [80], [82], and in 2004, dual-band *Wi-Fi* systems began to appear. Figure 27 shows an example [78] targeting the IEEE 802.11a/b/g standards and using a single synthesizer. The radio provides an RX NF of 5.5–6.5 dB, a TX output power of –3 to –5 dBm for 64QAM signals, and an integrated phase noise of 0.54° to 1°. By 2007, dual-band multiple-input, multiple-output (MIMO) transceivers aimed at the IEEE 802.11n standard had become a reality [83].

PAs

As the most power-hungry block in radios, PAs naturally prompted extensive investigations, calling for new circuits and architectures. Notable among these early efforts was the class-E CMOS topology reported in [22] and shown in Figure 28. This work's thought process begins by recognizing that the large output transistors need not be driven by the preceding stage in their entirety. That is, one can decompose these devices and drive part of them by themselves, as accomplished by the cross-coupled transistors in stage 2. Moreover, this pair can even be allowed to oscillate and hence be injection locked to the input signal. Interestingly, the cross-coupled pair also acts as two diode-connected devices for common-mode (CM) signals and provides CM stability, a property not recognized in [22]. The 1.8-GHz prototype achieved an efficiency of 41% while delivering 1 W. Many other new PA topologies followed [29], [30], [31], [32] [33].

UWB, Cognitive, WiGig, and 5G Radios

In the 2000s and 2010s, several types of new radios were conceived, intriguing researchers in industry and

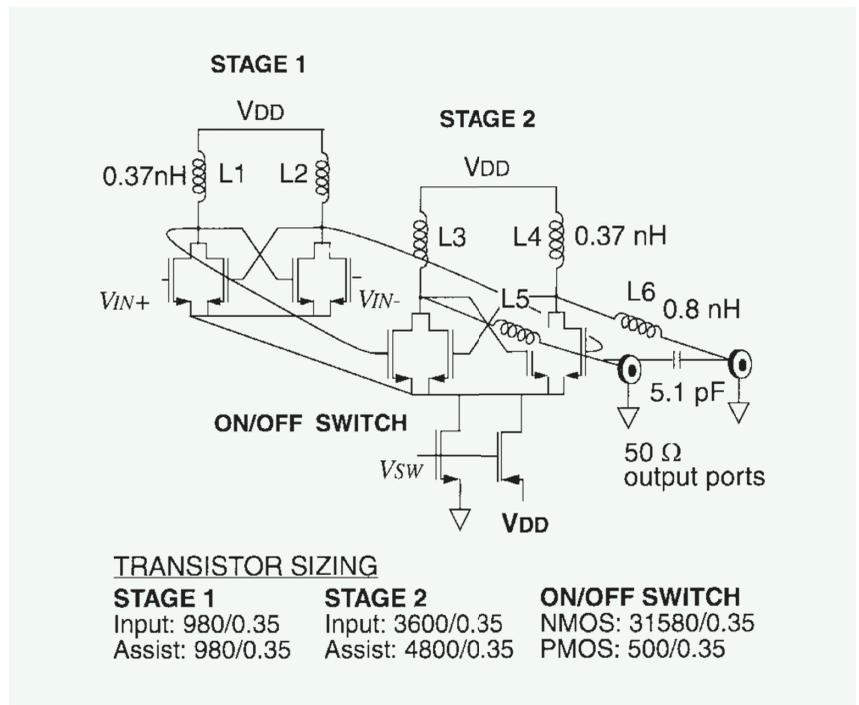


FIGURE 28: A class-E CMOS PA reported in 1999 [22].

academia. Ultrawideband (UWB) communication was viewed as a wireless link accommodating high data rates and hence as a good candidate for replacing the USB cable. After a great deal of work [89], [90], [91], [92], [93], it failed to find traction with the market. Cognitive radios aimed to identify and utilize any unoccupied RF channel for communication, but they, too, proved ill fated.

The unlicensed 60-GHz band presented another attractive medium

for high-throughput data transmission. Formalized by the WiGig standard, this approach motivated extensive work on pushing CMOS technology to high frequencies [94], [95], [96], [97], [98], [99], thus leading to impressive results. After nearly two decades of development, however, WiGig radios have not found a home and still appear to be a solution looking for a problem. Unfortunately, or fortunately, *Wi-Fi* continues to ascend to increasingly higher data

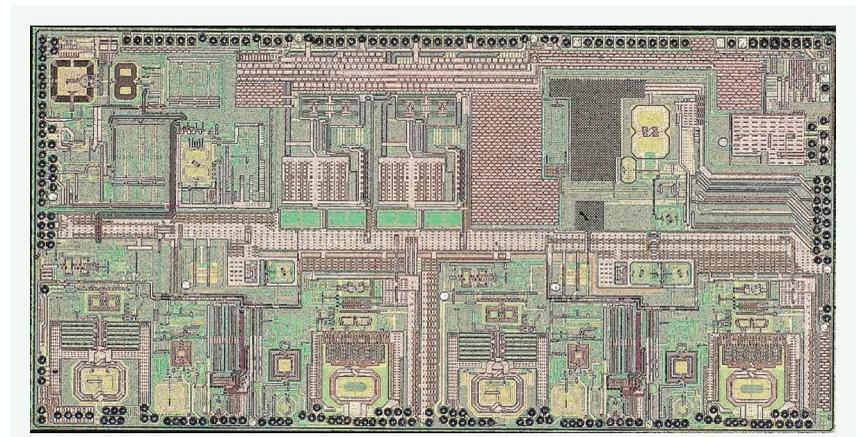


FIGURE 29: An example of a *Wi-Fi*/Bluetooth radio complexity. (Source: Courtesy of Realtek Semiconductor.)

Driven mostly by cellular and Wi-Fi markets, the progress in radios is no less astonishing than that of the semiconductor industry itself.

rates, thereby weakening the market for new radio standards.

The vast work on 60-GHz CMOS transceivers was readily leveraged to build 30-GHz radios for 5G cellular systems with the express purpose of achieving gigabit-per-second data rates. Also necessary here was the use of multiple transceivers for beamforming because the high path loss renders a single link fairly useless. Despite enormous research on 5G systems [100], [101], [102], [103], [104], it is unclear at this point whether their millimeter-wave links will play any significant role in the consumer market.

Multiband Multimode Radios Prosper

Perhaps the most remarkable development in RF design is the emergence of multiband multimode radios that meet the tough specifications of new cellular and Wi-Fi systems. The sheer complexity can be appreciated from the die photograph shown in Figure 29, which represents a 2x2 IEEE 802.11ax 2.4-GHz/5-GHz transceiver along with a Bluetooth radio.

Figure 30 shows an example of an LTE transceiver covering bands from 680 MHz to 6 GHz [105]. We observe the use of several RX front ends—as dictated by LNA bandwidths—as

well as two analog baseband chains before the signals arrive at analog-to-digital converters (ADCs). The same plan applies to the TX side. Two fractional-N PLLs provide the necessary LO frequencies. Also, the system allows loop-back operation between the TX and the RX so as to cancel the leakage and image of the former. The single-chip realization includes extensive processing in the digital domain, e.g., dc offset removal, I/Q gain and phase adjustment, and finite-impulse-response (FIR) filtering.

New generations of Wi-Fi have targeted ambitious data rates—up to about 10 Gb/s. With a basic channel bandwidth of 20 MHz, such data rates are accommodated by two methods: 1) channel “bonding,” i.e., transmitting one user’s data over multiple channels, and 2) high-order

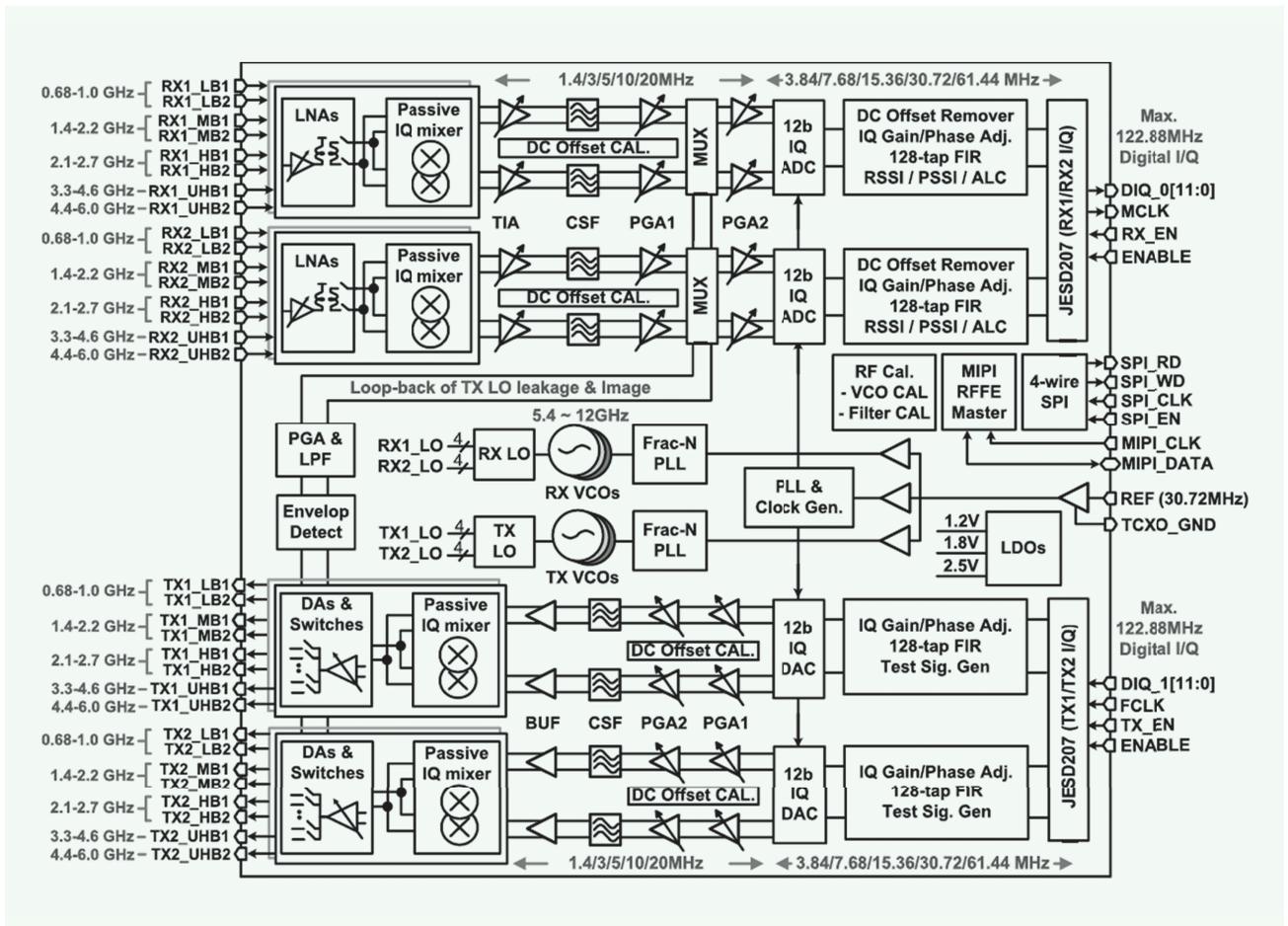


FIGURE 30: A multiband multimode LTE radio reported in 2018 [105]. Adj.: adjustment; Cal.: calibration; Sig.: signal; Gen.: generation; CLK: clock.

modulation, e.g., 1024QAM. It is even possible to bond channels from the 2.4-GHz band with those in the 5-GHz band. This, in turn, requires the concurrent operation of two radios, leading to a host of unwanted coupling issues between them. Consider, for example, the 4x4 dual-concurrent system depicted in Figure 31 [106]. Here, the 2.4-GHz and 5-GHz radios can operate simultaneously. Thus, the second harmonic of the former's TX can desensitize the latter's RX. Similarly, the concurrent operation of the synthesizers must deal with injection pulling between their oscillators.

Conclusion

This article has briefly described the journey that RF design has taken in the past 75 years and some of the key milestones that it has crossed. Driven mostly by cellular and Wi-Fi markets, the progress in radios is no less astonishing than that of the semiconductor industry itself. While most of us will not witness the next 75 years, we can expect much greater engineering marvels, from brain-to-brain wireless communication to distributed wireless sensors detecting wildfires.

References

[1] L. Terman, *Radio Engineering*, 3rd ed. New York, NY, USA: McGraw-Hill, 1947.

[2] A.P. Stern and J.A. Raper, "Transistor broadcast receivers," *Elect. Eng.*, vol. 73, no. 12, pp. 1107–1112, Dec. 1954, doi: 10.1109/EE.1954.6439142.

[3] R. L. Wallace, "Transistor amplifier circuits," U.S. Patent 2 652 460, Sep. 15, 1953.

[4] S. Li and G. M. Rebeiz, "A 130-151 GHz 8-way power amplifier with 16.8-17.5 dBm Psat and 11.7-13.4% PAE using CMOS 45nm RFSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Atlanta, GA, USA, 2021, pp. 115–118, doi: 10.1109/RFIC51843.2021.9490507.

[5] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952, doi: 10.1109/JRPROC.1952.273844.

[6] L. E. Barton, "An experimental transistor personal broadcast receiver," *Proc. IRE*, vol. 42, no. 7, pp. 1062–1066, Jul. 1954, doi: 10.1109/JRPROC.1954.274534.

[7] J. Hamasaki, "A wideband high-gain transistor amplifier at L-band," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, Feb. 1963, pp. 46–47, doi: 10.1109/ISSCC.1963.1157471.

[8] R. Engelbrecht and K. Kurokawa, "A wideband low noise L-band balanced transistor amplifier," *Proc. IEEE*, vol. 53, no. 3, pp.

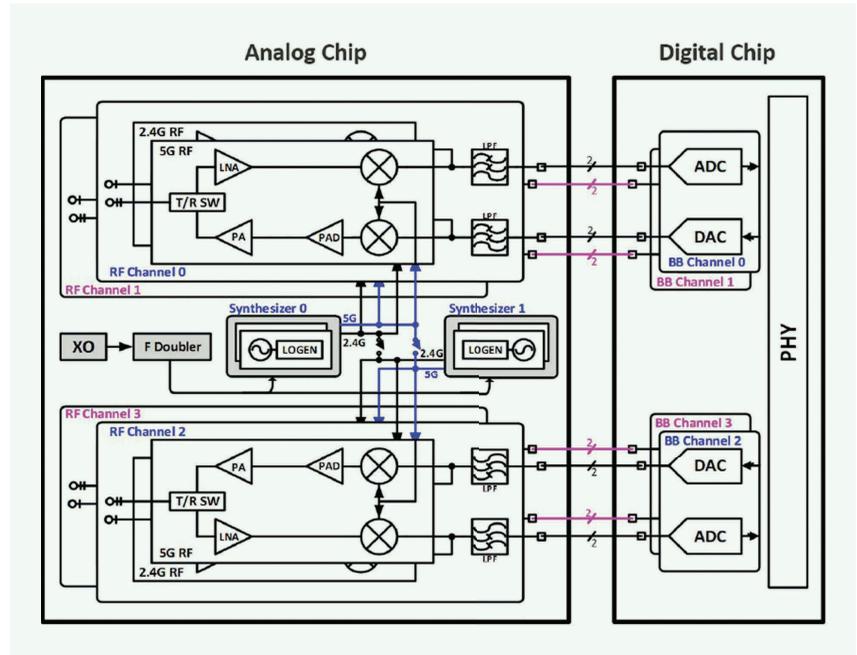


FIGURE 31: An IEEE 802.11ax radio reported in 2020 [106]. LPF: low-pass filter; PAD: PA driver; SW: switch.

237–247, Mar. 1965, doi: 10.1109/PROC.1965.3681.

[9] P. Hermann, L. Hoke, R. Petrosky, and R. Wood, "AM/FM monolithic receivers," *IEEE Trans. Broadcast. Telev. Receiv.*, vol. 14, no. 2, pp. 95–103, Jul. 1968, doi: 10.1109/TBTR1.1968.4320134.

[10] P. W. Sim, "Application of field-effect transistors to RF power generation," M.S. thesis, U.S. Naval Postgraduate School, Monterey, CA, USA, May 1966.

[11] R. P. Rafuse, "Symmetric MOSFET mixers of high dynamic range," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, Feb. 1968, pp. 122–123, doi: 10.1109/ISSCC.1968.1154637.

[12] H. Ikeda, "An MOS transistor RF oscillator suitable for MOS-IC," *Proc. IEEE*, vol. 56, no. 9, pp. 1638–1640, Sep. 1968, doi: 10.1109/PROC.1968.6694.

[13] P. Baseadeau and Q. Huang, "A 1-GHz, 1.5-V monolithic LC oscillator in 1-um CMOS," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 1994, pp. 172–175.

[14] R. H. Dawson and S. Katz, "Linear integrated circuits (Field Effect RF Amplifier/Mixer Integrated Circuits)," Defense Technical Information Center, Fort Belvoir, VA, USA, Final Report, RCA Electronics Components, Accession Number: AD0861267, 1969.

[15] L. Besser, F. Ghoul, and C. Hsieh, "Computerized optimization of transistor amplifiers and oscillators using 'COMPACT,'" in *Proc. 3rd Eur. Microw. Conf.*, Sep. 1973, pp. 1–4, doi: 10.1109/EUMA.1973.331614.

[16] C. Hsieh and S. Chan, "A feedforward S-band MIC amplifier system," *IEEE J. Solid-State Circuits*, vol. 11, no. 2, pp. 271–278, Apr. 1976, doi: 10.1109/JSSC.1976.1050714.

[17] L. W. Read, "An analysis of high frequency transistor mixers," *IEEE Trans. Broadcast. Telev. Receiv.*, vol. BTR-9, no. 1, pp. 72–78, May 1963, doi: 10.1109/TBTR1.1963.6312107.

[18] A. Bilotti and R. Pepper, "A monolithic limiter and balanced discriminator for FM and TV receivers," *IEEE Trans. Broadcast. Telev. Receiv.*, vol. 13, no. 3, pp. 60–65, Nov. 1967, doi: 10.1109/TBTR1.1967.4320098.

[19] A. Bilotti, "Applications of a monolithic analog multiplier," *IEEE J. Solid-State Circuits*, vol. 3, no. 4, pp. 373–380, Dec. 1968, doi: 10.1109/JSSC.1968.1049926.

[20] B. Gilbert, "A DG-500 MHz amplifier/multiplier principle," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, 1968, pp. 114–115, doi: 10.1109/ISSCC.1968.1154642.

[21] N. Sokal and A. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975, doi: 10.1109/JSSC.1975.1050582.

[22] K. Tsai and P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 962–970, Jul. 1999, doi: 10.1109/4.772411.

[23] K. Mertens, M. Steyaert, and B. Nauwelaers, "A 700MHz, 1W fully differential class E power amplifier in CMOS," in *Proc. 26th Eur. Solid-State Circuits Conf.*, 2000, pp. 65–68.

[24] D. Choi and S. Long, "A physically based analytic model of FET Class-E power amplifiers-designing for maximum PAE," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 9, pp. 1712–1720, Sep. 1999, doi: 10.1109/22.788613.

[25] Y. Tan, M. Kumar, and J. Lau, "A 900-MHz fully integrated SOI power amplifier for single-chip wireless transceiver applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1481–1486, Oct. 2000, doi: 10.1109/4.871326.

[26] A. Hadjichristos, J. Walukas, N. Klemmer, and G. Scott, "A highly integrated quad band low EVM polar modulation transmitter for GSM/EDGE applications," in *Proc. IEEE Custom Integr. Circuits Conf. (IEEE Cat. No.04CH37571)*, 2004, pp. 565–568, doi: 10.1109/CICC.2004.1358885.

- [27] R. Pullela, S. Tadjipour, D. Rozenblit, W. Domino, and A. Paff, "An integrated closed-loop polar transmitter with saturation prevention and low-IF receiver for quad-band GPRS/EDGE," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, 2009, pp. 112–113, 113a, doi: 10.1109/ISSCC.2009.4977333.
- [28] J. Chang, A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2- μm CMOS RF amplifier," *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 246–248, May 1993, doi: 10.1109/55.215182.
- [29] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer—a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002, doi: 10.1109/22.981284.
- [30] C. Wang, M. Vaidyanathan, and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1927–1937, Nov. 2004, doi: 10.1109/JSSC.2004.835834.
- [31] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011, doi: 10.1109/JSSC.2011.2163469.
- [32] A. Ben-Bassat, S. Gross, R. Banin, and O. Degani, "A fully integrated 27-dBm dual-band all-digital polar transmitter supporting 160 MHz for Wi-Fi 6 applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3414–3425, Dec. 2020, doi: 10.1109/JSSC.2020.3024973.
- [33] S. Y. S. Hung, J. Walling, and D. Allstot, "A 0.26 mm² DPD-less quadrature digital transmitter with -40dB EVM over >math>30\text{dB}</math> P_{out} range in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2020, pp. 184–185, doi: 10.1109/ISSCC19947.2020.9063070.
- [34] I. Vance, "An integrated circuit v.h.f. radio receiver," *Radio Electron. Eng.*, vol. 50, no. 4, pp. 160–166, Apr. 1980, doi: 10.1049/ree.1980.0024.
- [35] K. Weller and G. Robinson, "GaAs monolithic lumped element multistage microwave amplifier," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 1983, pp. 69–73, doi: 10.1109/MWSYM.1983.1130812.
- [36] I. Kipnis, J. Kukielka, and C. Snapp, "Silicon bipolar fixed and variable gain amplifier MMICs for microwave and lightwave applications up to 6 GHz," in *Proc. Microw. Millimeter-Wave Monolithic Circuits Symp., Dig. Papers*, 1989, pp. 101–104, doi: 10.1109/MCS.1989.37273.
- [37] B.-S. Song, "CMOS RF circuits for data communications applications," *IEEE J. Solid-State Circuits*, vol. 21, no. 2, pp. 310–317, Apr. 1986, doi: 10.1109/JSSC.1986.1052521.
- [38] K. Toh, R. G. Meyer, G. Chin, and A. Voshchenkov, "Wide-band, low-noise, matched-impedance amplifiers in submicrometer MOS technology," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1031–1040, Dec. 1987, doi: 10.1109/JSSC.1987.1052852.
- [39] R. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS," *IEEE J. Solid-State Circuits*, vol. 22, no. 4, pp. 512–521, Aug. 1987, doi: 10.1109/JSSC.1987.1052765.
- [40] S. Garverick and C. Sodini, "A wide-band NMOS balanced modulator/amplifier which uses 1-pm transistors for linearity," *IEEE J. Solid-State Circuits*, vol. 23, no. 1, pp. 195–198, Feb. 1988, doi: 10.1109/4.277.
- [41] J. Fenk, W. Birth, P. Shrig, and K. Schon, "An RF front-end for digital mobile radio," in *Proc. Bipolar Circuits Technol. Meeting*, 1990, pp. 244–247, doi: 10.1109/BIPOL.1990.171175.
- [42] P. Weger, W. Simburger, T. Leslie, and L. Treitinger, "Completely integrated 1.5 GHz direct conversion transceiver," in *Proc. IEEE Symp. VLSI Circuits*, 1994, pp. 135–136, doi: 10.1109/VLSIC.1994.586253.
- [43] P. Y. Chang, A. Rofougaran, K. Ahmed, and A. A. Abidi, "A highly linear 1-GHz CMOS downconversion mixer," in *Proc. 19th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 1993, pp. 210–213.
- [44] A. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1939–1944, Dec. 1996, doi: 10.1109/4.545816.
- [45] E. Heaney, P. O. Sullivan, and C. Kerrmarrec, "Ultra low power low noise amplifiers for wireless communications," in *Proc. 15th Annu. GaAs IC Symp.*, 1993, pp. 49–51, doi: 10.1109/GAAS.1993.394502.
- [46] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers*, 1996, pp. 32–33, doi: 10.1109/VLSIC.1996.507705.
- [47] J. Craninckx and M. Steyaert, "A 1.8-GHz low-phase-noise spiral-LC CMOS VCO," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers*, 1996, pp. 30–31, doi: 10.1109/VLSIC.1996.507704.
- [48] T. Soorapanth, D. Shaeffer, T. H. Lee, and S. Wong, "Analysis and optimization of accumulation-mode varactor for RF ICs," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers (Cat. No.98CH36215)*, 1998, pp. 32–33, doi: 10.1109/VLSIC.1998.687993.
- [49] D. Su and W. McFarland, "A 2.5-V, 1-W monolithic CMOS RF power amplifier," in *Proc. Custom Integr. Circuits Conf. (CICC)*, 1997, pp. 189–192, doi: 10.1109/CICC.1997.606611.
- [50] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1483–1492, Dec. 1995, doi: 10.1109/4.482196.
- [51] A. Rofougaran, G. Chang, M. Rofougaran, A. A. Abidi, and H. Samuelli, "A 900 MHz CMOS frequency-hopped spread-spectrum RF transmitter IC," in *Proc. Custom Integr. Circuits Conf.*, 1996, pp. 209–212, doi: 10.1109/CICC.1996.510545.
- [52] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2054–2065, Dec. 1998, doi: 10.1109/4.735547.
- [53] T. Riley, M. Copeland, and T. Kwaniowski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993, doi: 10.1109/4.229400.
- [54] M. Perrott, T. Tewksbury, and C. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2048–2060, Dec. 1997, doi: 10.1109/4.643663.
- [55] B. Park and P. Allen, "A 1 GHz, low-phase-noise CMOS frequency synthesizer with integrated LC VCO for wireless communications," in *Proc. IEEE Custom Integr. Circuits Conf. (Cat. No.98CH36143)*, 1998, pp. 567–570, doi: 10.1109/CICC.1998.695042.
- [56] W. Rhee, B. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1453–1460, Oct. 2000, doi: 10.1109/4.871322.
- [57] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec. 1995, doi: 10.1109/4.482187.
- [58] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Trans. Circuits Syst. II. Analog Digit. Signal Process.*, vol. 44, no. 6, pp. 428–435, June 1997, doi: 10.1109/82.592569.
- [59] J. Rudell, J. Ou, T. Cho, J. Weldon, and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2071–2088, Dec. 1997, doi: 10.1109/4.643665.
- [60] A. Shahani, D. Shaeffer, and T. H. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997, doi: 10.1109/4.643664.
- [61] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998, doi: 10.1109/4.735702.
- [62] B. Razavi, "A 900-MHz CMOS direct conversion receiver," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1997, pp. 113–114.
- [63] T. Cho, E. Dukatz, L. Plouvier, and S. Rabii, "A single-chip CMOS direct-conversion transceiver for 900 MHz spread-spectrum digital cordless phones," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers (Cat. No.99CH36278)*, 1999, pp. 228–229, doi: 10.1109/ISSCC.1999.759205.
- [64] A. Rofougaran et al., "A single-chip 900-MHz spread-spectrum wireless transceiver in 1- μm CMOS. II. Receiver design," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 535–367, Apr. 1998, doi: 10.1109/4.663558.
- [65] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1382–1385, Oct. 1999, doi: 10.1109/4.792608.
- [66] K. Kundert, private communication, Apr. 2023.
- [67] R. Telichevesky, K. Kundert, and J. White, "Efficient steady-state analysis based on matrix-free Krylov-subspace methods," in *Proc. 32nd Annu. ACM/IEEE Des. Automat. Conf.*, Jun. 1995, pp. 480–484, doi: 10.1145/217474.217574.
- [68] S. Zhou and M. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005, doi: 10.1109/JSSC.2005.845981.
- [69] R. Svitek and S. Raman, "DC offsets in direct-conversion receivers: Characterization and implications," *IEEE Microw. Mag.*, vol. 6, no. 3, pp. 76–81, Sep. 2005, doi: 10.1109/MMW.2005.1511916.
- [70] M. Chen and M. F. Chang, "Active 2nd-order intermodulation calibration for direct-conversion receivers," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, 2006, pp. 1830–1839, doi: 10.1109/ISSCC.2006.1696240.
- [71] J. Park, C. Lee, B. Kim, and J. Laskar, "Design and analysis of low flicker-noise CMOS mixers for direct-conversion receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 12, pp. 4372–4380, Dec. 2006, doi: 10.1109/TMTT.2006.885582.
- [72] W. Redman-White and D. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *Proc. 27th Eur. Solid-State Circuits Conf.*, 2001, pp. 41–44.
- [73] E. Sacchi, I. Bietti, L. Tee, and R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2003, pp. 459–462, doi: 10.1109/CICC.2003.1249440.

- [74] K. Lee et al., "Full-CMOS 2-GHz WCDMA direct conversion transmitter and receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 43–53, Jan. 2003, doi: 10.1109/JSSC.2002.806280.
- [75] J. Rogin, G. Brenna, D. Tschopp, and Q. Huang, "A 1.5-V 45-mW direct-conversion WCDMA receiver IC in 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2239–2248, Dec. 2003, doi: 10.1109/JSSC.2003.819087.
- [76] G. Brenna, D. Tschopp, J. Rogin, and Q. Huang, "A 2-GHz carrier leakage calibrated direct-conversion WCDMA transmitter in 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1253–1262, Aug. 2004, doi: 10.1109/JSSC.2004.831794.
- [77] W. Kim, S. Yang, and B. Park, "A direct conversion receiver with an IP2 calibrator for CDMA/PCS/GPS/AMPS applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1535–1541, Jul. 2006, doi: 10.1109/JSSC.2006.873926.
- [78] P. Zhang, L. Der, D. Guo, L. Huynh, T. Nguyen, and B. Razavi, "A CMOS direct-conversion transceiver for IEEE 802.11 a/b/g WLANs," in *Proc. IEEE Custom Integr. Circuits Conf. (IEEE Cat. No.04CH37571)*, May 2004, pp. 409–412, doi: 10.1109/CICC.2004.1358835.
- [79] D. Su, M. Zargari, S. Rabii, K. Singh, and B. Wooley, "A 5 GHz CMOS transceiver for IEEE 802.11a wireless LAN," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers (Cat. No.02CH37315)*, 2002, pp. 92–449, doi: 10.1109/ISSCC.2002.992954.
- [80] P. Zhang et al., "A 5-GHz direct-conversion CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2232–2238, Dec. 2003, doi: 10.1109/JSSC.2003.819088.
- [81] T. Nguyen, J. Lee, S. Han, and C. Pyo, "A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18- μ m CMOS technology," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 4062–4071, Dec. 2006, doi: 10.1109/TMTT.2006.885556.
- [82] A. Behzad, Z. Shi, S. Butala, L. Lin, K. Carter, and A. Rofougaran, "A 5-GHz direct-conversion CMOS transceiver utilizing automatic frequency control for the IEEE 802.11a wireless LAN standard," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2209–2220, Dec. 2003, doi: 10.1109/JSSC.2003.819085.
- [83] A. Behzad et al., "A fully integrated MIMO multiband direct conversion CMOS transceiver for WLAN applications (802.11n)," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2795–2808, Dec. 2007, doi: 10.1109/JSSC.2007.908667.
- [84] R. Rogenmoser, Q. Huang, and F. Plazza, "1.57 GHz asynchronous and 1.4 GHz dual-modulus 1.2 μ m CMOS prescalers," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 1994, pp. 387–390, doi: 10.1109/CICC.1994.379697.
- [85] J. Craninckx and M. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 890–897, Jul. 1996, doi: 10.1109/4.508200.
- [86] T. Stetzler, I. Post, J. Havens, and M. Koyama, "A 2.7–4.5 V single chip GSM transceiver RF integrated circuit," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1421–1429, Dec. 1995, doi: 10.1109/4.482189.
- [87] C. Marshall, F. Behbahani, S. Navid, S. Lee, and E. Saur, "A 2.7 V GSM transceiver ICs with on-chip filtering," in *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, 1995, pp. 148–149, doi: 10.1109/ISSCC.1995.535469.
- [88] D. G. Tucker, "The history of the homodyne and synchrodyne," *J. Brit. Inst. Radio Eng.*, vol. 14, no. 4, pp. 143–154, Apr. 1954, doi: 10.1049/jbire.1954.0021.
- [89] Y. Zheng, Y. Tang, J. Yang, and F. Lin, "A low power noncoherent CMOS UWB transceiver ICs," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp. – Dig. Papers*, 2005, pp. 347–350, doi: 10.1109/RFIC.2005.1489805.
- [90] B. Razavi, T. Aytur, C. Lam, R. Yan, and C. C. Lee, "A UWB CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555–2562, Dec. 2005, doi: 10.1109/JSSC.2005.857430.
- [91] A. Bevilacqua and A. M. Niknejad, "An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) (IEEE Cat. No.04CH37519)*, 2004, pp. 382–533, doi: 10.1109/ISSCC.2004.1332754.
- [92] A. Ismail and A. Abidi, "A 3.1 to 8.2 GHz direct conversion receiver for MB-OFDM UWB communications," in *Proc. IEEE Int. Dig. Tech. Papers, Solid-State Circuits Conf. (ISSCC)*, 2005, pp. 208–593, doi: 10.1109/ISSCC.2005.1493942.
- [93] J. Bergervoet, K. Harish, S. Lee, and R. Roovers, "A WiMedia-compliant UWB transceiver the opamp has a unity-gain bandwidth close to 4GHz and draws in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, Feb. 2007, pp. 112–113.
- [94] C. Doan, S. Emami, A. Niknejad, and R. W. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Commun. Mag.*, vol. 42, no. 12, pp. 132–140, Dec. 2004, doi: 10.1109/MCOM.2004.1367565.
- [95] B. Razavi, "A 60GHz direct-conversion CMOS receiver," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Dig. Tech. Papers*, Feb. 2005, pp. 400–606, doi: 10.1109/ISSCC.2005.1494038.
- [96] C. Marcu, D. Chowdhury, C. Thakkar, M. Tabesh, and A. Niknejad, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009, doi: 10.1109/JSSC.2009.2032584.
- [97] A. Tomkins, R. Aroca, S. Nicholson, and S. P. Voinescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, Aug. 2009, doi: 10.1109/JSSC.2009.2022918.
- [98] K. Okada, N. Li, K. Matsushita, A. Musa, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011, doi: 10.1109/JSSC.2011.2166184.
- [99] R. Wu et al., "64-QAM 60-GHz CMOS transceivers for IEEE 802.11ad/ay," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2871–2891, Nov. 2017, doi: 10.1109/JSSC.2017.2740264.
- [100] H. Park, D. Kang, J. Lee, H. Lee, S. Son, and S. Yang, "Millimeter-wave band CMOS RF phased-array transceiver IC designs for 5G applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2020, pp. 17.2.1–17.2.4, doi: 10.1109/IEDM13553.2020.9371948.
- [101] P. Sagazio, S. Callender, S. Pellerano, and C. Hull, "Architecture and circuit choices for 5G millimeter-wave beamforming transceivers," *IEEE Commun. Mag.*, vol. 56, no. 12, pp. 186–192, Dec. 2018, doi: 10.1109/MCOM.2018.1701374.
- [102] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2 x 2 beamformer flip-chip unit cell," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, May 2018, doi: 10.1109/JSSC.2018.2791481.
- [103] J. Pang et al., "A 28-GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2371–2386, Sep. 2020, doi: 10.1109/JSSC.2020.2995039.
- [104] H. Kim, B. Park, S. Song, T. Moon, and Y. Ho, "A 28-GHz CMOS direct conversion transceiver with packaged 2 x 4 antenna array for 5G cellular system," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018, doi: 10.1109/JSSC.2018.2817606.
- [105] K. Lim, S. Lee, Y. Lee, B. Moon, J. Lee, and S. Han, "A 65-nm CMOS 2 x 2 MIMO multi-band LTE RF transceiver for small cell base stations," *IEEE J. Solid-State Circuits*, vol. 53, pp. 1960–1976, Jul. 2018, doi: 10.1109/JSSC.2018.2824300.
- [106] E. Lu, W. Li, Z. Deng, E. Rostami, J. Zhan, and O. Shanaa, "A 4 x 4 dual-band dual-concurrent WiFi 802.11ax transceiver with integrated LNA, PA and T/R switch achieving +20dBm 1024-QAM MCS11 pout and -43dB EVM floor in 55nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2020, pp. 178–180, doi: 10.1109/ISSCC19947.2020.9063127.

About the Author

Behzad Razavi (razavi@ee.ucla.edu) is a professor with the University of California at Los Angeles, Los Angeles, CA 90095 USA. He was with Princeton University from 1992 to 1994, and with Stanford University in 1995. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. He is a member of the U.S. National Academy of Engineering and a fellow of the U.S. National Academy of Inventors. He has served on the Technical Program Committees of the ISSCC from 1993 to 2002 and the VLSI Circuits Symposium from 1998 to 2002. He has also served as a guest editor and an associate editor for the *IEEE Journal of Solid-State Circuits*, *IEEE Transactions on Circuits and Systems*, and *International Journal of High-Speed Electronics and Systems*. He has served as the founding editor-in-chief of the *IEEE Solid-State Circuits Letters*. He has served as an IEEE Distinguished Lecturer and is an IEEE Fellow. 