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Fifty Applications of the CMOS Inverter—Part 1

The CMOS inverter dates back to a patent filed by Wanlass in 1963 [1]. Shown in Figure 1 is the disclosed structure. (Unlike today's convention, Wanlass denotes the drains by arrows.) With the scaling of the supply voltage in nanometer technologies, the CMOS inverter has found much wider application, and many of its properties have come into focus. In this multipart article, we study 50 examples of circuits using inverters in critical roles. Moreover, we use simulations to quantify the performance of these topologies. Simulations are performed in the slow–slow corner of 28-nm technology at $T = 75^\circ$ C, with $V_{DD} = 0.95$ V. An estimate of the layout parasitic capacitances is also included. Unless otherwise stated, $L = 30$ nm for all transistors.

It is important to recognize the poor supply rejection of inverters. That is, the small-signal voltage gain from their supply to their output is comparable to that from their input to their output. For this reason, many of the circuits studied in this article require operation from low-noise voltage regulators.

The Tapered Buffer

Among the oldest applications of the inverter, the tapered buffer consists of a cascade of scaled stages optimized for minimal delay for driving a given capacitance, C_L [Figure 2(a)]. It can be shown that a scaling factor of $e \approx 2.718$ minimizes the delay if the drain capacitances of the transistors are neglected. Under this condition, the stages contribute equal delays. The number of stages is given by $n = \ln(C_L/C_{in})$, where C_{in} denotes the input capacitance of the first stage. If drain capacitances are included, the scaling factor is greater, e.g., around three to four.

In addition to the delay, the power consumption of the cascade is also of interest. The total capacitance for the tapered stages is equal to

$$C_{tot} = C_{in} + eC_{in} + e^2 C_{in} + \cdots + e^n C_{in} \quad (1)$$

$$= \frac{e^{n+1} - 1}{e - 1} C_{in} \quad (2)$$

$$= \frac{eC_L - C_{in}}{e - 1}. \quad (3)$$

The total power is thus given by

$$P = f_{in} \frac{eC_L - C_{in}}{e - 1} V_{DD}^2 \quad (4)$$

where f_{in} is the input frequency.

In wireless and wireline transceivers, the tapered buffer is used to drive long interconnects carrying local oscillator (LO) waveforms or clocks. In such environments, the delay may be less problematic, but the jitter introduced by the chain proves critical. To minimize jitter, we wish to sharpen the voltage transitions at the output of each stage.

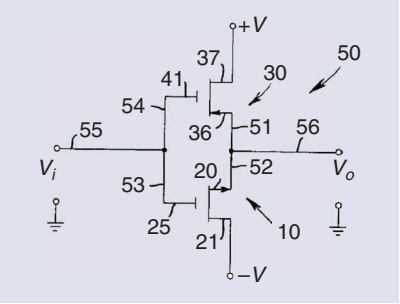

FIGURE 1: The CMOS inverter patented by Wanlass.

As an example, we design a buffer for driving $C_L = 50$ fF at $f_{in} = 10$ GHz. Depicted in Figure 2(b), the circuit employs an input inverter with $W_N = 0.5\,\mu$m and $W_P = 1\,\mu$m, exhibiting an input capacitance of about 3 fF. We thus have $n = \ln(C_L/C_{in}) \approx 3$. Scaling the next two stages by factors of three and nine, respectively, yields a delay of 22 ps. Simulations indicate $P_{tot} = 740\,\mu$W, slightly greater than the 700 μW predicted by (4) and arising from the inverters' crowbar current.

We compute the buffer's jitter by running a transient noise simulation for 100 ns, wherein a noise frequency range of 10 MHz to 300 GHz is specified. Provided in Figure 2(b), the eye diagram transitions reveal a peak-to-peak jitter of 100 fs, which translates to an RMS value of about 17 fs if we assume the peak-to-peak value of the Gaussian noise is roughly six times its standard deviation.

The T-Gate Static Latch

For digital or mixed-signal designs that must accommodate arbitrarily low clock or refresh rates, we incorporate static latches. For example, a system that performs foreground calibration must retain the settings indefinitely after power-up. The latch presented in Figure 3(a) is such

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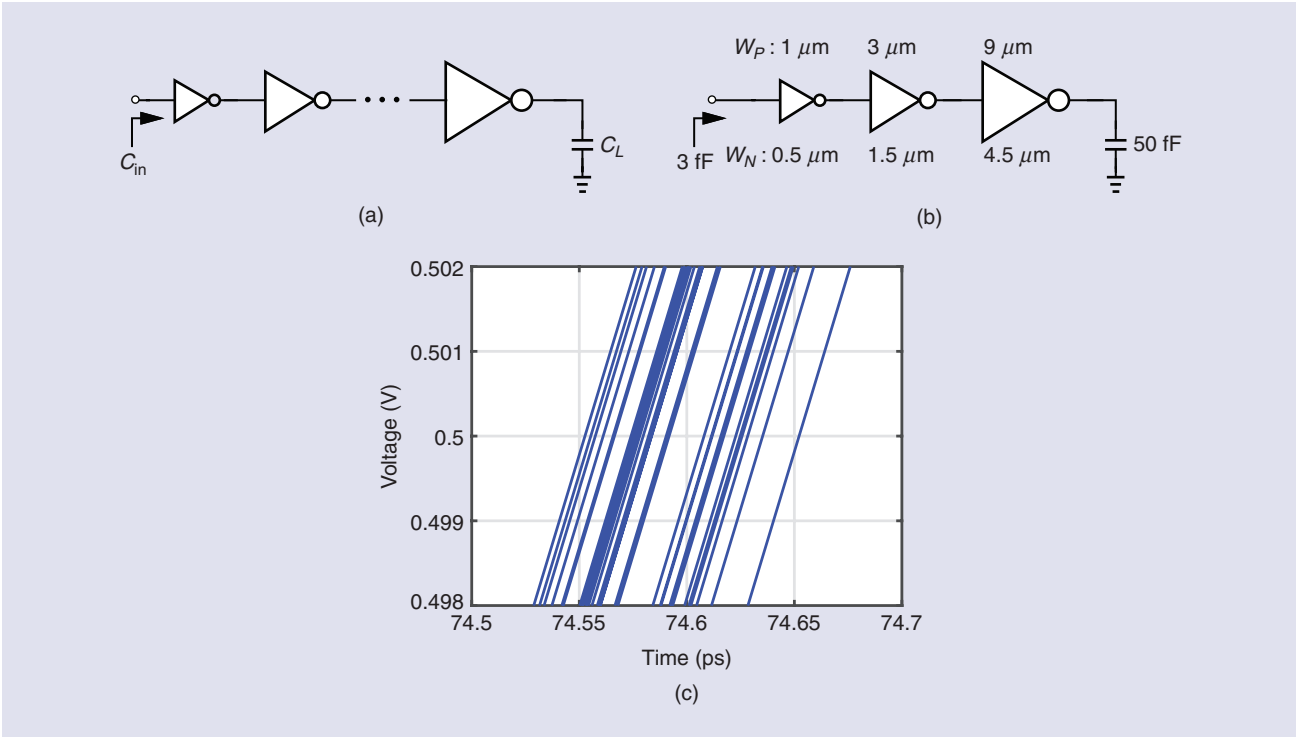

FIGURE 2: (a) The tapered buffer, (b) an example, and (c) its output jitter.

a candidate. In the sense mode, D_{in} travels through S_1, S_2, and Inv_1, and in the store mode, it is held by Inv_1, Inv_2, S_3, and S_4.

A quick method of evaluating the speed limitations of latches is to incorporate them in frequency dividers, specifically in ÷2 circuits. Shown in Figure 3(b) is such a structure, where Inv_a provides a net inversion around the loop and Inv_b acts as a buffer. With rail-to-rail voltage swings for CK and $\overline{CK}$, we plot the output frequency versus the input frequency in Figure 3(c), observing failure beyond f_{in} = 30 GHz. Since the loop can sustain a periodic waveform at 15 GHz, we expect the static latch to handle data rates up to about 15 Gb/s. The divider draws 300 μW at 30 GHz.

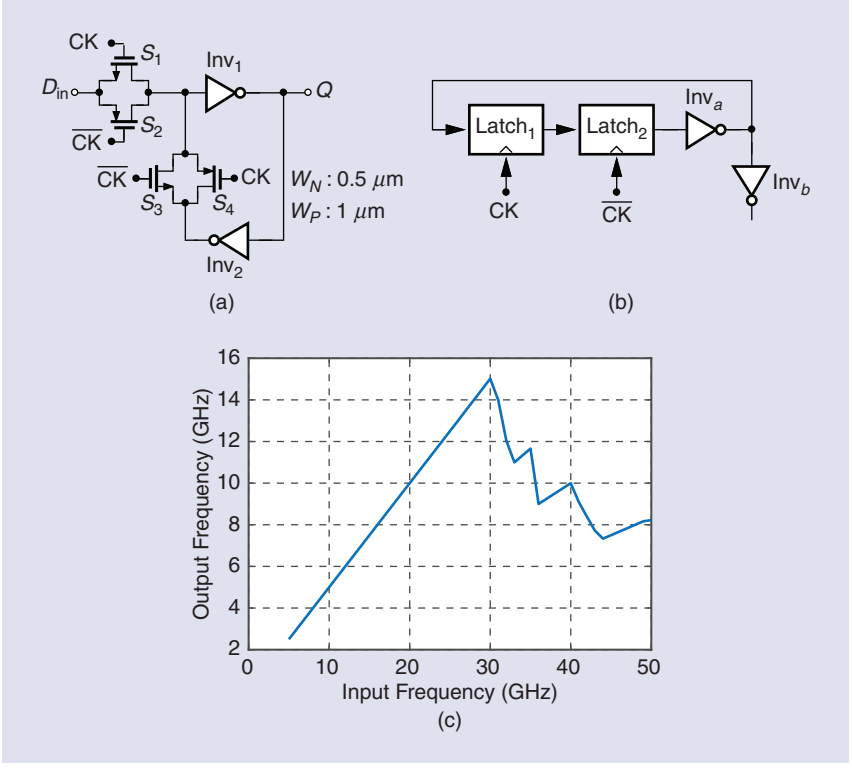

FIGURE 3: (a) A static latch, (b) a ÷2 circuit using this latch, and (c) an I/O frequency plot of the divider.

The Tristate Static Latch

Another static latch topology employs tristate inverters rather than T gates [2]. Depicted in Figure 4(a), the circuit reduces to two cascaded inverters in the sense mode and two cross-coupled inverters in the store mode. The reader may recognize the input and feedback stages as "clocked CMOS" (C^2MOS) logic, but they do not act as latches here. As in Figure 3(b), we construct a ÷2 circuit using this type of latch and evaluate its performance. Plotted in Figure 4(b), the I/O frequency behavior suggests a maximum speed of 27 GHz. Thus, this topology is slower than that in

Figure 3(a). The ÷2 stage draws 300 μA at this frequency.

The Set–Reset Latch

Set–reset (SR) latches can be used to hold data asynchronously. Depicted in Figure 5(a), the structure consists of two cross-coupled inverters controlled by input devices M_1 and M_2. If, for example, $\bar{Q} = 1$ and only S goes high, then $\bar{Q}$ falls, and Q reaches a logical one. Since M_1 and M_2 must overcome the PMOS transistors within Inv_1 and Inv_2, the circuit exemplifies "ratioed" logic. The inverters' NMOS transistors play a minor role in the SR operation, but they prove necessary for retaining the state if the latch must hold the data for a long time.

To assess the speed of the circuit, we place two instances of it in a loop so as to form a quadrature ring oscillator, as in Figure 5(b). We have $W_P = 2W_N = 1\,\mu$m for the inverters, and $W_{1,2} = 1\,\mu$m. Plotted in Figure 5(c), the output waveforms reveal a frequency of 18 GHz and, hence, a delay of about $1/(4 \times 18\,\text{GHz}) = 14$ ps per latch.

The Dynamic Latch

A simple dynamic latch can be realized by means of a T-gate and an inverter [Figure 6(a)]. In the sense mode, the circuit allows V_X to track D_{in}, and in the store mode, it holds the data on the total capacitance at this node. Note that the charge injection and clock feedthrough of T-gate devices may degrade the high and low values at X. The inverter restores the logical levels and prevents charge sharing with the next stage.

We construct the arrangement of Figure 3(b) for this latch as well. With $W_2 = 2W_1 = 1\,\mu$m and the same widths for the inverter devices, we arrive at the I/O frequency plot in Figure 6(b). The circuit operates up to 44 GHz and consumes 250 μA at this frequency, proving superior to the static counterparts studied above.

The Static Memory Cell

The cross-coupled inverters encountered in the SR latch can also hold a state in a static memory environment. For this purpose, the cell must be able to sense a state (in a "write" operation) and deliver a state (in a "read" operation). Illustrated in Figure 7(a), the circuit employs "access" devices M_1 and M_2 for both operations. Differential outputs improve the read speed.

Owing to the large bit line capacitance, C_B, a read operation may destroy the cell's state. Consider the situation in Figure 7(b), where Bit = 1 but the cell holds a zero at A. When M_1 turns on, it acts as a source follower, raising V_A. If V_A reaches the switching threshold of Inv_1, this inverter, and, hence, the entire cell, may change its state. Thus, M_a must be strong enough to avoid this effect.

Plotted in Figure 7(c), the cell's waveforms after the word line rises reveal that V_A reaches 0.2 V, still retaining the state. With $C_B = 40$ fF, Bit

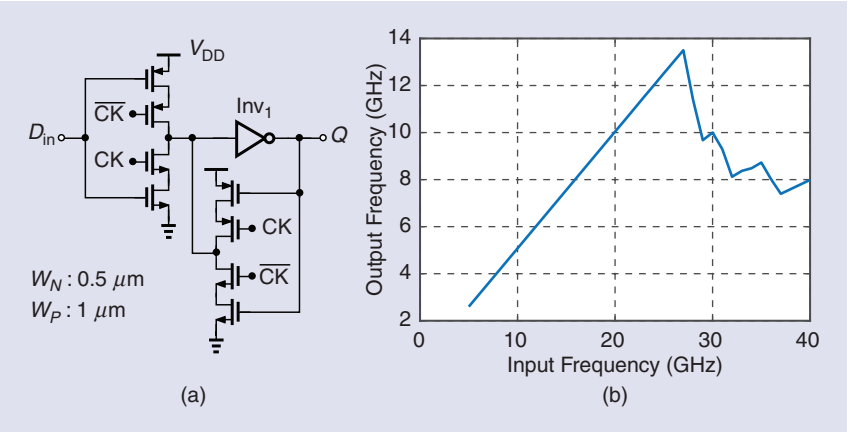

FIGURE 4: (a) A static latch using tristate inverters and (b) the I/O frequency plot of a divider using this latch.

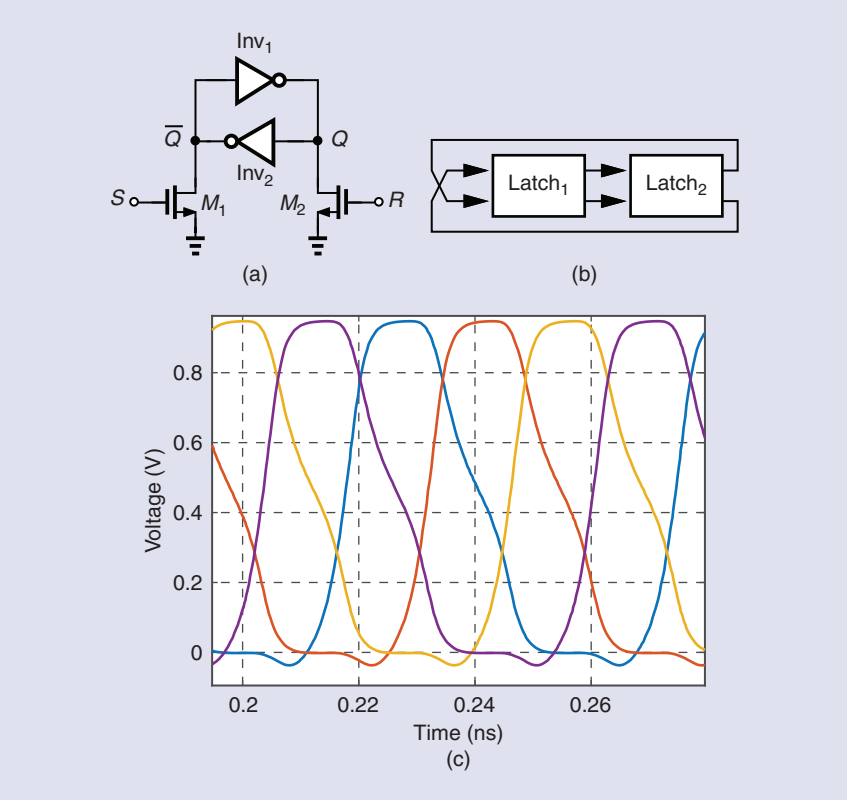

FIGURE 5: (a) An SR latch, (b) a ring oscillator using such a latch, and (c) oscillator output waveforms.

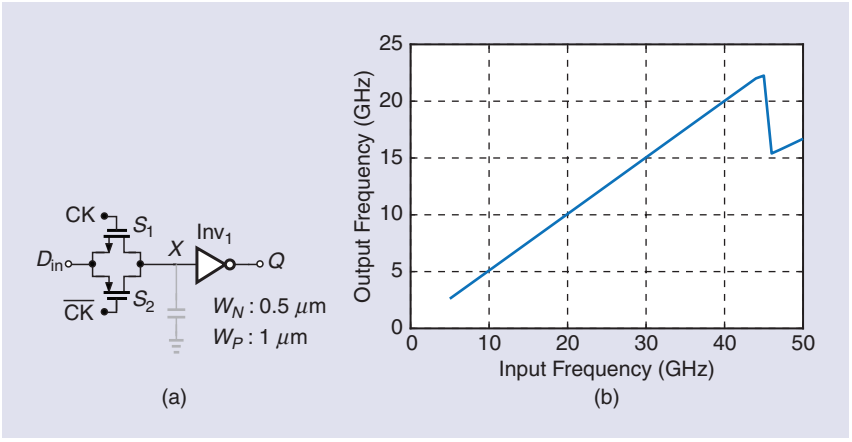

FIGURE 6: (a) A dynamic latch and (b) the I/O frequency plot of a divider using this latch.

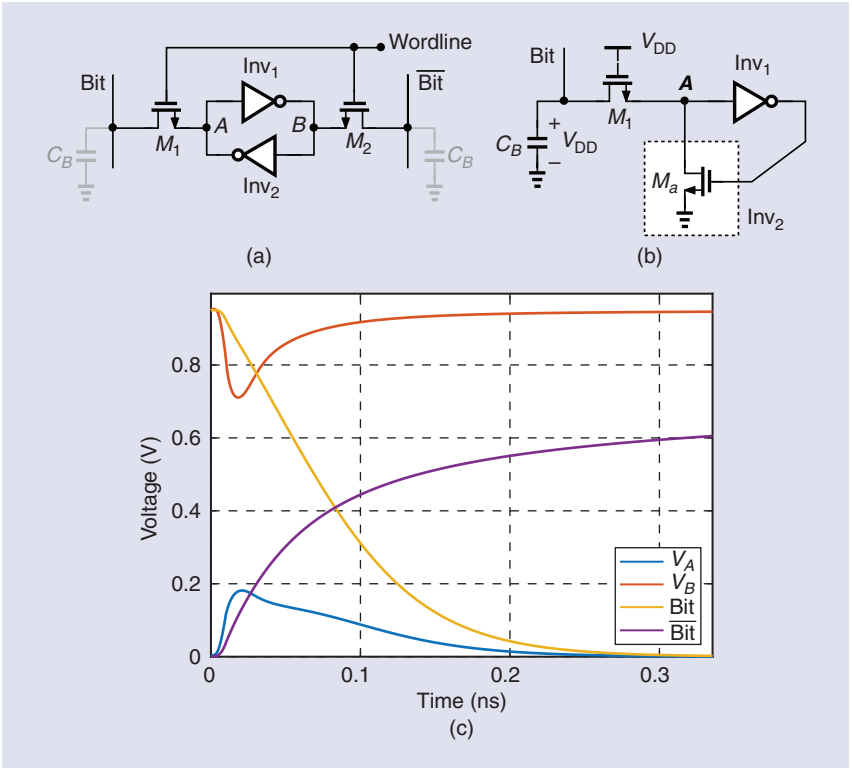

FIGURE 7: (a) A static memory cell, (b) the circuit in the read mode, and (c) the circuit's waveforms.

and $\overline{\text{Bit}}$ evolve rather slowly, an issue alleviated through the use of a differential sense amplifier (not shown).

The Low-Noise Amplifier

The LNAs used in RF receivers must present an input resistance of 50 Ω, a low noise figure (NF), and a reasonable gain. The CMOS inverter is one such candidate.

Beginning with the diode-connected transistor in Figure 8(a) and neglecting channel length modulation, we recognize that the device exhibits a small-signal resistance equal to $1/g_{m1}$. The topology in Figure 8(b) provides the same R_{in} because R_F appears in series with an ideal current source in the small-signal model. However, current source I_1 contributes noise without carrying the input signal. We thus convert I_1 to an "active" load, as illustrated in Figure 8(c), expecting an input resistance of

$$R_{in} = \frac{1}{g_{m1} + g_{m2}} \tag{5}$$

which can be set to 50 Ω. It can be proved that proper input matching places a lower bound of 3 dB on the NF.

Equation (5) appears to imply that R_F does not experience the Miller effect. However, computing the voltage gain from X to Y, we have $A_v = 1 - (g_{m1} + g_{m2})R_F$, and hence, $R_{in} = R_F/(1 - A_v) = 1/(g_{m1} + g_{m2})$.

In practice, the finite output resistance of M_1 and M_2 alters our results considerably. One can show that R_{in} in Figure 8(c) is now expressed as

$$R_{in} = \frac{R_F + r_{O1} \| r_{O2}}{1 + (g_{m1} + g_{m2})(r_{O1} \| r_{O2})}. \tag{6}$$

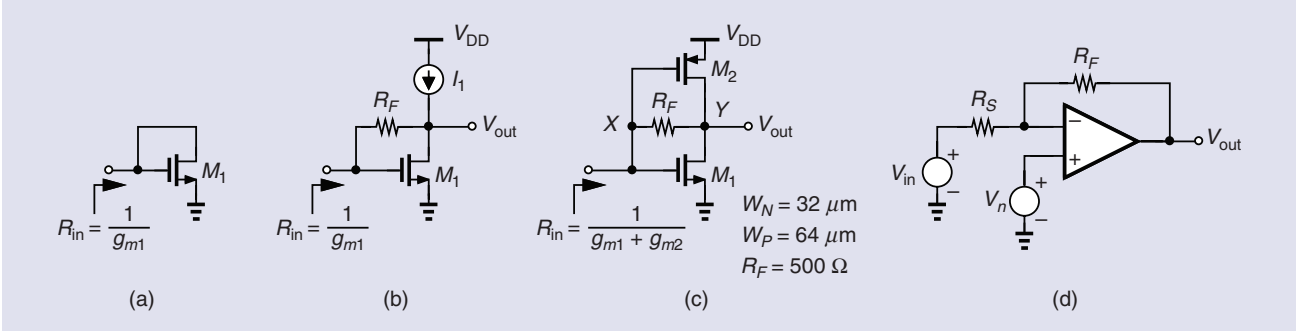

FIGURE 8: The (a) impedance of a diode-connected device, (b) input impedance of the device with a feedback resistor, (c) basic LNA, and (d) simple model for noise calculation.

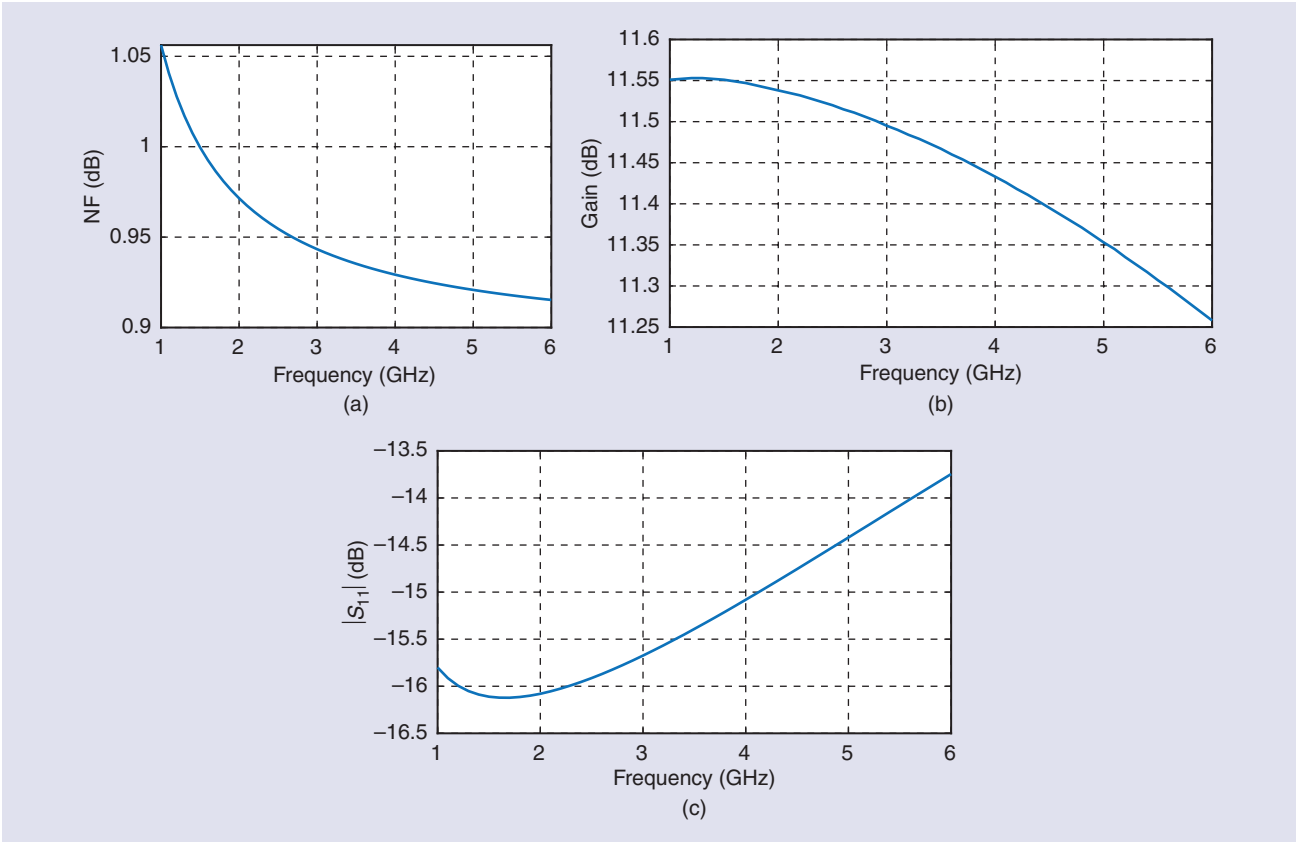

FIGURE 9: The LNA's (a) NF, (b) gain, and (c) return loss.

As an example, with $W_1 = 32\,\mu$m, $W_2 = 64\,\mu$m, and a bias current of 5.5 mA, we have $g_{m1} + g_{m2} \approx 44$ mS and $r_{O1} \| r_{O2} = 90\,\Omega$. It follows that $R_{in} = (R_F + 90\,\Omega)/9 = R_F/9 + 9\,\Omega$. We observe that for $R_{in} = 50\,\Omega$, R_F must not exceed $370\,\Omega$. Interestingly, the low output resistance of the transistors makes R_F a greater contributor to R_{in} than $1/(g_{m1} + g_{m2})$.

The dependence of R_{in} upon R_F also rewrites the NF equation. Drawing the circuit as in Figure 8(d), where V_n denotes the inverter's input-referred noise, we have

$$V_{out} = -\frac{R_F}{R_S} V_{in} + \left(1 + \frac{R_F}{R_S}\right) V_n. \quad (7)$$

It follows that

$$NF = 1 + \frac{\left(1 + \frac{R_F}{R_S}\right)^2 \overline{V_n^2}}{4kTR_S\left(\frac{R_F^2}{R_S^2}\right)}. \quad (8)$$

We now assume $R_F \gg r_{O1} \| r_{O2}$ and $(g_{m1} + g_{m2})(r_{O1} \| r_{O2}) \gg 1$ in (6) and write $R_{in} \approx R_F/[(g_{m1} + g_{m2})(r_{O1} \| r_{O2})] = R_S$. We also assume $R_F \gg R_S$ in (8), arriving at

$$NF \approx \gamma \frac{r_{O1} \| r_{O2}}{R_F} + 1. \quad (9)$$

The NF no longer faces a lower bound of 3 dB. In our numerical example, $(r_{O1} \| r_{O2})/R_F \approx 0.24$, and NF ≈ 1.9 dB. These calculations have neglected the noise of R_F.

We simulate the LNA with the numerical values mentioned above but with $R_F = 500\,\Omega$ so as to reduce both its noise contribution and the first term in (9), even though it leads to $R_{in} \approx 66\,\Omega$. Figure 9(a) plots the NF for a frequency range of 1–6 GHz, displaying a peak value of 1.05 dB (due to flicker noise). The power consumption is 5.2 mW. We note from Figure 9(b) that the gain from V_{in} to V_{out} in Figure 8(d) is about 11 dB. Figure 9(c) reveals an acceptable range for the input return loss, $|S_{11}|$.

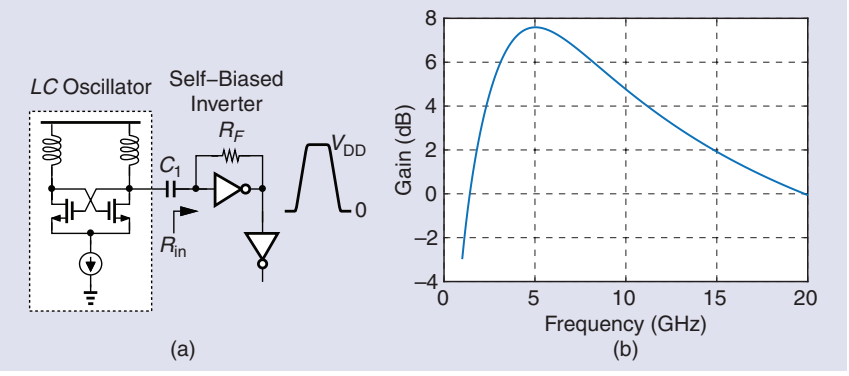

FIGURE 10: (a) A self-biased inverter following an oscillator and (b) the circuit's gain.

The Self-Biased Inverter

The topology of Figure 8(c) can be modified so as to serve other purposes as well. Displayed in Figure 10(a), the "self-biased inverter" acts as an amplifier and proves particularly useful if rail-to-rail voltage swings are sought. For example, an *LC* oscillator delivering moderate swings with a common-mode level near V_{DD} can be followed by this stage, thus providing a rail-to-rail output.

The value of C_1 in Figure 10(a) is governed by two considerations. First, it must be about 10 times the input capacitance of the inverter to minimize attenuation. Second, it must be sufficiently large so that the high-pass corner frequency, $1/(2\pi C_1 R_{in})$, falls well below the lowest frequency traveling through the circuit.

We scale the LNA of Figure 8(c) down by a factor of 32, arriving at $W_N = 1\,\mu$m, $W_P = 2\,\mu$m, $I_D = 170\,\mu$A, and $r_{O1} \| r_{O2} = 2.9\,\text{k}\Omega$. Figure 10(b) plots the small-signal gain of such a design with $C_1 = 30\,$fF, revealing a high-pass corner around 2.5 GHz and a peak gain of 7.5 dB at 6 GHz. Beyond 20 GHz, the circuit begins to lose its efficacy for a fanout of one.

The input resistance merits a great deal of deliberation. Equation (6) yields $R_{in} = (R_F + 2.9\,\text{k}\Omega)/9$; e.g., $R_{in} = 1\,\text{k}\Omega$ if $R_F = 6.1\,\text{k}\Omega$. Unfortunately, an input resistance of $1\,\text{k}\Omega$ can significantly lower the tank Q in Figure 10(a). Fortunately, R_{in} is much higher if the VCO output swing is large enough to cause large-signal operation in the inverter. Nonetheless, the phase noise of the VCO must be closely examined before and after the self-biased inverter is attached.

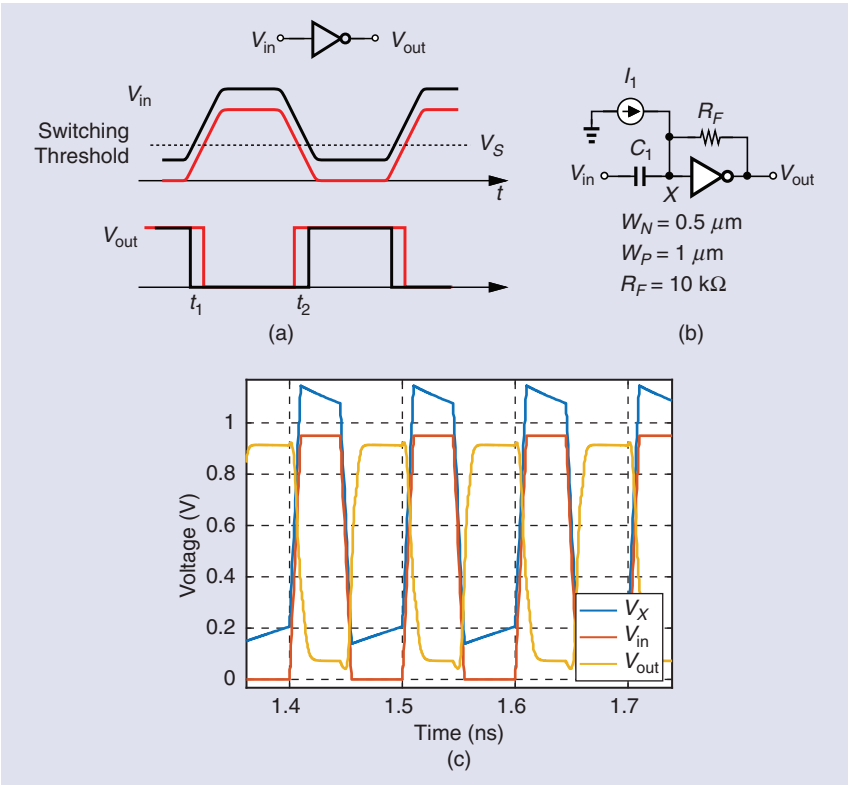

FIGURE 11: (a) The effect of a dc offset on the inverter output duty cycle, (b) the duty cycle correction circuit, and (c) the input and output waveforms.

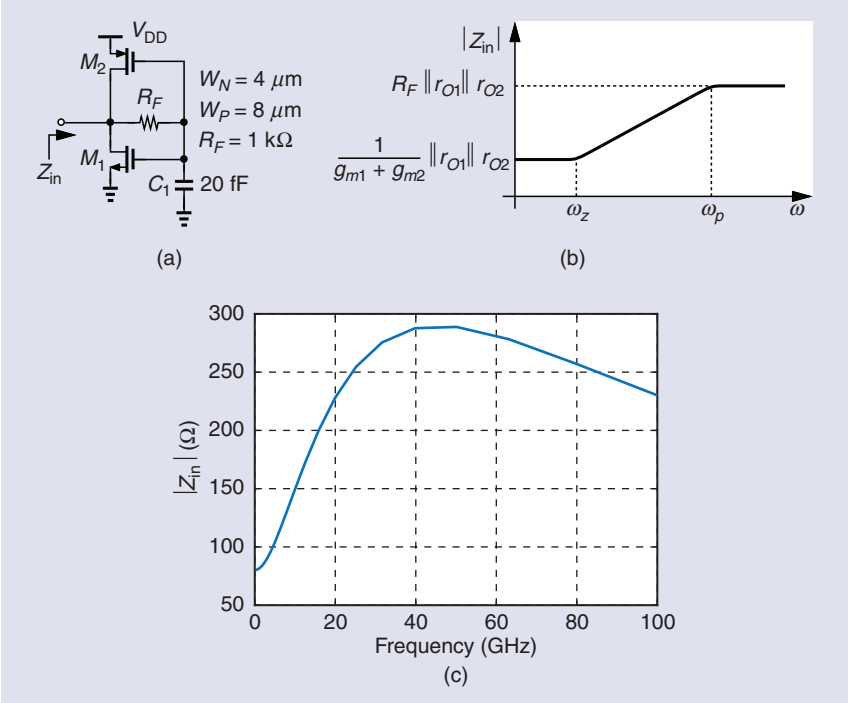

FIGURE 12: (a) An active inductor using an inverter, (b) its impedance behavior, and (c) its simulated impedance.

The Duty Cycle Correction Circuit

High-speed systems face tight timing constraints, often demanding a precise 50% duty cycle for their clocks. Moreover, if a clock or LO waveform is applied to a $\div 2$ circuit to generate quadrature phases, the output phase accuracy dictates a 50% duty cycle for the input. To arrive at a duty cycle correction circuit, we begin with the input waveforms in Figure 11(a), assuming, for simplicity, that V_{out} jumps as V_{in} crosses the switching threshold of the inverter, V_S. We observe that a vertical shift in V_{in} alters the times at which

V_{in} crosses V_S, a property afforded by the finite rise and fall times of V_{in}. As a result, the inverter output duty cycle changes. Specifically, for an input offset of $+\Delta V, t_2 - t_1$ increases by $2\Delta V/S$, where S denotes the input slew rate.

The self-biased inverter provides a simple environment for this correction method. As demonstrated in Figure 11(b) [3], we inject current I_1 into the input node, creating a departure equal to $I_1 R_{in}$ from the inverter's switching threshold, where R_{in} is given by (6). The output low level thus lasts longer by $2I_1 R_{in}/S$.

The topology of Figure 11(b) faces two issues. First, it offers a narrow correction range if V_{in} exhibits fast transitions. As seen in the simulation results presented in Figure 11(c) for an input frequency of 10 GHz and rise and fall times of 10 ps, we can improve a duty cycle of 45% to 48% with $I_1 = 10\,\mu$A and $R_F = 10\,$kΩ. This is expected, as $S = 0.95$ V/10 ps, $I_1 R_{in} = 180$ mV, and, hence, the correction amounts to only 3.8 ps. One can cascade multiple stages to widen this range.

Second, Figure 11(a) and (c) reveals that the inverter input, in fact, rises above V_{DD} (or falls below ground), possibly stressing one of the inverter's transistors.

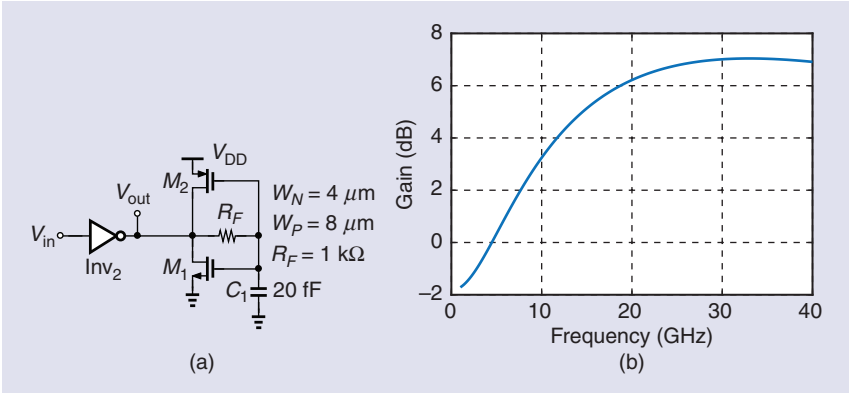

FIGURE 13: (a) A CTLE using an active inductor and (b) its frequency response.

The Active Inductor

It is possible to configure a feedback loop such that it presents an inductive input impedance across some frequency range, hence the term "active inductor."

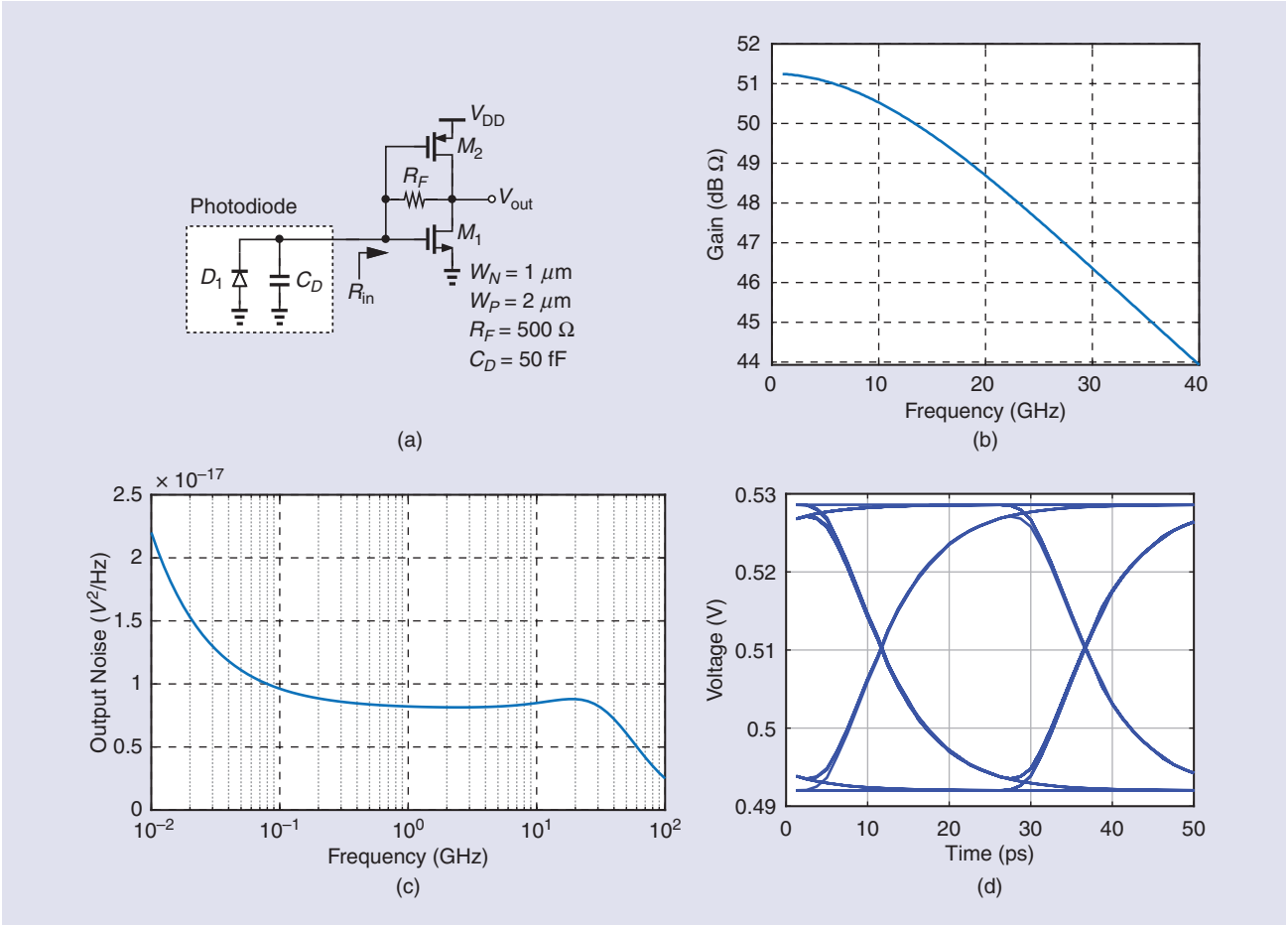

FIGURE 14: (a) An optical receiver using an inverter-based TIA, (b) the TIA's gain, (c) the TIA's output noise spectrum, and (d) the TIA's output eye diagram.

The self-biased inverter studied in previous sections can create such an impedance. As illustrated in Figure 12(a) [4], at low frequencies, $Z_{in} = (r_{O1} \| r_{O2}) \| \ (g_{m1} + g_{m2})^{-1}$, a low value, and at high frequencies, $Z_{in} = (r_{O1} \| r_{O2}) \| R_F$, a large value [Figure 12(b)]. The equivalent inductance is roughly equal to $R_F C_1 / (g_{m1} + g_{m2})$. Figure 12(c) plots this behavior for $R_F = 1\,\text{k}\Omega$, $C_1 = 20\,\text{fF}$, $W_N = 4\,\mu\text{m}$, and $W_P = 8\,\mu\text{m}$. The slope of $|Z_{in}|$ beyond the zero frequency yields $L = 1.4$ nH, somewhat close to the theoretical value of $R_F C_1 / (g_{m1} + g_{m2}) = 1.9$ nH.

The response depicted in Figure 12(c) is reminiscent of that of continuous-time linear equalizers (CTLEs). We can then utilize the circuit as the load of another inverter so as to construct a CTLE [4]. Illustrated in Figure 13(a), such an arrangement proves attractive, as it consumes less voltage headroom than topologies using differential pairs. Figure 13(b) displays the resulting small-signal behavior, revealing 9 dB of boost around 20 GHz. The circuit consumes 0.65 mW. Of course, the common-mode level of the data arriving at the input of Inv_2 must be accurately set so as to ensure that this inverter does not fight the bias point of M_1 and M_2.

The Transimpedance Amplifier

In optical communication receivers, a photodiode converts the light intensity provided by a fiber to an electric current. A TIA is thus necessary to transform this current to a voltage. The input resistance, bandwidth, and noise of the TIA prove critical here.

As evident in Figure 14(a), an optical receiver front end must present a low resistance, R_{in}, to the photodiode's capacitance to guarantee sufficient bandwidth for the incoming data. In a manner similar to the LNA of Figure 8(c), an inverter with a feedback resistor can play such a role. The pole formed by the input resistance—expressed by (6)—and C_D should preferably exceed $0.7 r_b$, where r_b is the bit rate. For example, if C_D = 50 fF and r_b = 40 Gb/s, we must have $R_{in} \approx 114\,\Omega$.

Additionally, the TIA's input-referred noise current must be small enough to yield an acceptable BER for a given received optical power and, hence, a given peak current produced by the photodiode. Neglecting channel length modulation and assuming $(g_{m1} + g_{m2}) R_F \gg 1$, we can express the noise of the circuit in Figure 14(a) as

$$\overline{I_{n,in}^2} \approx \frac{4kT\gamma}{(g_{m1} + g_{m2}) R_F^2} + \frac{4kT}{R_F}. \quad (10)$$

Figure 14(b) plots the circuit's transimpedance gain, implying a value of $51\,\text{dB}\Omega \equiv 360\,\Omega$ and a 3-dB bandwidth of 25 GHz. Presented in Figure 14(c) is the output noise voltage spectrum, whose area from 10 MHz to 100 GHz amounts to $600 \times 10^{-9}\,\text{V}^2$. As explained in [5], we divide this value by $(\pi/2)(360\,\Omega)^2(18\,\text{GHz})$ and take the square root, arriving at an input-referred noise current of $13\,\text{pA}/\sqrt{\text{Hz}}$. Figure 14(d) displays the output eye diagram at 40 Gb/s in response to a peak input current of 100 μA.

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EDITOR'S NOTE

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