Behzad Razavi

The Ring Oscillator

Ring oscillators are commonly used in many systems because of their wide tuning range, compact layout, and ability to generate multiple phases. These advantages over inductance–capacitance (*LC*) oscillators come at the cost of phase noise.

The concept of an oscillator consisting of gain stages in a ring can be traced to the vacuum-tube era. For example, in his 1953 patent, Gallay presented the structure shown in Figure 1, where nine triodes form an oscillating loop. The grid (G), cathode (C), and anode (A) of a triode can be visualized as the gate, source, and drain, respectively, of a MOSFET. CMOS ring oscillators began to appear in communication circuits in the late 1980s [2], [3]. In this article, we study single-ended and differential ring topologies and analyze their design tradeoffs.

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Basic Structure

In its simplest form, a ring oscillator comprises N gain stages in a loop, with negative feedback at low frequencies to avoid latch-up. If each stage inverts, then N must be odd (Figure 2). A rising edge at a node within the loop travels through N inverters and returns as a falling edge, forming one half of the oscillation period T_0. Thus, T_0 is equal to $2NT_D$, where T_D denotes the large-signal gate delay.

The inverter-based ring shown in Figure 2 merits three remarks. First, since the delay of an inverter falls as the supply voltage V_{DD} increases, the oscillation frequency f_0 is inversely proportional to V_{DD}. This supply sensitivity, K_{VDD}, proves serious as noise on V_{DD} directly modulates the output frequency. Second, for a total load capacitance of C_L at each node in Figure 2, the average power drawn from V_{DD} is approximately equal to $Nf_0C_LV_{DD}^2$. Third, an N-stage ring provides N output phases with a minimum separation of T_D seconds or $[T_D/(2NT_D)](2\pi) = \pi/N$ rad, but, due to the inversion in each stage, the actual phase difference is $-\pi + \pi/N$.

The problem of supply noise can be greatly alleviated through the use of differential rings. In an implementation such as the one shown in Figure 3, we prefer that the differential pairs experience nearly complete switching and, hence, produce a single-ended voltage swing equal to $I_{SS}R_D$. To this end, we select these transistors wide enough so that, with an input voltage difference of $I_{SS}R_D$, one transistor turns off. However, a ring consisting of only three stages does not provide complete switching because the delay through the loop is too short to allow V_X and V_Y to reach V_{DD}. It can be shown [4] that the maximum swing is approximately $0.5I_{SS}R_D$ in this case. For reasonable supply rejection, the tail current source must operate in the saturation region.

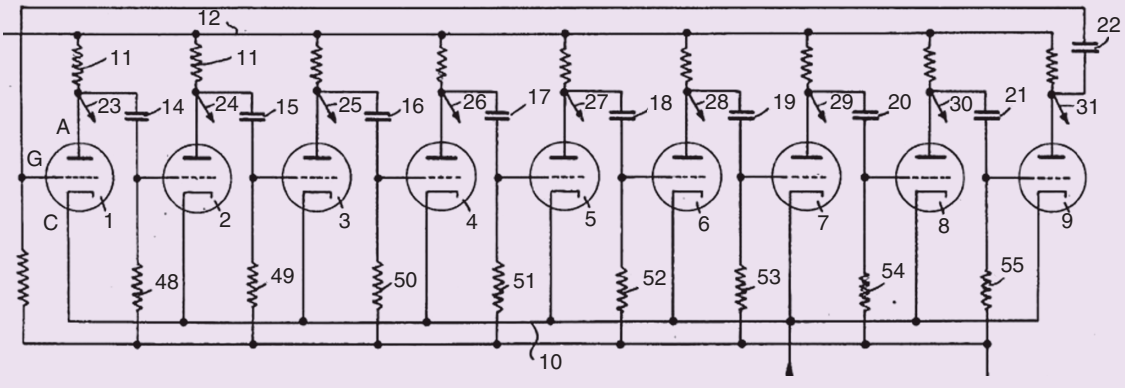

FIGURE 1: The ring oscillator described by Gallay. G: grid; C: cathode; A: anode.

Another advantage of differential rings is that they can provide multiple phases having a minimum spacing equal to π divided by an even number. This is possible because a differential ring with an even N can still have negative feedback at low frequencies.

Performance Studies

We wish to quantitatively study the behavior of inverter-based and differential ring oscillators and compare their performance in terms of phase noise, power consumption, and supply sensitivity. We design the two for roughly the same oscillation frequency in 40-nm technology and simulate them in the slow–slow corner at 75 °C and with a worst-case supply voltage of 0.95 V. We also include some explicit load capacitance at each node as an estimate of the layout parasitics.

Figure 4 depicts the inverter-based ring along with its waveform and phase-noise profile. The circuit runs at $f_0 = 22.6$ GHz, draws 57 μW, and exhibits a K_{VDD} of 50.2 GHz/V, a very large value. The phase noise falls with a slope of approximately 30 dB/dec from 100-kHz offset to 100-MHz offset, revealing the dominance of upconverted flicker noise.

The phase noise is excessively high, but it can be simply traded for power by "linear scaling": if we multiply the widths of all of the transistors by M, f_0 and the supply sensitivity remain constant (if the layout parasitics are scaled) while the power consumption rises by the same factor and the phase noise falls by $10 \log M$. For example, selecting $(W/L)_N = (100 \times 120\,\text{nm})/40\,\text{nm}$ and $(W/L)_P = (100 \times 240\,\text{nm})/40\,\text{nm}$ raises the power to 5.7 mW and reduces the phase noise at 1-MHz offset from –47 dBc/Hz to –67 dBc/Hz. Of course, the area also grows proportionally.

Shown in Figure 5 are the differential ring, its waveforms, and its phase-noise profile. Operating at $f_0 = 20.8$ GHz, the oscillator consumes 285 μW and has a K_{VDD} of 1.82 GHz/V. We recognize that V_X and V_Y do not have time to reach $V_{DD} = 0.95$ V, and the single-ended voltage swing is 270 mV_{pp}, somewhat close to our estimate of $0.5 I_{SS} R_D = 300$ mV. The transistors do not enter the triode region, a point to which we return later in the context of flicker noise. The phase noise displays a slope of nearly –30 dB/dec from 100-kHz offset to 1-MHz offset and –20 dB/dec thereafter. That is, flicker noise upconversion is much less pronounced here. Linear scaling can also be applied to the differential ring by multiplying $W_{1,2}$ and I_{SS} by a factor of M and dividing R_D by the same factor.

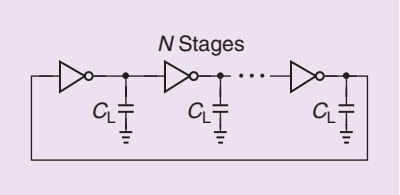

FIGURE 2: A ring oscillator consisting of N inverters.

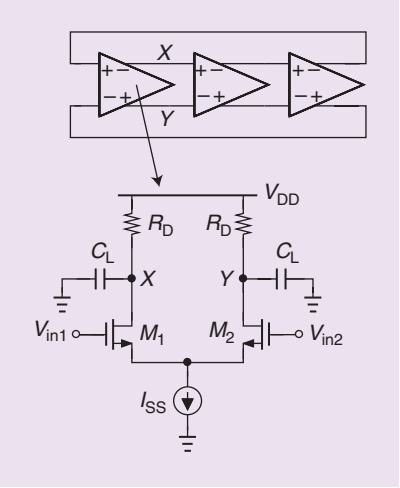

FIGURE 3: A three-stage differential ring oscillator.

Let us now compare the two designs. Why is the supply sensitivity of the first ring so much higher than that of the second? This is because the supply dependence of the delay is different in the two designs. In an inverter, the drive strength depends on V_{DD}; that is, the drain current and on-resistance of the transistors directly and substantially change as V_{DD} fluctuates. In a differential pair, on the other hand, the load resistance is relatively constant, and only the capacitance has a slight supply dependence. Illustrated in Figure 6, this effect arises from the nonlinear drain-bulk capacitance, C_{DB}, of M_1 and M_2, which varies with the common-mode voltage at X and Y and, hence, with V_{DD}.

To compare the phase-noise profiles fairly, we must normalize them to the oscillation frequency and the power consumption. This can be accomplished by defining a figure of merit (FOM) as follows:

$$\text{FOM} = 10 \log \frac{f_0^2}{\Delta f^2 P_{\text{mW}} S_{\phi n}(\Delta f)}, \quad (1)$$

where Δf denotes the offset frequency at which the phase noise, $S_{\phi n}(\Delta f)$, is measured and P_{mW} is the power consumption expressed in milliwatts. Table 1 summarizes the two oscillators' performance parameters. As a

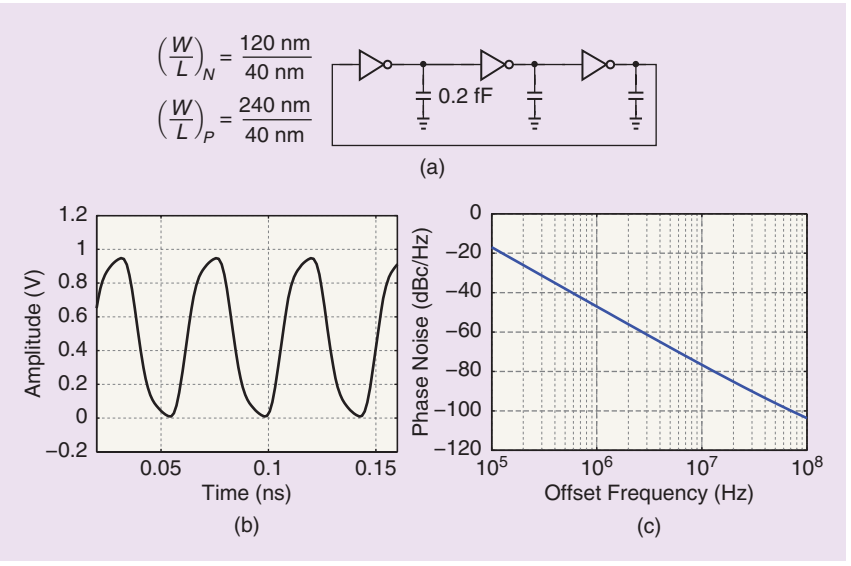

FIGURE 4: (a) A ring oscillator design example, (b) its waveform, and (c) its phase-noise profile.

point of reference, we note that the FOM of *LC* oscillators lies in the vicinity of 190 dB.

The differential ring provides higher performance than the inverter-based design at $\Delta f = 100$ kHz but not at $\Delta f = 100$ MHz. In other words, the former exhibits less phase noise due to flicker noise but greater phase noise due to thermal noise. To understand the reason, we first recognize that the flicker noise of the inverter transistors in Figure 4(a) directly modulates the voltage transitions and translates to phase noise. In Figure 5(a), on the other hand, the flicker noise of M_1 and M_2 is not upconverted if the rising and falling edges of V_X and V_Y are symmetric [5], which is nearly the case in Figure 5(b). However, if M_1 and M_2 enter the triode region, this symmetry degrades, and the flicker noise of these transistors upconverts to greater phase noise.

The thermal-regime phase noise of the first ring is lower primarily because of its greater voltage swings. The ratio of the two oscillators' single-ended swings is approximately $3.5 (\equiv 11\,\text{dB})$, close to their FOM difference at 100-MHz offset.

The foregoing observations suggest that the choice between the two ring topologies depends on two factors.

- If the regulator providing the oscillator supply voltage suffers from substantial noise, then a differential ring is preferable, but at the cost of greater phase noise at high offset frequencies.
- If the phase-locked loop containing the oscillator has a wide bandwidth, thus suppressing the flicker-noise-induced phase noise, then an inverter-based ring can be utilized for its lower thermal-noise-induced phase noise.

In other words, it is ultimately the total area under the phase-locked oscillator's phase-noise profile—the integrated jitter—that determines this choice.

Ring Oscillators With 45° or 90° Phase Separations

Many applications call for oscillators that have multiple phases, with a minimum separation equal to π divided by an even number. We first consider a four-stage differential ring as a candidate for delivering 45° phase spacings. What can we predict about the phase noise and FOM of such a topology? Since the ring is longer, we expect that the voltage swings are closer to $I_{SS}R_D$, helping to reduce the phase noise. However, for a given power consumption, the use of four stages—rather than three—means that the bias current per stage is lower. As shown in [5], the phase noise at an offset of Δf in the thermal regime is given by

$$S_{\phi n}(f) = \frac{8kT}{3I_{SS}}\left(\frac{\gamma}{V_{GS}-V_{TH}}+\frac{1}{I_{SS}R_D}\right)\left(\frac{f_0}{\Delta f}\right)^2, \quad (2)$$

where γ is the noise coefficient of MOSFETs and $V_{GS}-V_{TH}$ is the overdrive of the differential-pair transistors when they carry half of I_{SS}.

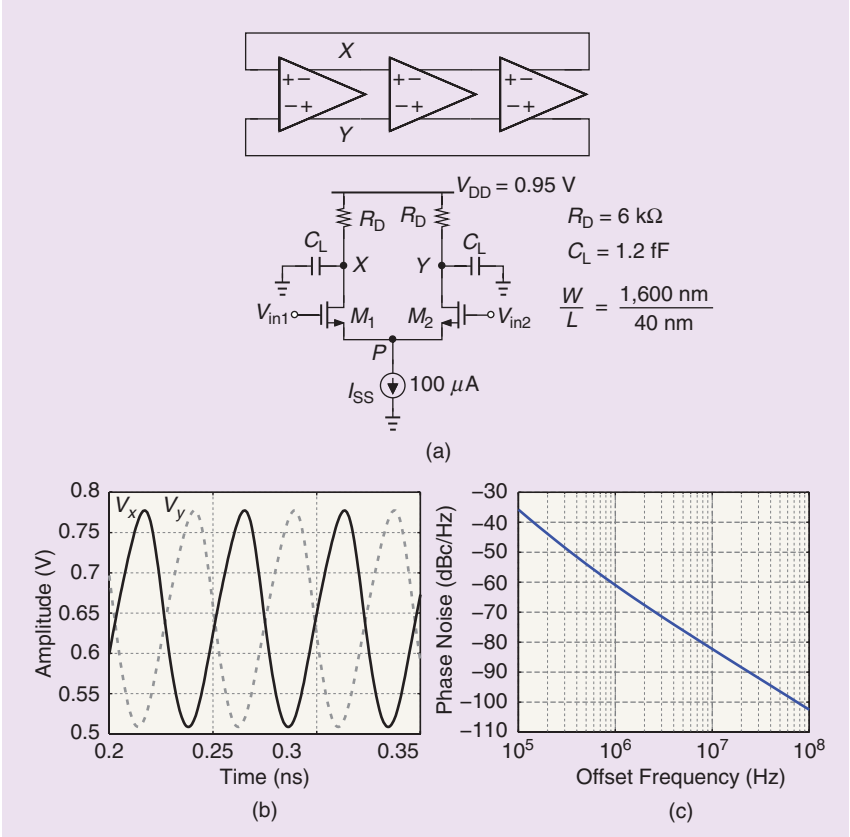

FIGURE 5: (a) A differential ring oscillator design example, (b) its waveforms, and (c) its phase noise.

TABLE 1. A COMPARISON OF INVERTER-BASED AND DIFFERENTIAL RINGS.

				FOM (dB)	
RING TYPE	**f_0 (GHz)**	**P (mW)**	**K_{VDD} (GHz/V)**	**Δf = 100 kHz**	**Δf = 100 MHz**
Inverter-based ring	22.6	0.057	50.2	137	164
Differential ring	20.8	0.285	1.82	148	154

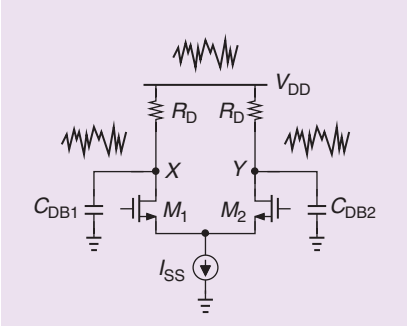

FIGURE 6: Modulation of drain-bulk capacitances by supply noise.

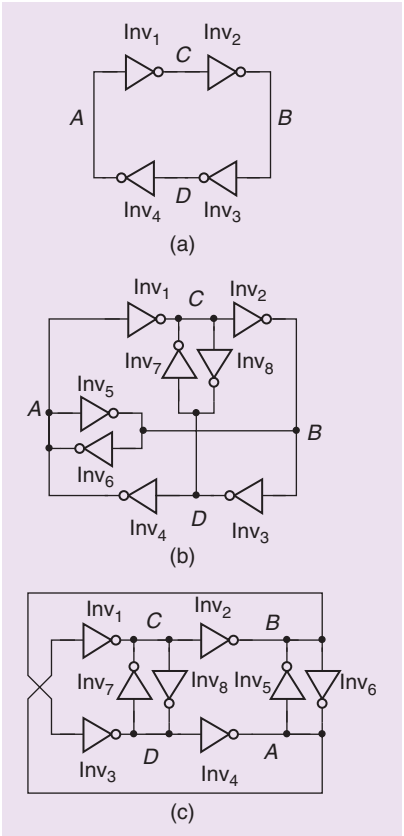

FIGURE 7: (a) A four-stage ring. (b) The addition of cross-coupled inverters to avoid latch-up. (c) A redrawing of the topology in (b).

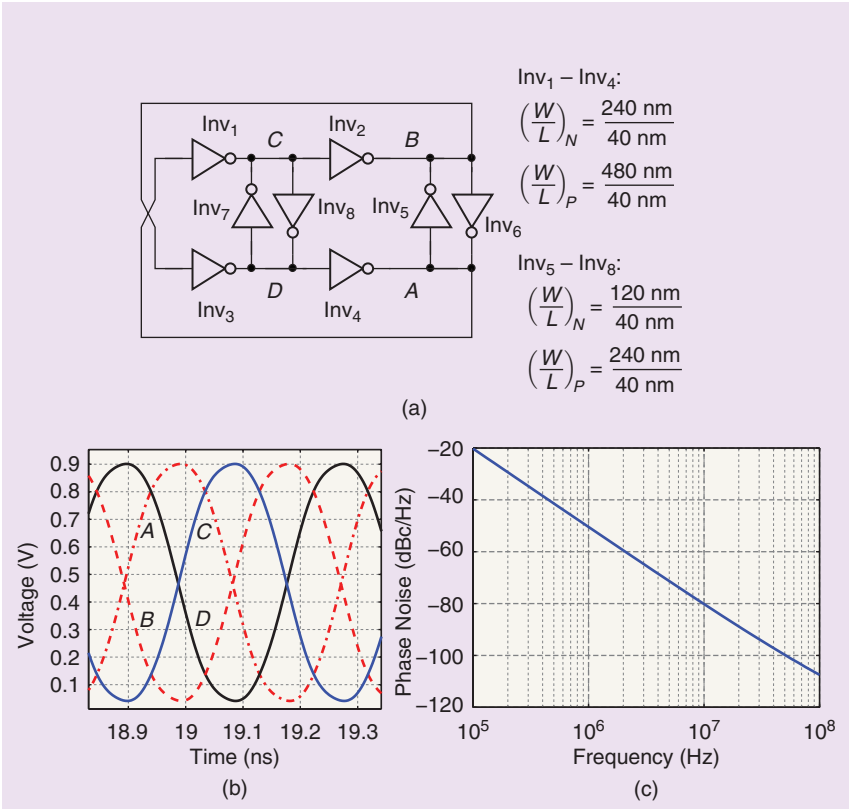

FIGURE 8: (a) A quadrature oscillator design example, (b) its output waveforms, and (c) its phase noise.

This expression assumes that the single-ended voltage swing is equal to $I_{SS}R_D$. We observe that $S_{\phi n}$ rises if I_{SS} falls and $I_{SS}R_D$ remains constant. According to simulations, the increase in the swing and the decrease in I_{SS} partially cancel each other, yielding a 1-dB degradation in the FOM for the four-stage differential ring.

We next turn to the inverter-based oscillator of Figure 2 and ask how it can be modified to provide quadrature outputs. Let us begin with the four-stage loop shown in Figure 7(a). Ignoring for the moment the inversion provided by each stage, we recognize that the circuit can oscillate at a frequency $f_0 = 1/(8T_D)$. Thus, A and B carry complementary waveforms, and so do C and D. Also, the latter two are 90° out of phase with respect to the former two. From another perspective, the loop consists of four one-pole stages, thereby generating 90° phase separations between consecutive nodes—if it oscillates.

Unfortunately, the circuit of Figure 7(a) prefers to latch up: the loop can indefinitely maintain $A = B = 1$ and $C = D = 0$ or vice versa. We must, therefore, devise a mechanism that avoids this condition. For example, we can tie a circuit between A and B to discourage them from reaching the same state. Such a circuit is readily realized by a pair of cross-coupled inverters because they fight equal logical states at their input and output nodes. This point leads to the structure depicted in Figure 7(b), often redrawn as in Figure 7(c). The topology was reported in [6].

How should the cross-coupled inverters be sized with respect to those in the main loop? The former must fight the latter if Inv_1–Inv_4 tend toward latch-up. From this perspective, Inv_5–Inv_8 should be strong enough. On the other hand, these inverters also fight Inv_1–Inv_4 during transitions, both draining power and injecting noise. Thus, Inv_5–Inv_8 should not be excessively strong. As a rule of thumb, we choose a ratio of two between the strengths of Inv_1–Inv_4 and those of Inv_5–Inv_8. Greater ratios run the risk of latch-up in the presence of mismatches, and lower ratios degrade the FOM.

Let us design the circuit of Figure 7(b) and study its performance. Returning to our ring design in Figure 4(a) and assuming a minimum allowable width of 120 nm for the transistors, we choose for the main inverters $(W/L)_N = 240$ nm/40 nm and $(W/L)_P = 480$ nm/40 nm and for the cross-coupled inverters $(W/L)_N = 120$ nm/40 nm and $(W/L)_P = 240$ nm/40 nm [Figure 8(a)]. Plotted in Figure 8(b), the quadrature waveforms exhibit a slight swing degradation due to the fight between the main and cross-coupled inverters. The oscillation frequency, f_0, is equal to 26.5 GHz, and the supply current is 235 μA.

(continued on p. 81)

Electrical Engineering and Computer Science until 1994.

He received the nation's highest professional distinction for engineers in 2015, when he was elected to the National Academy of Engineering. His work in analog circuits has improved technologies including cell phones and medical devices, and the students he has mentored through the years have multiplied the impact of his work. Current doctoral student Yanchao Wang says Temes is known for his research expertise and patient mentorship, and she appreciates his example of leading a balanced life.

Temes, now 90, hikes in the woods every day. On Saturdays, his graduate students join him to talk about their research and anything else. "I have passed retirement age many years ago, but I cannot stop my addiction to the fun aspects of my job," Temes said.

—Rachel Robertson

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A CIRCUIT FOR ALL SEASONS

(continued from p. 13)

Figure 8(c) plots the phase noise of the quadrature oscillator. At 1-MHz offset, the phase noise is equal to −50 dBc/Hz, 3 dB lower than that of the reference design. For a fair comparison, we must take into account 1) the supply current ratio, $10\log(235\,\mu\text{A}/60\,\mu\text{A}) = 5.9\,\text{dB}$, and 2) the frequency ratio, $20\log(26.5\,\text{GHz}/22.6\,\text{GHz}) = 1.4\,\text{dB}$. Thus, the quadrature design's FOM is worse by $5.9 - 1.4 - 3 = 1.5\,\text{dB}$. This is the penalty paid for generating quadrature phases.

Tolerable Supply Noise

Oscillators are typically supplied from an on-chip low-dropout (LDO) regulator, which itself suffers from output noise. Consider the arrangement shown in Figure 9, where the LDO noise is denoted by V_n and has a spectrum $S_{\text{VDD}}(f)$. We wish to determine how much LDO noise our oscillators can tolerate while experiencing a negligible rise in their phase noise. A typical on-chip LDO displays roughly 10–20 nV/$\sqrt{\text{Hz}}$ of noise at 1 MHz.

The supply noise directly modulates the oscillation frequency, yielding an output of the form

$$V_{\text{out}}(t) = V_0 \cos\left[\omega_0 t + K_{\text{VDD}} \int V_n(t)\,dt\right], \tag{3}$$

where $\omega_0 = 2\pi f_0$. The second term within the argument of the cosine represents phase noise, $S_{\phi,\text{VDD}}$, and its spectrum is obtained by subjecting S_{VDD} to an integrator transfer function:

$$S_{\phi,\text{VDD}} = S_{\text{VDD}} \frac{K_{\text{VDD}}^2}{\omega^2}. \tag{4}$$

This phase noise must fall well below the intrinsic phase-noise profiles $S_{\phi n}$ obtained in the previous sections. We write

$$S_{\text{VDD}} \frac{K_{\text{VDD}}^2}{4\pi^2 f^2} \ll S_{\phi n}(f). \tag{5}$$

For example, at 1-MHz offset, we have, from Figure 4(c), $S_{\phi n} = -47\,\text{dBc/Hz}$, which, with $K_{\text{VDD}} = 50.2\,\text{GHz/V} = 2\pi(50.2)\,\text{Grad/s/V}$, gives

$$S_{\text{VDD}} \ll \frac{4\pi^2 f^2}{K_{\text{VDD}}^2} S_{\phi n} \tag{6}$$

$$\ll 7.9 \times 10^{-15}\ \text{V}^2/\text{Hz}. \tag{7}$$

This result implies that S_{VDD} should be well below 89 nV/$\sqrt{\text{Hz}}$. Such a relaxed noise requirement appears to impose no severe restriction on the LDO design, but recall that the excessive phase-noise value of −47 dBc/Hz must eventually be lowered by linear scaling. For example, if we allow a power dissipation of $100 \times 57\,\mu\text{W} = 5.7\,\text{mW}$ for a 20-GHz oscillator, the phase noise can be reduced by 20 dB. This, in turn, demands that the LDO noise at 1 MHz fall to well below 8.9 nV/$\sqrt{\text{Hz}}$, a formidable challenge.

Let us repeat the foregoing calculations for the differential ring of Figure 5(a). For a fair comparison, suppose we apply linear scaling to this circuit to obtain $S_{\phi n}(1\,\text{MHz}) = -67$ dBc/Hz. This means that, with $K_{\text{VDD}} = 1.82\,\text{GHz/V} = 2\pi(1.82)\,\text{Grad/s/V}$, we have

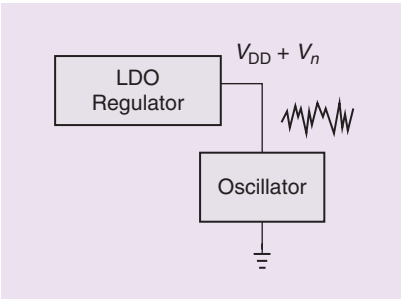

FIGURE 9: Modulation of an oscillator by LDO noise.

$$S_{\text{VDD}} \ll \frac{4\pi^2 f^2}{K_{\text{VDD}}^2} S_{\phi n} \tag{8}$$

$$\ll 6.02 \times 10^{-14}\ \text{V}^2/\text{Hz}. \tag{9}$$

In other words, the LDO thermal noise should be well below $\sqrt{6.02 \times 10^{-14}\ \text{V}^2/\text{Hz}} = 245$ nV/Hz, a far more relaxed requirement than the 8.9 nV/$\sqrt{\text{Hz}}$ bound for the first design.

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