10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-μm CMOS Technology

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***Abstract*—A limiting amplifier incorporates active feedback, inductive peaking, and negative Miller capacitance to achieve a voltage gain of 50 dB, a bandwidth of 9.4 GHz, and a sensitivity of 4.6 mV_{pp} for a bit-error rate of 10^{-12} while consuming 150 mW. A driver employs T-coil peaking and negative impedance conversion to achieve operation at 10 Gb/s while delivering a current of 100 mA to 25-Ω lasers or a voltage swing of 2 V_{pp} to 50-Ω modulators with a power dissipation of 675 mW. Fabricated in 0.18-μm CMOS technology, both prototypes operate with a 1.8-V supply.**

***Index Terms*—Broadband amplifiers, inductive peaking, laser drivers, limiting amplifiers, T-coils.**

I. Introduction

THE trend toward full integration of broadband transceivers [1], [2] makes it desirable to realize front-end circuits such as limiting amplifiers (LAs) and laser/modulator drivers (LMDs) in CMOS technology. While CMOS devices present difficult challenges in the design of these circuits, the need for higher port density and lower power dissipation motivates further research on broadband CMOS techniques.

It is the purpose of this paper to demonstrate that CMOS technology can be used to realize two of the critical building blocks in a typical optical system, namely, the LA in the receiver (RX) and the LMD in the transmitter (TX). These circuits may serve as standalone functions in optical modules or coexist with serializers and deserializers on the same chip. This paper introduces various device and circuit techniques that overcome the technology limitations and allow the operation of these circuits at 10 Gb/s with low supply voltages.

Section II reviews system-level considerations and design tradeoffs for LAs and LMDs in a typical optical transceiver. Sections III and IV present the architecture and circuit design of the LA and the LMD, respectively. Section V summarizes the experimental results.

II. General Considerations

A. Limiting Amplifiers

As the intermediate stage between a transimpedance amplifier (TIA) and a clock and data recovery (CDR) circuit, the LA must satisfy a number of requirements. With a typical received average optical power of -18 dBm, a large extinction ratio, a photodiode responsivity of about 0.75 A/W, and a TIA gain of 1 kΩ, the LA senses a signal level of 11.9 mV. Thus, the LA must exhibit a gain higher than 40 dB to provide sufficiently large voltage swings for the subsequent CDR and decision circuits. Moreover, the circuit bandwidth must approach 10 GHz to introduce negligible intersymbol interference (ISI).

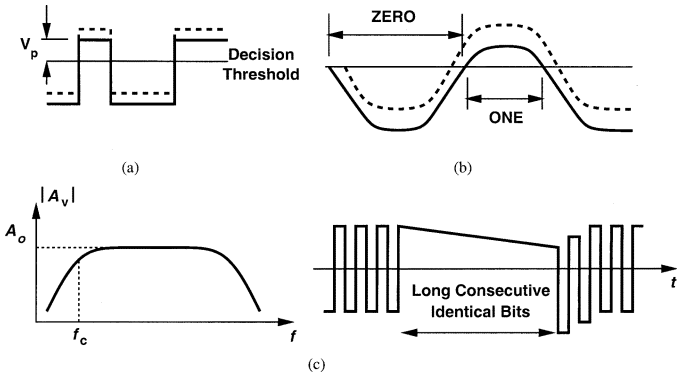

Fig. 1. (a) Sensitivity degradation due to offset. (b) Pulsewidth distortion due to offset. (c) Effect of offset cancellation in frequency and time domains.

In addition to a large gain and wide bandwidth, the LA must also achieve a relatively low input-referred noise so as not to limit the overall RX sensitivity. With a received signal current $I_{in} = 12\ \mu$A and a bit-error rate (BER) of 10^{-12}, the total noise current referred to the receiver input must be below $\sqrt{\overline{I^2_{n,in}}} = \overline{I_{in}/7} = 1.7\ \mu A_{rms}$. All circuits in the RX chain contribute to $\overline{I^2_{n,in}}$ where the LA input-referred noise voltage is scaled by the transimpedance gain when referred to the receiver input. Allocating 20% of $\overline{I^2_{n,in}}$ to the LA noise, the LA input sensitivity should be less than 4.75 mV_{pp}.

The LA offset may also impact the receiver performance. As shown in Fig. 1(a), vertical shift of the signal with respect to the decision threshold reduces the peak signal level, degrading the receiver sensitivity. In addition, the LA offset leads to pulsewidth distortion [Fig. 1(b)] complicating the design of the CDR circuit. Continuous-time offset cancellation circuits introduce a lower cutoff frequency in the transfer function and "droop" in the time domain after long runs (also known as baseline wander) [Fig. 1(c)]. At the end of the droop period, the signal is again shifted with respect to the decision threshold. To minimize this effect, the lower cutoff frequency must be sufficiently small, typically on the order of a few tens of kilohertz.

B. Laser and Modulator Drivers

Optical transmitters impress the data upon light through one of two techniques. In "direct modulation," a driver directly turns

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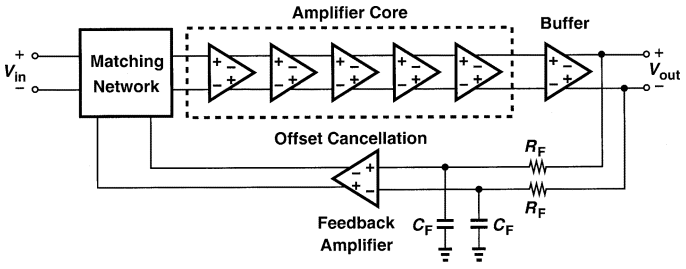


Fig. 2. Limiting amplifier architecture.

a laser on and off, but laser nonidealites such as chirping and relaxation oscillation may corrupt the optical output. In "external modulation," on the other hand, the laser itself operates continuously and its output is applied to an optical device such as a Mach–Zehnder modulator.

From the circuit-design point of view, laser and modulator drivers present somewhat different requirements. Lasers typically exhibit a low impedance (e.g., 5 Ω plus a 20-Ω series resistor) and run at a current level of around 100 mA. Modulators have a higher impedance ($\sim$50 Ω), but operate with voltage swings around 2.5 V and, hence, currents on the order of 50 mA. The overall voltage swing experienced by each driver is, therefore, in the vicinity of 2–2.5 V. Since LMDs must employ back-termination resistors at the output to suppress secondary reflections, the output stage is typically designed for a total current nearly twice the above values.[1]

III. Limiting Amplifier Design

A. LA Architecture

Shown in Fig. 2, the architecture of the LA consists of a broadband input-matching network, five identical gain stages comprising the LA core, an offset cancellation feedback loop, and an output buffer.

The LA core must provide sufficient gain and bandwidth while exhibiting a low input-referred noise. It is, therefore, desirable to employ wide transistors at the input, but at the cost of degrading the input impedance matching at high frequencies. For this reason, a broadband matching network using a T-coil network precedes the core [4].

Designed to operate as a standalone module, the LA must deliver large voltage swings to 50-Ω loads, requiring a high-current output buffer. The large input capacitance of the buffer mandates that the core itself provide a relatively low output impedance, thus prohibiting the use of inverse scaling [5]. As explained below, each stage in the core must achieve a bandwidth substantially greater than 10 GHz.

B. LA Building Blocks

1) Amplifier Core: A cascade of n identical gain cells, each having a bandwidth BW_c, exhibits an overall bandwidth of

$$\mathrm{BW}_{\mathrm{tot}} = \mathrm{BW}_c \sqrt[m]{2^{1/n} - 1} \tag{1}$$

[1]One exception is the design in [3], but at the cost of greater voltage headroom.

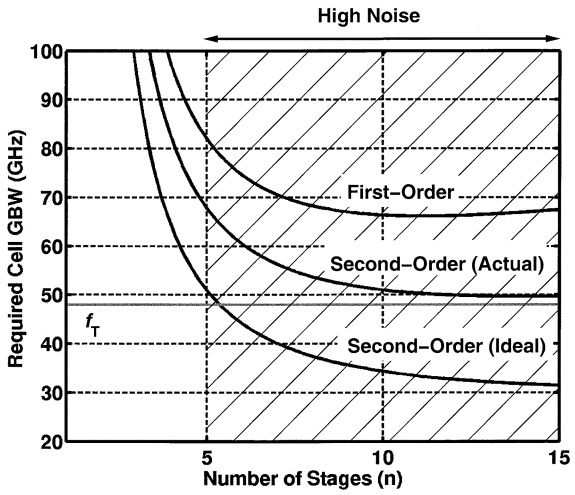


Fig. 3. Required cell GBW as a function of the number of stages n for $A_{\mathrm{tot}} = 50$ dB and $\mathrm{BW}_{\mathrm{tot}} = 10$ GHz.

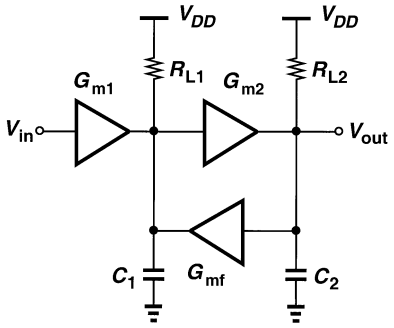


Fig. 4. Active-feedback architecture.

where m is equal to 2 for first-order stages and 4 for second-order stages [6]. For example, if $\mathrm{BW}_{\mathrm{tot}} = 10$ GHz and $n = 5$, then the cell bandwidth must exceed 26 GHz for $m = 2$ and 16 GHz for $m = 4$. More generally, for a total gain of A_{tot}, the required cell gain-bandwidth product GBW_c can be written as

$$\mathrm{GBW}_c = \frac{\mathrm{GBW}_{\mathrm{tot}}}{A_{\mathrm{tot}}^{1-1/n} \sqrt[m]{2^{1/n} - 1}} \tag{2}$$

where $\mathrm{GBW}_{\mathrm{tot}} = A_{\mathrm{tot}}\mathrm{BW}_{\mathrm{tot}}$ and $\mathrm{GBW}_c = {A_{\mathrm{tot}}}^{1/n}\mathrm{BW}_c$.

Fig. 3 plots the required cell GBW for a cascade of n first-order or second-order gain cells yielding $A_{\mathrm{tot}} = 50$ dB and $\mathrm{BW}_{\mathrm{tot}} = 10$ GHz. With $f_T \approx 48$ GHz in 0.18-μm CMOS technology, first-order stages are incapable of realizing such an amplifier. Ideal second-order stages perform better, but imperfections such as Miller effect and device junction capacitances (actual second-order plot) exacerbate the issue.

Another critical difficulty stems from the relationship between n and the overall input-referred noise. For a larger n, the lower gain per stage leads to rapid accumulation of noise. For the input-referred noise levels targeted in this design, n must fall below approximately 5.

This work introduces active negative feedback as a means of improving the GBW of amplifiers. Illustrated in Fig. 4, such an arrangement employs a transconductance stage G_{mf} to return a

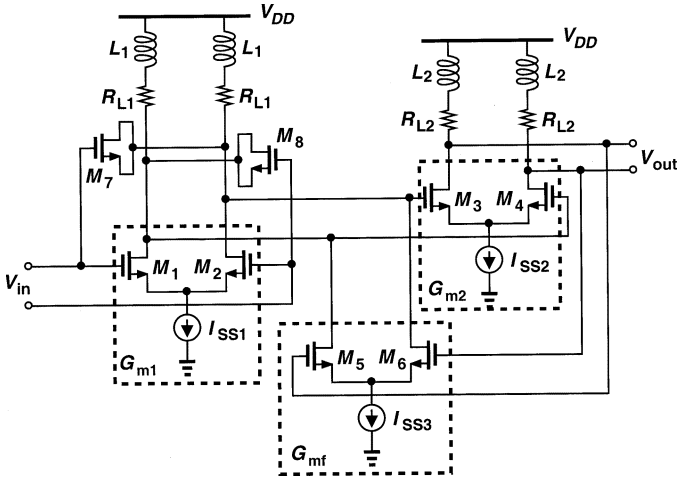


Fig. 5. Active-feedback cell realization.

fraction of the output to the input of G_{m2}. Unlike the conventional Cherry–Hooper amplifier [7], active feedback does not resistively load the transimpedance stage. The transfer function of the overall amplifier is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A_{vo}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3}$$

where

$$A_{vo} = \frac{G_{m1}G_{m2}R_{L1}R_{L2}}{1 + G_{m2}G_{mf}R_{L1}R_{L2}} \tag{4}$$

$$\zeta = \frac{1}{2}\frac{R_{L1}C_1 + R_{L2}C_2}{\sqrt{R_{L1}R_{L2}C_1C_2(1 + G_{mf}G_{m2}R_{L1}R_{L2})}} \tag{5}$$

$$\omega_n^2 = \frac{1 + G_{mf}G_{m2}R_{L1}R_{L2}}{R_{L1}R_{L2}C_1C_2}. \tag{6}$$

For a maximally-flat Butterworth response, $\zeta = \sqrt{2}/2$ and the -3-dB bandwidth, $\omega_{-3\text{dB}} = 2\pi f_{-3\text{dB}} = \omega_n/(2\pi)$. Multiplying (4) by (6), we thus have

$$A_{vo}{\omega_{-3\text{dB}}}^2 = \frac{G_{m1}G_{m2}}{C_1C_2} \tag{7}$$

or

$$A_{vo}\omega_{-3\text{dB}} = \frac{G_{m1}G_{m2}}{C_1C_2}\frac{1}{\omega_{-3\text{dB}}}. \tag{8}$$

Since $G_{m1}/C_1 \approx G_{m2}/C_2 \approx 2\pi f_T$, (8) can be rewritten as

$$A_{vo}\omega_{-3\text{dB}} = f_T\frac{f_T}{f_{-3\text{dB}}}. \tag{9}$$

This result reveals that active feedback increases the GBW beyond the technology f_T by a factor equal to the ratio of f_T and the cell bandwidth.

In addition to active feedback, each cell also employs inductive peaking and negative Miller capacitance [8]. Fig. 5 shows the overall gain stage, where M_7 and M_8 partially cancel the effect of gate–drain and gate–source capacitors of M_1 and M_2. Since M_7 and M_8 sustain a gate–source voltage of near zero, they are realized by placing nMOS devices inside an n-well (similar to MOS varactors), thus providing a greater fraction of the gate-oxide capacitance and, hence, better tracking with M_1 and M_2.

TABLE I
DESIGN VALUES FOR THE ACTIVE FEEDBACK GAIN CELL

Parameter	Value
W/L_{1-4}	32 μm/0.18 μm
W/L_{5-6}	4 μm/0.18 μm
W/L_{7-8}	20 μm/0.5 μm
I_{SS1}, I_{SS2}	6 mA
I_{SS3}	0.5 mA
R_{L1}, R_{L2}	210 Ω
L_1	1.75 nH
L_2	1.0 nH

Fig. 6 shows the progressive improvement in the 10-Gb/s eye opening at the output of the five-stage core as each circuit technique is applied (the last stage is loaded by the input capacitance of the output buffer). Active feedback greatly improves the performance, and inductive peaking and negative Miller capacitors produce a completely open eye with minimal added power consumption and voltage headroom.

Table I summarizes the design values for the gain cell of Fig. 5. The inductors are realized as metal-6 spirals to minimize their parasitic capacitance to the substrate. Symmetric inductors are attractive here, but they lead to routing difficulties between the stages [9]. Thus, asymmetric inductors are used.

The variation of the load resistors in the gain stages with process and temperature leads to a departure from optimal inductive peaking, thus degrading the performance. Simulations reveal an eye closure of 1 dB for a $\pm 15\%$ variation in R_{L1} and R_{L2} in Fig. 5.

2) Output Buffer: Buffers driving off-chip loads typically present a bandwidth bottleneck resulting from the large input transistors that are necessary for high current drive capability. In broadband applications, the buffer must drive an on-chip back-termination resistor of about 75 Ω in addition to an off-chip load of 50 Ω [10]. To deliver a single-ended voltage swing of 0.5 V to the equivalent resistance of 30 Ω, the buffer must steer 17 mA, requiring a tail current of 20 to 25 mA when the incomplete switching of the stage is taken into account. Consequently, the input devices must be 120 μm wide.

This work employs an inductively peaked f_T doubler as the output buffer. Depicted in Fig. 7, the circuit exhibits an input capacitance roughly equal to half the gate–source capacitance of M_1 while providing the same transconductance as that of M_1. The penalty is higher power dissipation.[2]

3) Input Matching and Offset Cancellation: Fig. 8 illustrates the details of the input matching network and the offset cancellation loop. T-coils are added at the input to improve the impedance match even with the large input transistors used in the core [4]. Each T-coil occupies an area of $100\,\mu\text{m} \times 100\,\mu\text{m}$.

[2]Owing to complete switching, bipolar f_T doublers incur negligible power penalty. CMOS counterparts, on the other hand, cannot steer large tail currents with reasonable input transistor dimensions.

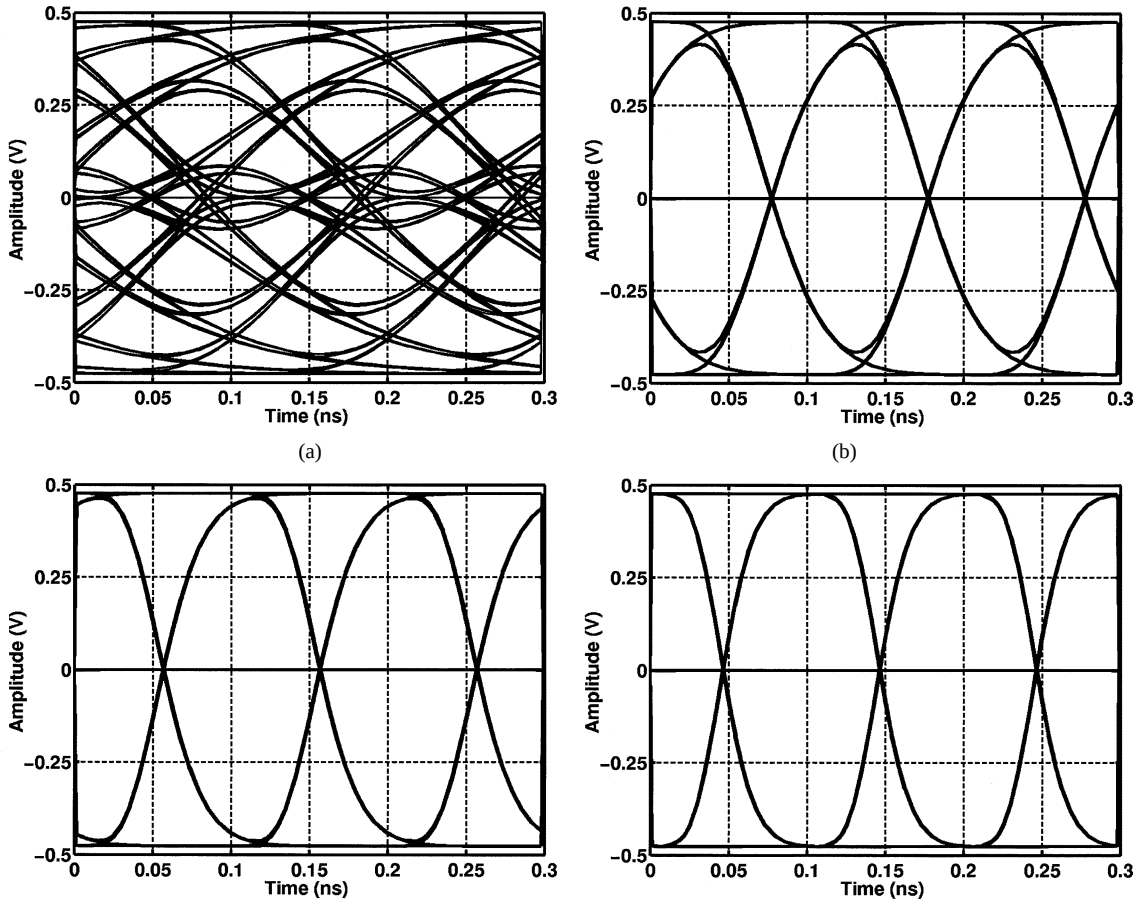


Fig. 6. Progressive improvement in core output. (a) Resistively-loaded differential pairs. (b) Active feedback added. (c) Inductive peaking added. (d) Negative capacitance added.

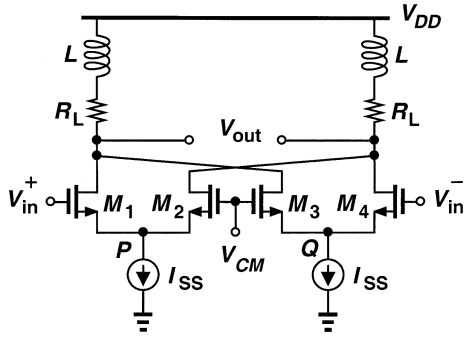


Fig. 7. Output buffer realized as an inductively peaked f_T doubler.

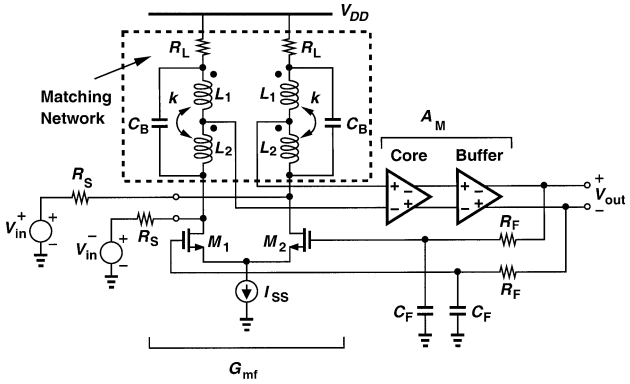


Fig. 8. Input matching and offset cancellation feedback circuit.

The principal difficulty in the design of the offset cancellation loop relates to the required corner frequency f_c of the resulting high-pass filter. In order to ensure negligible droop in the output in the presence of long runs, f_c must fall in the range of a few tens of kilohertz. In the circuit of Fig. 8

$$f_c = \frac{A_M A_{\rm FB}/2 + 1}{2\pi R_F C_F} \tag{10}$$

where $A_{\rm FB}$ denotes the low-frequency gain of the feedback network while the circuit is driven by a source impedance of R_s. With $A_M \approx 50$ dB and $A_{\rm FB} \approx 0$ dB, $R_F C_F$ must reach a few milliseconds for f_c to be equal to a few tens of kilohertz. In this work, a 13 MΩ poly resistor serves as R_F and a 150-pF MOS capacitor as C_F. Note that the distributed nature of the resistor's parasitic capacitance minimizes its impact on the speed of the output buffer.[3]

Another issue stems from the low load resistance seen by the feedback amplifier at the input of the LA. To compensate for an input-referred offset voltage of roughly 20 mV, M_1 and M_2 must steer about 1 mA to their loads while sensing an output

[3]One can view R_F as 10 kΩ + 1290 kΩ, noting that the first 10-kΩ portion exhibits negligible capacitance while isolating the buffer from the rest of R_F and its parasitic capacitance.

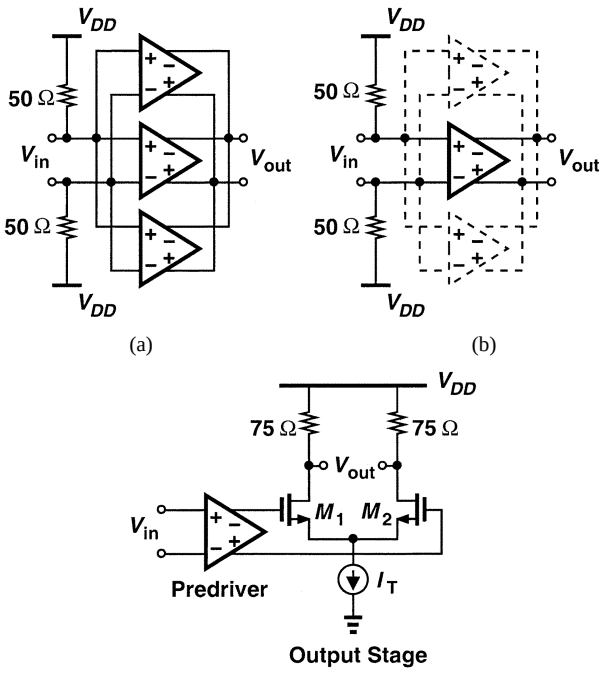


Fig. 9. LMD architecture. (a) Laser driver. (b) Modulator driver. (c) Details of one slice.

offset of less than 10 mV, a value determined by pulsewidth distortion requirements. Thus, these transistors must be sufficiently wide.

IV. Laser/Modulator Driver Design

LMDs are among the most challenging broadband circuits because they must deliver very large currents with high voltage swings. The LMD architecture, shown in Fig. 9, consists of three two-stage slices. For operation as a modulator driver, only one slice is enabled, as shown in Fig. 9(b), delivering approximately 40 mA to a 50-Ω load. To drive 25-Ω lasers,[4] on the other hand, all three slices are enabled, providing an output current exceeding 100 mA. Fig. 9(c) details each slice, consisting of a predriver followed by an output stage. Simulations and measurements indicate that the input and output capacitances of the disabled slices do not degrade the performance of the enabled slice.

The design of the LMD driver begins with the output stage and the required current swing. For a single slice to deliver 40 mA to a 50-Ω off-chip load and, hence, 27 mA to a 75-Ω on-chip termination, the tail current of the output stage, I_T, must exceed 67 mA. However, complete switching of the tail current necessitates large input swings and/or wide transistors, both of which make the design of the predriver stage difficult. Thus, the final choice of the tail current is determined after iterations between the two stages. In this design, I_T is approximately equal to 90 mA, each transistor in the differential pair has $W = 600\ \mu$m and $L = 0.18\ \mu$m, and the predriver output swing is 600 mV_{pp} (single-ended).

[4]Laser diodes exhibit a dynamic resistance of about 5 Ω. However, it is difficult to construct 5-Ω transmission lines on printed-circuit boards. Thus, a 20-Ω resistor is typically placed in series with the laser diode.

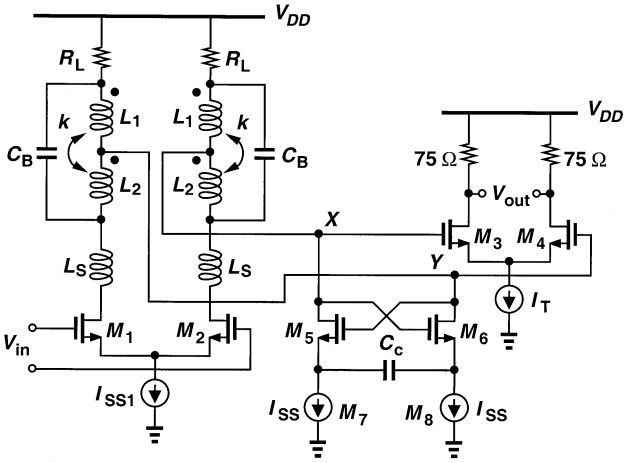


Fig. 10. Circuit realization of one slice in the driver.

The input capacitance of the output stage consists of the gate–source capacitance, which is approximately 0.75 pF, and the Miller multiplication of the gate–drain capacitance, which is about 0.88 pF. The result imposes a maximum load resistance of less than 10 Ω in the predriver for a bandwidth of about 10 GHz. To produce a single-ended swing of 600 mV_{pp}, the predriver must, therefore, employ a tail current greater than 62 mA!

The above observations suggest that the predriver is as power hungry and as difficult to design as the output stage. We also recognize that the output stage by itself cannot serve as an LMD because its input capacitance leads to substantial impedance mismatch at gigahertz frequencies.

This work presents three techniques that improve the bandwidth at the interface between the predriver and the output stage by about a factor of four, thereby lowering the predriver tail current by the same factor. The overall circuit realization of one slice is shown in Fig. 10.

1) Negative Capacitance: A negative impedance converter (NIC) consisting of M_5 and M_6 in Fig. 10 transforms C_c to a negative capacitance between nodes X and Y. If the gate–drain capacitance of M_5 and M_6 is neglected, the impedance seen looking into the drains is expressed as

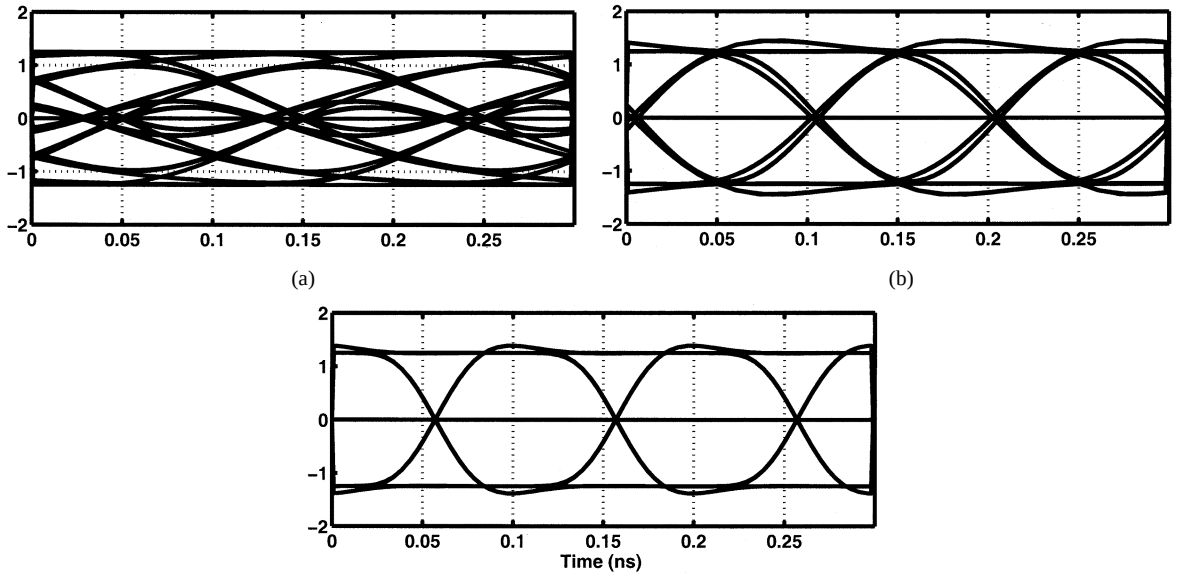
$$Z_{\text{NIC}} = -\frac{1}{sC_c}\frac{g_m + s(C_{gs} + 2C_c)}{g_m - sC_{gs}} \tag{11}$$

or

$$\frac{1}{Z_{\text{NIC}}} = -\frac{1 - sC_{gs}/g_m}{\left(\frac{C_{gs}}{C_c} + 2\right)\frac{1}{g_m} + \frac{1}{sC_c}}. \tag{12}$$

Thus, for frequencies well below the f_T of the transistors, Z_{NIC} is equivalent to a negative capacitance $-C_c$ in series with a negative resistance $-(C_{gs}/C_c + 2)/g_m$.

The upper bound on the value of C_c is that which places the circuit at the edge of relaxation oscillation. For random data, C_c must fall well below this bound to ensure minimal ringing and ISI. In this design, $C_c = 200$ fF, cancelling approximately 30% of the input capacitance of the output stage. The floating capacitor C_c is in fact realized as two nMOS varactors in series,



(a) (b) (c)

Fig. 11. Progressive improvement in driver output. (a) Resistive interface. (b) Inductive and series peaking added. (c) Negative capacitance added.

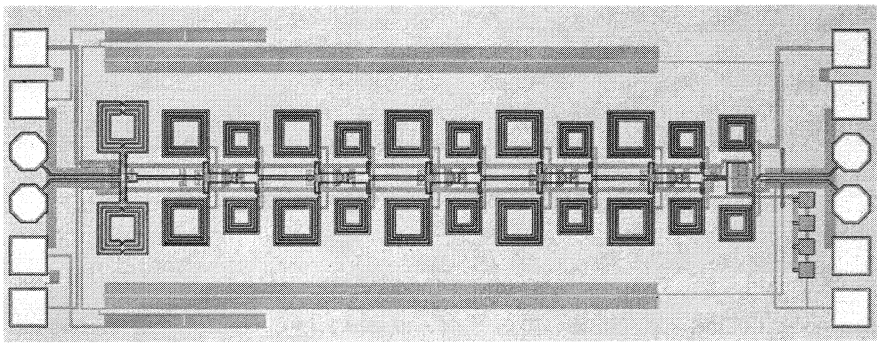
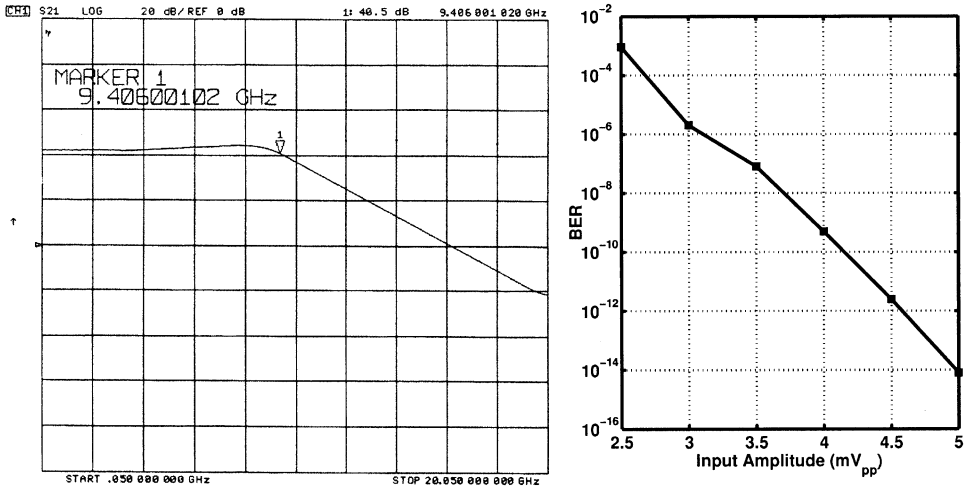


Fig. 12. LA die photo.

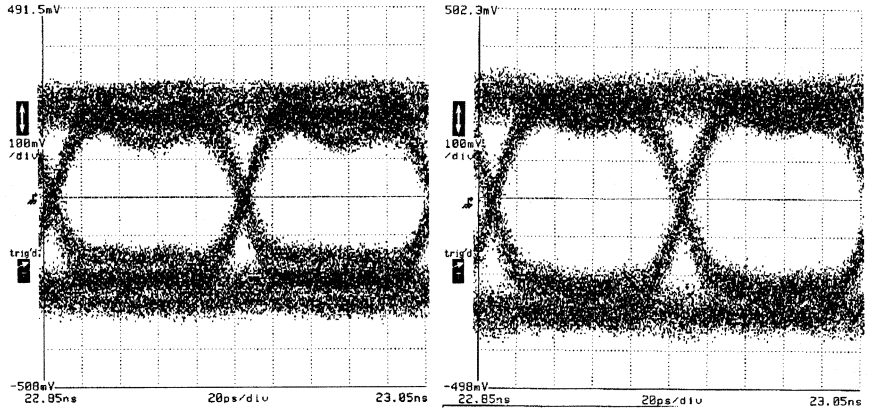


(a) (b)

Fig. 13. LA measured response. (a) Frequency response. (Horizontal scale: $\sim$2 GHz/div., vertical scale: 20 dB/div.) (b) BER versus input signal level.

with their gates tied to the sources of M_5 and M_6. With $I_{ss} = 2.5$ mA, the NIC consumes 7% of the overall driver power.

2) T-Coil and Series Peaking: The low resistance values required at the interface between the predriver and the output stage make T-coil peaking attractive. Even with on-chip spiral T-coils [4], this technique increases the bandwidth by approximately a factor of 2.2. In this design, $R_L = 40\ \Omega$ and the total T-coil inductance is 3 nH.



(a) (b)

Fig. 14. Measured LA output for input level of (a) 5 mV_{pp} and (b) 10 mV_{pp}. (Horizontal scale: 20 ps/div., vertical scale: 100 mV/div.)

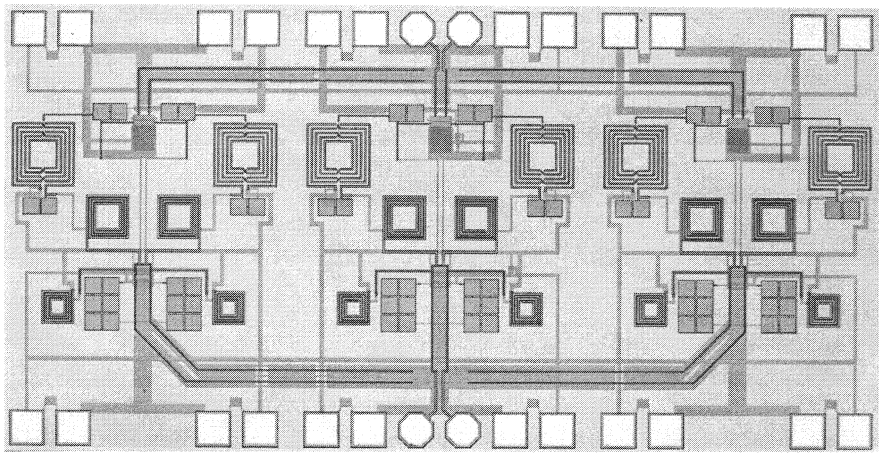


Fig. 15. LMD die photograph.

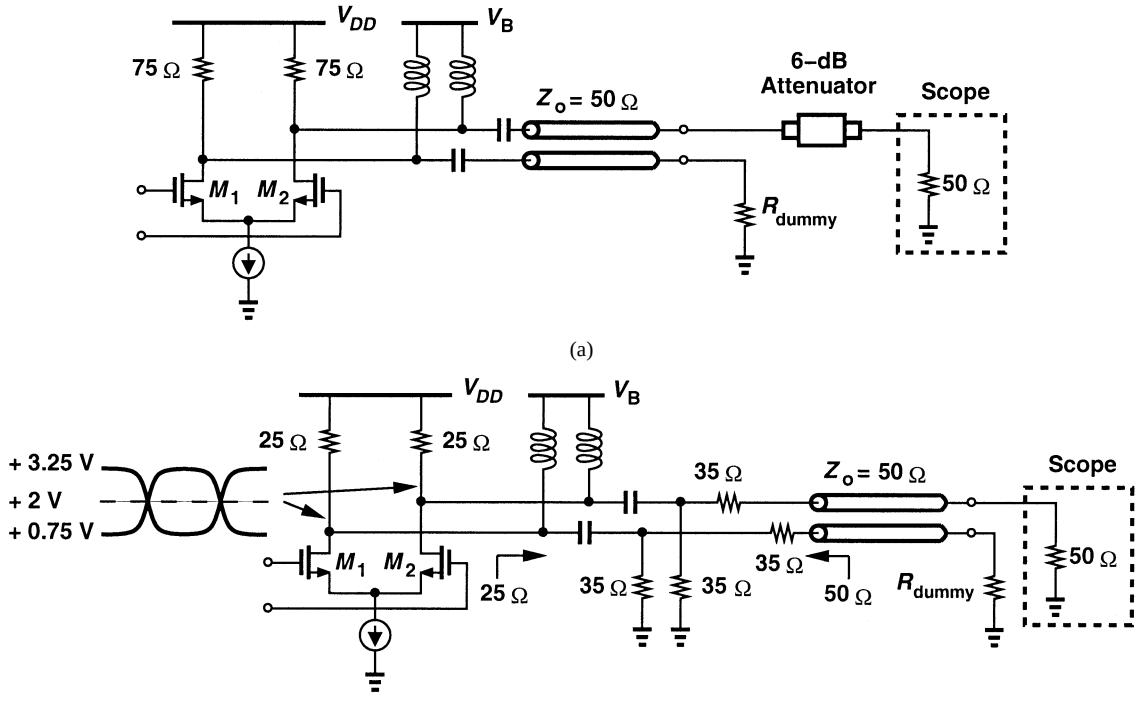
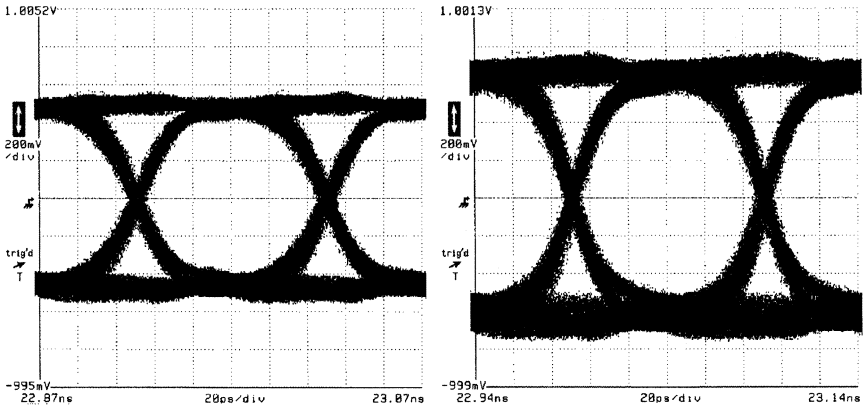


Fig. 16. Test setup for (a) modulator driver and (b) laser driver.



(a) (b)

Fig. 17. Measured eye diagram for (a) modulator driver (attenuated), (b) laser driver (Horizontal scale: 20 ps/div., vertical scale: 200 mV/div.).

TABLE II
LA AND LMD PERFORMANCE SUMMARY

Limiting Amplifier

Parameter	This work	[5]	[10]
Diff. Gain (dB)	50	32	60
BW (GHz)	9.4	3	>15
Sensitivity	4.6 mV_{pp} BER=10^{-12}	2.2 mV_{pp} BER=10^{-12}	3.5 mV_{pp} BER=10^{-9}
Jitter (PP)	9.4 ps	N/A	N/A
Jitter (RMS)	1.6 ps	N/A	N/A
S11, S22	–15 dB (< 10 GHz)	–17 dB (< 3 GHz)	–10 dB (< 10 GHz)
Supply Voltage	1.8 V	2.5 V	3.5 V–5.5 V
Power Dissipation			
Core	100 mW	53 mW	N/A
Buffer	30 mW	N/A	N/A
Total	150 mW	53 mW	600 mW
On–chip Offset Cancellation	Yes	No	No
Die Area (mm^2)	0.5x1.5	0.2x0.15	1.2x2.6
Technology	0.18 μm CMOS	0.25 μm CMOS	SiGe HBT f_T= 47 GHz

Laser/Modulator Driver

Parameter	This work	[3]	[9]
Speed	10 Gb/s	10 Gb/s	10–14 Gb/s
Input Swing	800 mV_{pp}	800 mV_{pp}	560 mV_{pp}
Laser Current	> 100 mA	100 mA	15–60 mA
Modulator Swing	2 V_{pp}	2.5 V_{pp}	3.6 V_{pp}
25 Ω Drive	Yes	Yes	No
Supply Voltage	1.8 V	5.2 V	5.2 V
Power Dissipation			
Core	360 mW	N/A	N/A
Buffer	315 mW	N/A	N/A
Total	675 mW	1.3 W	2.2 W
Die Area (mm^2)	0.9x1.8	N/A	1.2x1.1
Technology	0.18 μm CMOS	0.25 μm GaAs PHEMT	Si Bipolar f_T= 25 GHz

The predriver input transistors M_1 and M_2 are chosen wide enough ($W = 80$ μm) to steer most of the tail current with single-ended input swing of 400 mV_{pp}. The drain junction capacitance of these transistors limits the bandwidth that is broadened by negative capacitance and T-coil techniques. For this reason, inductors L_S are inserted to create series peaking and improve the bandwidth further. In this design, $L_S = 1.75$ nH. Fig. 11 shows the progressive improvement in the driver performance as various techniques are employed. Variation of R_L by $\pm 15\%$ results in an eye closure of 1.5 dB.

V. EXPERIMENTAL RESULTS

The LA and LMD have been fabricated in 0.18-μm CMOS technology and tested in chip-on-board assemblies. The on-chip input and output lines are designed as 50-Ω differential transmission lines to absorb the routing capacitance in an artificial distributed transmission line. These lines are realized using metal-6 on top of a metal-1 ground plane.

A. LA

Shown in Fig. 12 is the die photograph of the LA. The circuit occupies an area of 0.5×1.5 mm^2. Fig. 13(a) plots the frequency response of the LA, indicating a -3-dB bandwidth of 9.4 GHz and an overall differential gain of 50 dB. Fig. 13(b) shows the measured BER as a function of the input signal amplitude for a $10^{23} - 1$ 10-Gb/s pseudorandom bit pattern. The LA exhibits a sensitivity of 4.6 mV_{pp} for BER $= 10^{-12}$.

Fig. 14 depicts the measured output for input levels of 5 and 10 mV_{pp} suggesting that the circuit limits even for a 5-mV_{pp} input.[5]

B. LMD

Fig. 15 shows the die photograph of the LMD, which occupies an area of 0.9×1.8 mm^2. The setups for characterization of the circuit as a modulator driver or a laser driver are shown in Fig. 16(a) and (b), respectively. In both cases, bias-Ts establish a bias voltage of 2 V at the drains of the output transistors. Testing the circuit as a modulator driver is straightforward

[5]Most of the jitter observed in these waveforms arises from the pattern generator and the oscilloscope.

since the driver can interface directly with the external 50-Ω environment [Fig. 16(a)]. A 6-dB attenuator is added to avoid overloading the high-speed oscilloscope.

Tested as a laser driver, the circuit must drive a 25-Ω transmission line followed by a 25-Ω load, making the design of the printed-circuit board difficult. The arrangement in Fig. 16(b) alleviates the problem by presenting a 25-Ω load to the LMD and a 50-Ω source to the transmission line. The additional 35-Ω resistors attenuate the signal delivered to the oscilloscope by 58%. For a maximum peak-to-peak swing of 2.5 V, each drain node reaches a value of 3.25 V while the corresponding gate voltage drops to 1.25 V. Thus, the gate-drain potential difference is stressed by about 200 mV.

The resulting eye diagrams for the LMD are shown in Fig. 17. Table II summarizes the performance of the LA and the LMD along with that of prior work.

VI. Conclusion

This work demonstrates the performance of a limiting amplifier and a laser/modulator driver for 10-Gb/s applications in 0.18-μm CMOS technology. The two prototypes employ various wideband techniques to simultaneously achieve a high gain and a broad bandwidth. These include active feedback, T-coil peaking, and negative capacitance.

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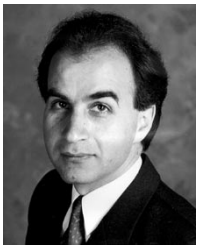

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