Analysis of Phase Noise in Phase/Frequency Detectors

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***Abstract*—The phase noise of phase/frequency detectors can significantly raise the in-band phase noise of frequency synthesizers, corrupting the modulated signal. This paper analyzes the phase noise mechanisms in CMOS phase/frequency detectors and applies the results to two different topologies. It is shown that an octave increase in the input frequency raises the phase noise by 6 dB if flicker noise is dominant and by 3 dB if white noise is dominant. An optimization methodology is also proposed that lowers the phase noise by 4 to 8 dB for a given power consumption. Simulation and analytical results agree to within 3.1 dB for the two topologies at different frequencies.**

***Index Terms*—Flicker noise, inverter phase noise, jitter, oscillator phase noise, PFD, phase/frequency detector, phase noise, PLLs, white noise.**

I. Introduction

THE phase noise of the phase/frequency detector (PFD) in a phase-locked loop (PLL) directly adds to that of the reference, manifesting itself for a high frequency multiplication factor and/or a wide loop bandwidth.

This paper investigates the phase noise mechanisms in PFDs and computes the phase noise spectral density due to both white noise and flicker noise. The results are applied to two PFD topologies, one using static NAND gates and the other employing true single-phase clocking (TSPC). A PFD phase noise simulation technique is also proposed. The objective is to enable the designer to predict the PFD phase noise, and more importantly, design the PFD so as to make its contribution to the overall PLL phase noise negligible.

The paper is organized as follows. Section II describes the background and motivation for this work. Section III builds the foundation by calculating the jitter spectrum of an inverter and Section IV extends the results to a NAND gate. Section V applies these findings to the analysis of two PFD topologies. Section VI discusses the optimization of phase noise for the two PFDs and Section VII presents simulation results.

II. Background

A. Motivation

The in-band multiplication of a PFD's phase noise can create difficulties in RF synthesizer design [1]–[3]. Consider, as an example, a 5-GHz synthesizer targeting IEEE802.11a applications. To negligibly corrupt the 64QAM signal constellation, the synthesizer must achieve an integrated phase noise of roughly 0.5° rms [4].[1] Now, suppose the standard NOR PFD shown in Fig. 1(a) is employed at the input of such a synthesizer with an input frequency of 20 MHz and a loop bandwidth of about 2 MHz. Plotted in Fig. 1(b) is the simulated output phase noise of the synthesizer including only the PFD contribution. Here, the PFD incorporates $(W/L)_{PMOS} = 0.3\ \mu\text{m}/60\ \text{nm}$ and $(W/L)_{NMOS} = 0.2\ \mu\text{m}/60\ \text{nm}$. The area under this plot from 10 kHz to 10 MHz yields an rms jitter of 0.3°, severely tightening the contribution allowed for the voltage-controlled oscillator (VCO).

As another example, consider a 60-GHz transceiver operating with QPSK signals. A synthesizer multiplying the above PFD phase noise to 60 GHz would exhibit an rms jitter of 3.5°. On the other hand, for negligible corruption of QPSK signals, the rms jitter must be less than about 2.1° [4].

The above examples underscore the need for a detailed treatment of phase noise mechanisms in PFDs. Of course, the charge pump may also contribute significant phase noise and merits its own analysis.

B. Observations

Consider the generic PLL shown in Fig. 2. The PFD generates the Up and Down pulses in response to the rising edges on A and B. The noise in the PFD devices modulates the width and edges of the output pulses, creating a random component in the current produced by the charge pump (CP). We neglect the phase noise of all other building blocks and denote the input frequency by f_{in}.

The phase noise in Up and Down translates to random modulation of the time during which I_1 or I_2 is injected into the loop filter. We consider three possible cases. As shown in Fig. 3(a), the phase noise may modulate the widths of Up and Down by the same amount, in which case the CP produces no net output. In the second case [Fig. 3(b)], the phase noise modulates only the position of Up with respect to Down. As explained in Appendix A, this effect is negligible. Lastly, the phase noise may modulate the widths of Up and Down pulses *differently* [Fig. 3(c)], and it is this case that matters most.

The above observations also reveal that, contrary to a designer's first guess, the PFD phase noise of interest is *not* equal to the phase noise of the Up or Down signals themselves. After all, if the widths of Up and Down pulses vary randomly but exactly in unison, then the net current produced by the CP contains no random component. This point raises the question of how exactly the PFD noise must be simulated, which we address in Section VII.

Manuscript received November 16, 2011; revised January 30, 2012; accepted March 03, 2012. Date of publication October 05, 2012; date of current version February 21, 2013. This work was supported by Realtek Semiconductor and MIT Lincoln Laboratory. This paper was recommended by Associate Editor Howard Luong.

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Digital Object Identifier 10.1109/TCSI.2012.2215792

[1]We assume the transmit and receive synthesizers contribute equal but uncorrelated amounts of phase noise.

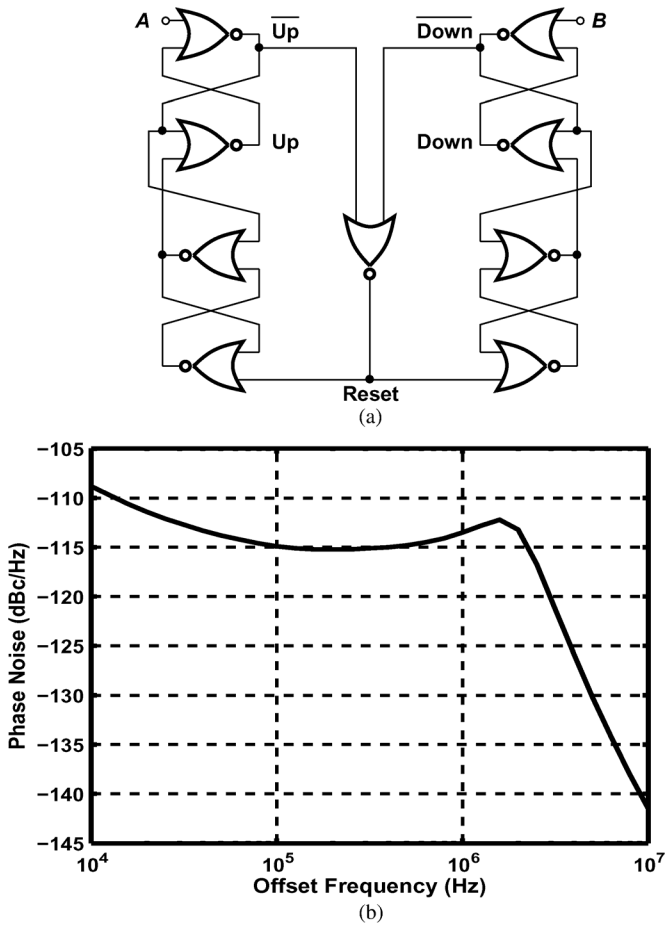

Fig. 1. (a) NOR-based PFD, and (b) output phase noise of a 5-GHz PLL due to PFD.

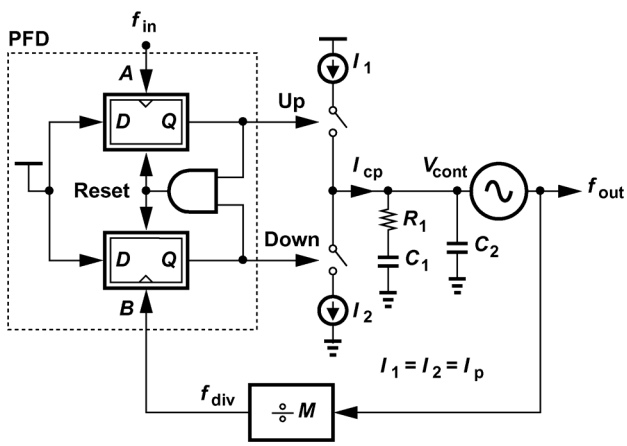

Fig. 2. A PFD in an integer-N PLL.

The foregoing points suggest that the phase noise arising from a PFD in fact relates to the random pulsewidth *difference* between the Up and Down signals, ΔT_{UD}. Moreover, four edges, namely, the rising and falling edges of both Up and Down signals, contribute to ΔT_{UD}. Some of the PFD internal transitions displace Up and Down by the same amount and should be ignored (Section V).

The analysis of PFD phase noise in [5], [6] relates the phase noise to the timing jitter, Δt, as $\Delta\phi_{in} = 2\pi f_s \Delta t$, where f_s denotes the operating frequency, but expresses Δt in terms of the

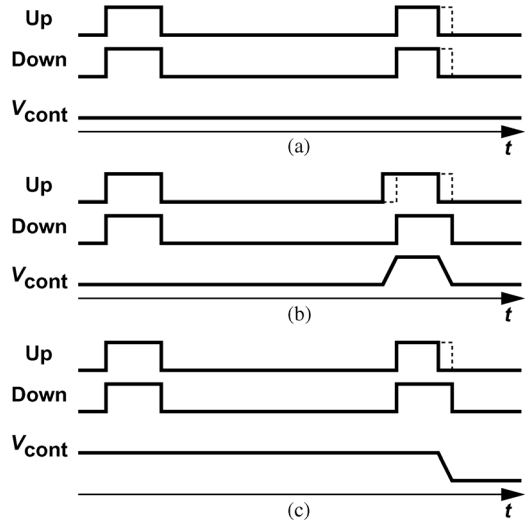

Fig. 3. Modulation of Up and Down (a) width by the same amount, (b) position, and (c) width differently.

(thermal) noise factor and input resistance of the PFD. By contrast, our approach begins with the gates comprising the PFD and determines the jitter in the Up and Down pulsewidth difference, taking into account both flicker and thermal noise. The mismatch between Up and Down currents is neglected here.[2]

III. Phase Noise of CMOS Inverter

A good understanding of the phase noise mechanisms in CMOS inverters proves beneficial in the analysis of PFDs as well. Consider the CMOS inverter and its waveforms shown in Fig. 4. We wish to study the time envelope of the noise produced by M_1 and M_2. These transistors inject thermal and flicker noise to the output node as they turn on. At the end of the transition, however, the on transistor carries no current and produces no flicker noise. Thus, the thermal noise envelope of each transistor lasts about half of the input cycle, T_{in}, whereas its flicker noise envelope pulsates only during transitions [Fig. 4(b)]. Note that in typical PLLs, the transition times within a PFD are much shorter than the input period.

In the analysis that follows, we make numerous approximations based on our intuitive understanding of the circuit's behavior. The soundness of these approximations is ultimately put to test in Section VII, where two completely different PFD realizations are simulated and the results are compared with hand calculations.

It is convenient to view the noise injection of M_1 and M_2 as follows: the transistor that is turning on injects thermal and flicker noise during the transition, and the transistor that is turning off (coming out of the deep triode region) deposits kT/C noise at the output.

A. Noise of Transistor Turning On

In order to formulate the noise contribution by the transistors in Fig. 4, we must examine the circuits' waveforms more closely. As depicted in Fig. 5 for a rising transition at the input and for an inverter with a fanout of about 2, the output begins

[2]Simulations show 0.2 dB higher phase noise due to a 10% mismatch between the Up and Down currents.

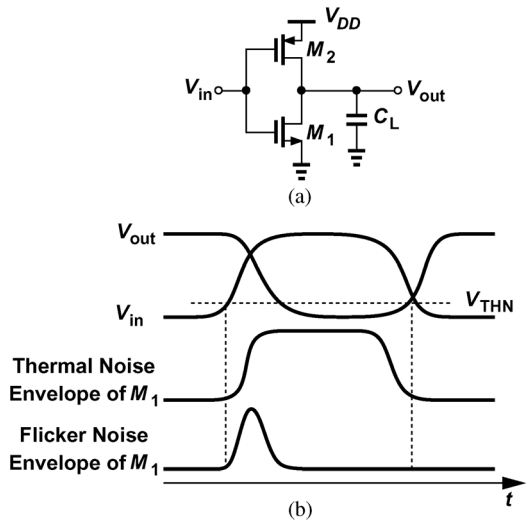

Fig. 4. (a) CMOS inverter, and (b) thermal and flicker noise envelopes of M_1.

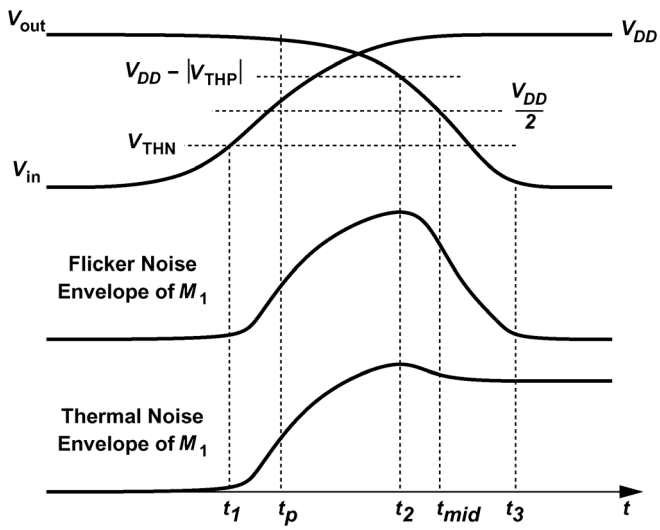

Fig. 5. Detailed view of thermal and flicker noise envelopes during input and output transitions.

to fall only after V_{in} is relatively close to V_{DD}. Transistor M_1 turns on as V_{in} exceeds its threshold, V_{THN}, at $t = t_1$, and injects increasingly larger flicker and thermal noise as V_{in} rises. The noise envelope reaches a maximum before the transistor enters the triode region, around $t = t_2$. Thereafter, the flicker noise injection subsides, falling to zero at $t = t_3$. The thermal noise current, on the other hand, goes from $4kT\gamma g_m$ to a slightly lower value, $4kT/R_{on}$, where R_{on} denotes the channel resistance of M_1 with $V_{GS} = V_{DD}$.

Our next simplifying assumption is that the output phase noise of interest manifests itself while V_{out} in Fig. 5 crosses approximately $V_{DD}/2$ and the noise injected by the transistors after this point is unimportant [7]. Thus, in the waveforms of Fig. 5, we consider the area under the envelopes for only up to $t = t_{mid}$.

We now wish to approximate the area under the noise envelopes by a simple function. As shown in Fig. 6, the flicker noise envelope is approximated by a rectangular waveform of the same height, h, but lasting from the time the actual envelope

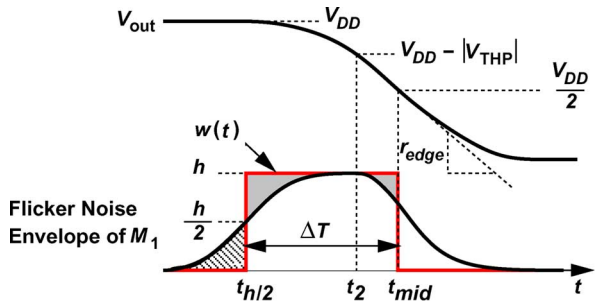

Fig. 6. Rectangular approximation of noise envelope.

reaches half of its height, $t_{h/2}$, to the time V_{out} reaches $V_{DD}/2$, t_{mid}. We expect that the sum of the gray areas is roughly equal to the cross-hatched area. Transient noise simulations in Cadence's Spectre indicate an error of about 4% in this approximation. We apply the same concept to the thermal noise envelope as well. Note that [7] uses a rectangle from the time V_{out} begins to fall (t_p in Fig. 5) to t_{mid}, which, according to simulations, underestimates the integrated noise power by 2 to 3 dB.

Another simplifying assumption can be derived from the waveforms in Fig. 5: at the peak of the noise envelope, one transistor is nearly off. Thus, we consider only the noise of M_1 on the falling edges at the output and only the noise of M_2 on the rising edges.

Based on the foregoing approximations and utilizing the rectangular function, $w(t)$, in Fig. 6, we now outline the inverter phase noise analysis as follows. As shown in Fig. 7(a), the noise current of each transistor, $i_n(t)$ is equivalently multiplied by shifted versions of $w(t)$. Each product is integrated for a duration of $\Delta T = t_{mid} - t_{h/2}$ and divided by the load capacitance, C_L, yielding the noise voltage [Fig. 7(b)]. These voltages are then divided by the slew rate, r_{edge} (Fig. 6), to give the time displacement (jitter), sampled, and summed. We write the noise voltage, $v_{n,1}$, after the first window as

$$v_{n,1} = \frac{1}{C_L}\int_0^{\Delta T} i_n(t)dt = \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(t)dt. \quad (1)$$

Note that the load capacitance is assumed constant and equal to its value at $V_{out} = V_{DD}/2$. Also, the integration tacitly neglects the effect of the inverter's output resistance, r_O. This approximation is justified because the time constant, $r_O C_L$, at the inverter output is much greater than ΔT. Similarly,

$$v_{n,m} = \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(t - mT_{in})dt. \quad (2)$$

The particular shape of $w(t)$ allows this equation to be rewritten as

$$v_{n,m} = \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(mT_{in} - t)dt, \quad (3)$$

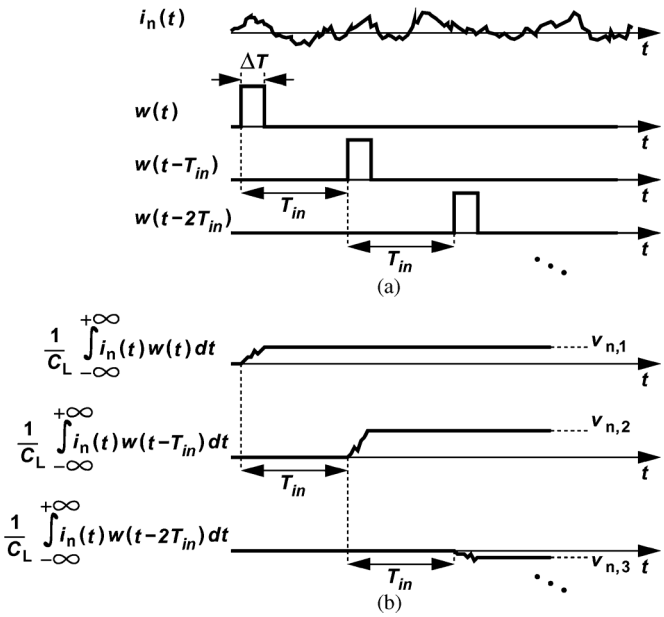

Fig. 7. (a) Equivalent operation of inverter on noise of one transistor, and (b) conversion of noise current to noise voltage.

which is the convolution integral [7]. The noise voltage spectrum is therefore given by

$$S_{Vn}(f) = \frac{1}{C_L^2} |W(f)|^2 S_{In}(f), \tag{4}$$

where $W(f)$ denotes the Fourier transform of $w(t)$ and $S_{In}(f)$ the spectrum of $i_n(t)$. As shown in Appendix B, the phase noise spectrum[3] due to noise of NMOS transistor on the falling edges is equal to

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} \sum_{m=-\infty}^{m=+\infty} S_{Vn}\left(f - \frac{m}{T_{in}}\right). \tag{5}$$

It is important to recognize two differences between the above analysis and that in [7]: (1) as mentioned earlier, our window definition (from $t_{h/2}$ to t_{mid}) more accurately predicts the injected noise power, and (2) the sampling phenomenon reveals aliasing even for flicker noise if the $1/f$ corner, f_{cor}, is comparable with the operation frequency, which may be the case for PFDs.

We now simplify (5) if $\overline{I_n^2}$ is white. As shown in Appendix C, $S_\Phi(f)$ is also white and equal to

$$\begin{aligned} S_\Phi(f) &= \frac{\pi^2}{r_{edge}^2 T_{in}^2} \frac{1}{C_L^2} \frac{\Delta T}{f_{in}} S_I(f) \\ &= \frac{\pi^2}{r_{edge}^2 C_L^2} \frac{\Delta T}{T_{in}} S_I(f). \end{aligned} \tag{6}$$

In this expression, the load capacitance appears in both $r_{edge}(= I_D/C_L$, where I_D is the drain current of the on transistor as V_{out} crosses $V_{DD}/2)$ and in ΔT. Thus, $S_\Phi(f)$ is *directly* proportional to C_L and f_{in}. The output phase noise due to white noise therefore rises by 3 dB for each doubling of the operation frequency.

The flicker noise behavior of the inverter can also be deduced from (5). If f_{in} is well above the flicker noise corner frequency, no aliasing occurs and (5) is simplified by choosing $m = 0$:

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} S_{Vn}(f). \tag{7}$$

Since ΔT is much less than $1/f_{cor}$, we can assume $W(f) = \Delta T^2 \mathrm{sinc}^2(\pi f \Delta T)$ is relatively constant for the frequency range of interest and equal to ΔT^2. It follows that

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} \frac{\Delta T^2}{C_L^2} S_{1/f}(f), \tag{8}$$

where $S_{1/f}(f)$ denotes the noise current spectral density of the on transistor due to its $1/f$ noise. In this case, the phase noise rises by 6 dB for each doubling of f_{in}. It also exhibits a stronger dependence upon ΔT. As mentioned earlier, (6) and (8) are evaluated for M_1 on the falling edge at the output and for M_2 on the rising edge. Note that [7] does not analyze the effect of flicker noise in CMOS inverters.

B. Noise of Transistor Turning Off

As illustrated in Fig. 5, when the noise envelope reaches its peak, one transistor is near the edge of the triode region and the other is almost off. Before turning off, however, this transistor has acted as a resistor, producing noise across C_L. Turning off once every T_{in} seconds, the NMOS transistor deposits a noise voltage whose spectral density is given by $(kT/C_L)/f_{in}$. As shown in Appendix B, the falling edges exhibit a phase noise equal to

$$S_1(f) = \frac{\pi^2}{T_{in}^2} \frac{1}{r_{edge}^2} \frac{kT}{C_L f_{in}}. \tag{9}$$

Taking the PMOS contribution into account, we obtain the total kT/C-induced phase noise as

$$S_\Phi(f) = \frac{2\pi^2}{T_{in}^2} \frac{1}{r_{edge}^2} \frac{kT}{C_L f_{in}}. \tag{10}$$

C. Total Phase Noise

The total phase noise is given by the sum of five terms: (6) and (8) evaluated for both NMOS and PMOS transistors, and (10):

$$\begin{aligned} S_\Phi(f) = &\left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} \left[\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f) \right] \right\}_{NMOS} \\ &+ \left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} \left[\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f) \right] \right\}_{PMOS} \\ &+ \frac{2\pi^2 f_{in}}{r_{edge}^2} \frac{kT}{C_L}. \end{aligned} \tag{11}$$

IV. Phase Noise of CMOS NAND Gate

The inverter phase noise analysis can be readily extended to other CMOS gates as well. We briefly consider here the noise

[3]Throughout this paper, all the spectra are two-sided, and the phase noise is denoted by $S_\Phi(f)$.

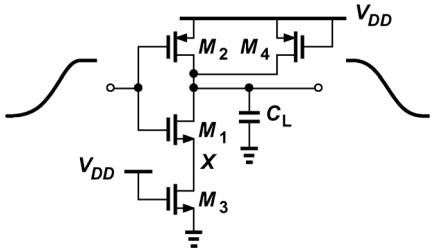

Fig. 8. NAND gate with one input changing.

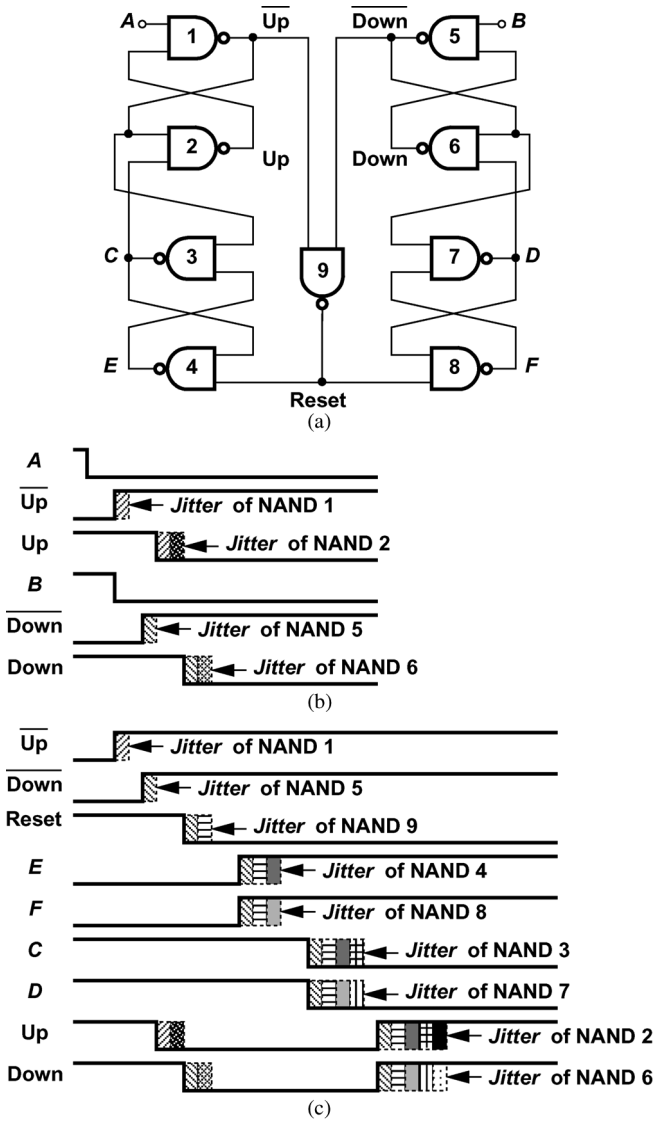

Fig. 9. (a) NAND-based PFD, (b) jitter contributions to falling edges of outputs, and (c) jitter contributions to rising edges of outputs.

behavior of a static NAND gate and use the results in Section V to study a NAND-based PFD.

Since in a PFD environment, the two inputs do not change simultaneously, we can reduce the gate to an inverter for each transition. Such an inverter incurs an additional capacitance at the output due to the second PMOS transistor, and its output falling edge is produced by the series combination of two NMOS transistors (Fig. 8).

In our PFD design, M_1 and M_3 have the same width and minimum length; thus, they can be replaced with one NMOS device having twice their length.[4] In other words, (11) holds if $r_{edge}, \Delta T, C_L$ and $S_{In}(f)$ are modified to reflect the equivalent values in the NAND circuit.

V. PFD Phase Noise Analysis

A. NAND PFD

As suggested by the factors ΔT in (6) and ΔT^2 in (8), the phase noise rises in proportion to the turn-on time of the transistors in each gate. A worthy effort in PFD design, therefore, is to minimize the rise and fall times. We thus modify the standard NOR-based PFD to the NAND-based topology shown in Fig. 9(a). Note that this circuit responds to the *falling* edges of A and B, and its Up and Down outputs are *low* when asserted.

We must now examine the propagation of the edges through the PFD circuit, seeking those whose jitter modulates the pulsewidth *difference* between the Up and Down pulses. To this end, we draw a detailed timing diagram, mark with a certain shade or pattern the jitter contributed by each gate to each transition, carry the jitters on to the final Up and Down pulses, and omit those that are in common.

Fig. 9(b) shows the timing diagram, assuming input A falls earlier than input B. NAND 1 adds jitter to the falling edge of A, producing a rising edge on $\overline{\text{Up}}$. This edge experiences additional jitter in NAND 2 and generates the falling edge of Up. That is, each falling edge of Up is corrupted by only the jitters of NANDs 1 and 2. Similarly, when a falling edge of B follows, $\overline{\text{Down}}$ rises with NAND 5's jitter and Down falls with both NAND 5's and NAND 6's jitters.

We must also follow the $\overline{\text{Up}}$ and $\overline{\text{Down}}$ rising edges through the reset path. As illustrated in Fig. 9(c), after $\overline{\text{Down}}$ goes up, Reset falls, inheriting the jitters of NAND 5 and NAND 9. In response, E and F rise, incurring additional jitter from NAND 4 and NAND 8, respectively. Subsequently, C falls with the jitter of NAND 3 and D with that of NAND 7. Finally, Up and Down rise with the jitters of NAND 2 and NAND 6, respectively.

The Up and Down waveforms in Fig. 9(c) merit two remarks. First, NAND 2 contributes jitter to both the rising and falling edges of Up, but the two jitters are uncorrelated because the former is due to a PMOS device and the latter due to an NMOS device (the series combination of M_1 and M_3 in Fig. 8). A similar observation applies to NAND 6 contributions to Down. Second, the jitter produced by NAND 9 appears on the rising edges of both Up and Down pulses and hence is immaterial. As seen from Fig. 9(c), NANDs 1–8 make a total of 10 contributions to the pulsewidth difference between Up and Down. The phase noise spectral densities of these contributions are summed to obtain the overall PFD phase noise.

In response to the jitter components in the Up and Down pulses (except for those that are in common), the charge pump in Fig. 2 produces an error current, ΔI. Adding up the powers of uncommon jitters, T_m, $m = 1, \ldots, 10$, in the Up and Down pulses, we have

$$\overline{\Delta I^2} = \frac{I_p^2}{T_{in}^2} \sum_{m=1}^{10} T_m^2. \tag{12}$$

[4]The drain and source capacitance at node X introduce a negligible error in this equivalency.

It can be shown that the transfer function from this current injection to the PLL output within the loop bandwidth is equal to $\Phi_{out,PLL}/\Delta I = (2\pi/I_p)M$. It follows that

$$S_{\Phi,PLL}(f) = \frac{4\pi^2}{T_{in}^2} M^2 \sum_{m=1}^{10} S_{Tm}(f), \tag{13}$$

where $S_{Tm}(f)$ denotes the spectral density of jitter component T_m and is equal to $S_{Vn}(f)/r_{edge}^2$. For roughly similar gates and rise and fall times, the in-band phase noise observed at the PLL output is given by

$$S_{\Phi,PLL} \cong 10M^2 \left[\frac{4\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f) + \frac{4\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) + \frac{4\pi^2 f_{in}}{r_{edge}^2} \frac{kT}{C_L} \right]. \tag{14}$$

As explained in Section VI, however, an optimum design may incorporate different sizings for the gates.

An important point emerging from our analysis is that, to reduce the flicker noise of a PFD, the channel length of its constituent transistors must *not* be increased. This is because longer-channel devices inevitably raise ΔT in (14). Instead, the channel area of the transistors can be increased by choosing *wider* devices.

B. TSPC PFD

The foregoing analysis can be applied to other PFD topologies as well. In this section, we study the phase noise of a TSPC implementation [8] as it can potentially achieve a higher speed and proves useful in cascaded PLLs. Depicted in Fig. 10(a), the circuit operates as follows. A rising edge on A turns on M_5, discharging the Up output. Similarly, a rising edge on B discharges the Down output. Once both Up and Down are low, Reset rises, discharging nodes C and D and forcing Up and Down to go high.

In a manner similar to the analysis of the NAND PFD, we follow the transitions through the circuit and mark the jitter contributed by each stage. As illustrated in Fig. 10(b), the falling edges of Up and Down are corrupted by the noise of the series combinations $M_5 - M_6$ and $M_{11} - M_{12}$, respectively. Next, Reset experiences the jitter due to $M_{11} - M_{12}$ and the NOR gate. The falling transitions at C and D inherit the jitter of Reset and incur additional noise due to M_3 and M_9, respectively. Finally, these edges are corrupted by the noise of M_4 and M_{10}.

Let us draw several conclusions. First, the jitter of the NOR gate modulates the widths of Up and Down equally and hence is ignored. Second, the overall TSPC PFD phase noise arises from six transitions and can be potentially smaller than that of the NAND PFD. Third, the noise injection mechanisms in each stage are similar to those of the inverter and NAND gates studied earlier. For example, when M_5 turns on, its corresponding stage acts approximately like a NAND gate (except that M_4 has been off well before this transition). Also, when node C falls, the series combination $M_5 - M_6$ deposits kT/C noise at the output while M_4 turns on as in an inverter and injects both thermal and flicker noise. Thus, (14) applies here as well if the factor of 10 is replaced by 6 and the gates and rise and fall times are assumed similar.

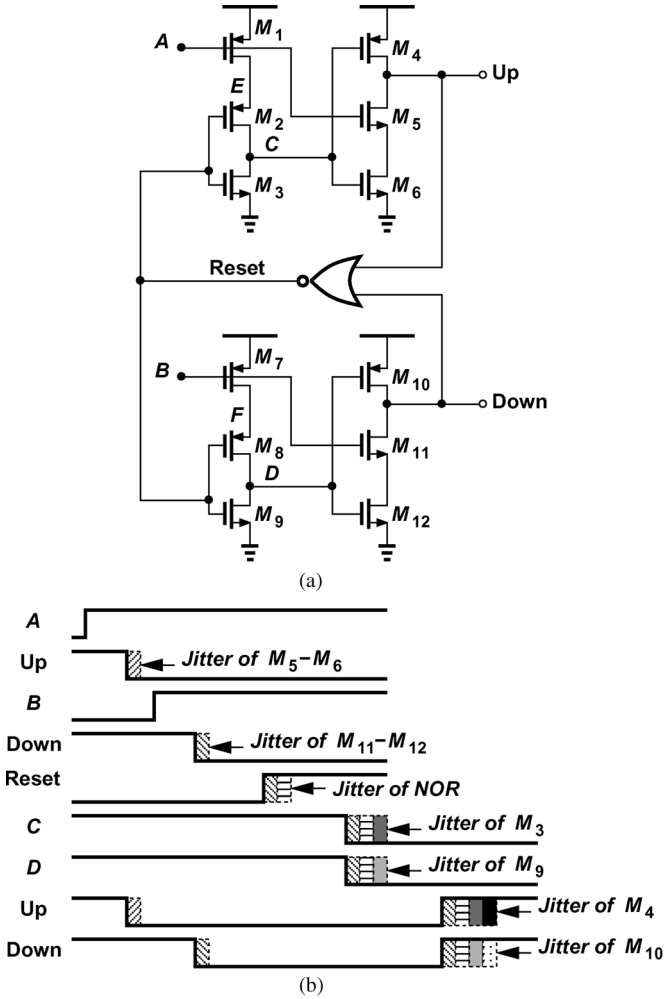

Fig. 10. (a) TSPC PFD, and (b) jitter contributions to the outputs.

VI. Design Optimization

With the insights developed above into PFD phase noise mechanisms, we now seek to optimize each design for minimum phase noise. Of course, one can simply enlarge the widths of all of the PFD transistors by a factor of α so as to reduce the phase noise by the same factor, but at the cost of proportionally higher power consumption. A more methodical approach, however, is to assume a certain power budget and determine the best sizing of the transistors that yields minimum phase noise. This optimization can still be followed by the above scaling technique to trade power for phase noise. We consider $1/f$ noise here as it dominates for offsets as high as 10 MHz, but optimization for thermal noise is similar.

Since the PFD power dissipation is proportional to the total transistor width in the signal path, W_{tot}, we must determine how a given W_{tot} is apportioned among the transistors so as to minimize the phase noise. Our general procedure is to favor transistors that define the transition time of critical edges. We also make four approximations: (1) The capacitance at a given node is proportional to the width of the "driver" transistor, W_a, and the width of the "driven" transistor, W_b: $C_L \propto \eta W_a + W_b$. The first term on the right accounts

for the drain junction capacitance and the Miller multiplication of the gate-drain overlap capacitance at the output node (about a factor of 2). (2) The drain $1/f$ noise current spectrum is given by $S_{1/f}(f) = g_m^2 K_f/(W_a L_a C_{ox} f)$, where $g_m \approx I_D/(V_{GS} - V_{TH})$ and $V_{GS} = V_{DD}$.[5] (3) At the point of interest, namely, $V_{GS} \approx V_{DD}$ and $V_{out} \approx V_{DD}/2$, we have $I_D \propto W_a$ regardless of the transistor (short-channel) characteristics. Thus, the slew rate in (8), $r_{edge} \propto I_D/C_L \propto W_a/C_L$. (4) The window width, ΔT, is proportional to $V_{DD}/r_{edge} \approx V_{DD}C_L/I_D$. Equation (8) is now rewritten as

$$S_\Phi(f) \propto \frac{f_{in}^2 V_{DD}^2 C_L^2}{W_a^3}\frac{1}{f}. \tag{15}$$

For given values of f_{in}, V_{DD}, and f,

$$S_\Phi(f) \propto \frac{(\eta W_a + W_b)^2}{W_a^3}. \tag{16}$$

The power consumed to charge and discharge such a node once per cycle is approximately equal to $P = f_{in}C_L V_{DD}^2$. We now apply these results to the optimization of the NAND and TSPC PFDs.

A. NAND PFD Optimization

As evident from Figs. 9(b) and (c), the NAND PFD phase noise arises from five transistors: the PMOS device in NAND 1, the NMOS device in NAND 2, the PMOS device in NAND 4, the NMOS device in NAND 3, and the PMOS device in NAND 2. Denoting the widths of PMOS and NMOS transistors in NAND j by W_{Pj} and W_{Nj}, respectively, we use (16) to express the first PMOS contribution as:

$$S_{\Phi_1}(f) \propto \frac{[\eta(2W_{P1} + W_{N1}) + W_2 + W_3 + W_9]^2}{W_{P1}^3}. \tag{17}$$

Here, the factor of 2 accounts for the two PMOS devices tied to the output and $W_j = W_{Pj} + W_{Nj}$. The sum $W_2 + W_3 + W_9$ represents the load due to the three NANDs driven by NAND 1. The other four contributions can be expressed in a similar manner, e.g., for the NMOS device in NAND 2:

$$S_{\Phi_2}(f) \propto \frac{[\eta(2W_{P2} + W_{N2}) + W_{P1} + W_{N1}]^2}{W_{N2}^3}. \tag{18}$$

Note that the proportionality factors relating the right-hand sides of (17) and (18) to their left-hand side are different as they include the mobility and flicker noise coefficient of PMOS and NMOS devices, respectively. The total power consumption satisfies the relation:

$$P \propto f_{in}V_{DD}^2\left[W_{P9} + W_{N9} + 2\sum_{j=1}^{4}(W_{Pj} + W_{Nj})\right]. \tag{19}$$

As explained in Section V, the jitter of some of the edges does not enter the overall PFD phase noise. The transistors causing these edges can therefore have nearly minimum widths so long as they respond fast enough to avoid circuit failure. The devices falling into this category are the NFETs in NANDs 1, 4, and 9 and the PFETs in NANDs 3 and 9. The sum of the five phase noise contributions described above must be minimized subject to the power budget imposed by (19). This is accomplished using the "fmincon" function in MATLAB. For example, a total width of 162 μm (corresponding to 0.24 mW at 1 GHz) for the transistors yields $W_{P1} = 11$, $W_{N1} = 0.12$, $W_{P2} = 9.1$, $W_{N2} = 5.9$, $W_{P3} = 0.12$, $W_{N3} = 6.22$, $W_{P4} = 7.8$, $W_{N4} = 0.12$, $W_{P9} = 0.12$, $W_{N9} = 0.12$, all in microns. Using transient circuit simulations, we adjust some of the noncritical transistors widths so to minimize crowbar currents and speed up the critical transitions, obtaining $W_{P1} = 10.6$, $W_{N1} = 0.5$, $W_{P2} = 8.5$, $W_{N2} = 5.5$, $W_{P3} = 0.6$, $W_{N3} = 5.84$, $W_{P4} = 7.4$, $W_{N4} = 0.5$, $W_{P9} = 0.12$, $W_{N9} = 2$, all in microns. It is interesting that such a range of widths would not be obvious if we attempted to manually optimize the PFD transistors by trial and error. As shown in Section VII, this optimization lowers the phase noise by 4 to 6 dB.

B. TSPC PFD Optimization

The foregoing procedure can be applied to the TSPC PFD of Fig. 10(a) as well. Here the phase noise has three contributions arising from $1/f$ noise:

$$S_{\Phi_1}(f) \propto \frac{[\eta(W_4 + W_5) + W_{P,NOR} + W_{N,NOR}]^2}{W_5^3}, \tag{20}$$

where W_j refers to the width of M_j and $W_{P,NOR}$ and $W_{N,NOR}$ are the PMOS and NMOS widths in the NOR gate, respectively. The power consumption satisfies the relation:

$$P \propto f_{in}V_{DD}^2\left(2\sum_{j=1}^{6} W_j + W_{P,NOR} + W_{N,NOR}\right). \tag{21}$$

For simplicity, we assume equal widths for the transistors within each cascode structure. Also, $M_1 - M_2$ and $M_7 - M_8$ in Fig. 10(a) contribute no jitter to the PFD and hence can have small widths. For example, a total width of 162 μm (corresponding to 0.2 mW at 1 GHz) is apportioned as follows: $W_1 = 0.12$, $W_2 = 0.12$, $W_3 = 28$, $W_4 = 25$, $W_5 = 13.72$, $W_6 = 13.72$, $W_{P,NOR} = 0.12$, $W_{N,NOR} = 0.12$, all in microns. Manual adjustment to improve transition times in the simulations yields $W_1 = 1.4$, $W_2 = 1.4$, $W_3 = 12$, $W_4 = 24$, $W_5 = 10$, $W_6 = 10$, $W_{P,NOR} = 10$, $W_{N,NOR} = 0.12$, all in microns. As discussed in Section VII, this optimization reduces the phase noise by 5 to 8 dB.

C. Dependence on Operation Frequency

Equation (14) reveals that the phase noise of PFDs rises in proportion to f_{in} in the thermal regime and f_{in}^2 in the flicker noise regime. This dependence imposes certain bounds on the in-band phase noise of PLLs. For a feedback divide ratio of M, the first term in (14) yields an output phase noise of

$$S_{\Phi,out}(f) \propto f_{in}M^2 S_I(f) \propto \frac{f_{out}^2}{f_{in}}S_I(f). \tag{22}$$

[5]This g_m equation assumes heavy velocity saturation. For long-channel devices, $g_m \approx 2I_D/(V_{GS} - V_{TH})$. This distinction is not critical in our analysis.

That is, to minimize the phase noise due to the PFD thermal noise, f_{in} must be maximized. For PFD flicker noise, on the other hand,

$$S_{\Phi,out}(f) \propto f_{in}^2 M^2 S_{1/f}(f) \propto f_{out}^2 S_{1/f}(f). \quad (23)$$

Interestingly, this PFD contribution is independent of the input frequency so long as flicker noise does not experience aliasing.

VII. Simulation Results

This section presents simulation results in 65-nm CMOS technology for the circuits studied in this paper and compares them with our analytical derivations. The objective is threefold: (a) validate the trends predicted by our analysis, e.g., the dependence of phase noise upon the input frequency and node capacitance, (b) check the absolute accuracy of the analytical results, and (c) examine the soundness of our optimization procedure.

A few remarks with respect to the hand calculations are warranted. First, the transistor capacitances, drain bias currents, and drain (1/f and thermal) noise currents are obtained from ac and transient simulations for various values of V_{GS} and V_{DS}. These simulations also reveal the peak noise current and the gate-source voltage, $V_{GS,half}$, at which the noise current is equal to half of its peak. Second, the window width, ΔT, in (6), (8), (11) and (14) is derived from transient simulations of the stage of interest by finding the time at which the gate-source voltage reaches $V_{GS,half}$.

A. Inverter and NAND Simulations

Fig. 11 plots the phase noise of a chain of eight inverters with $W_P = 6\ \mu\text{m}$ and $W_N = 3\ \mu\text{m}$ at an input frequency of 1 GHz. (As explained in Section VII-B, scaling to other frequencies is straightforward.) In order to investigate the robustness of our analytical approach, the chain is also studied with an additional node capacitance of 20 fF. In each case, the results of Cadence pnoise simulations are compared with those of hand calculations. Fig. 12 repeats these experiments for a chain of eight NAND gates with one input tied to V_{DD} and $W_P = W_N = 6\ \mu\text{m}$. We observe that in all cases, the hand calculations incur an error of less than 2 dB.

B. PFD Simulations

As argued in Section II, the PFD phase noise cannot be simulated by examining only the Up or Down pulses. For this reason, we embed the PFD within an otherwise ideal PLL, run a pss and pnoise analysis, allow the PLL to settle, and compute the output phase noise of the PLL in the steady state. If the PLL bandwidth is large enough, the PFD phase noise up to the offset frequencies of interest passes to the output unattenuated. Such a simulation takes a long time but is necessary here to demonstrate the validity of our approach. The PLL comprises behavioral descriptions of the VCO, frequency divider, and charge pump. The loop filter employs a noiseless resistor. To ensure that the PLL does not attenuate the PFD phase noise for offset

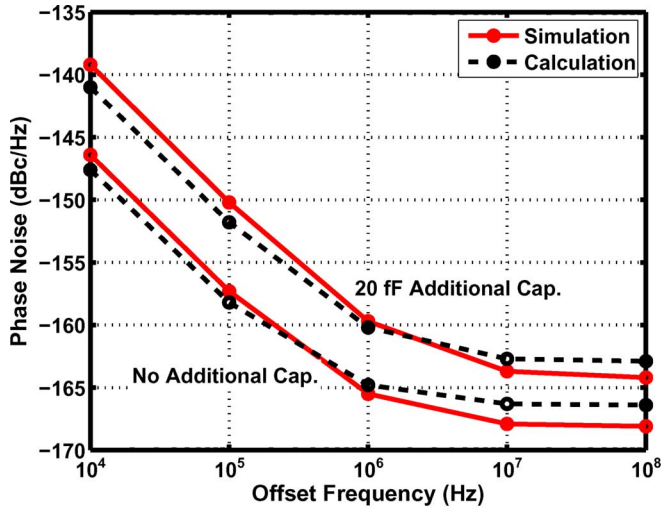

Fig. 11. Phase noise of a chain of eight inverters running at 1 GHz.

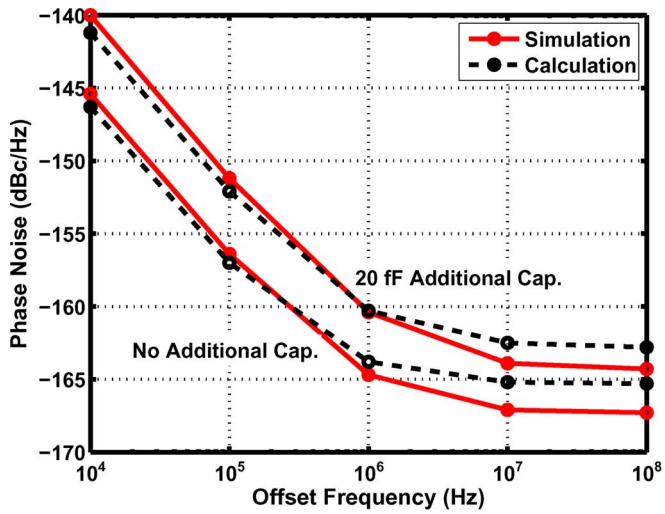

Fig. 12. Phase noise of a chain of eight NANDs running at 1 GHz (with one input tied to V_{DD}).

frequencies as high as 100 MHz, the reference frequency, f_{ref}, is chosen equal to or greater than 1 GHz. Such a high value is chosen so as to readily observe and validate the effect of flicker noise. For much lower input frequencies, the aliasing of white noise tends to mask the effect of flicker noise, making it difficult to correlate the simulations with the analytical results. For example, if f_{ref} is reduced to 20 MHz, then the effect of flicker noise rises by $10\log(50) = 17$ dB and that of white noise by $20\log(50) = 34$ dB, masking the former.

Fig. 13 plots the simulated and calculated phase noise of the NAND PFD for different input frequencies. (Each simulation incorporates a different set of PLL parameters[6] commensurate with the reference frequency.) As predicted in Section III, doubling f_{ref} raises the phase noise by 6 dB in the 1/f noise regime and by 3 dB in the white noise regime. The error in the analytical calculations is 3.1 dB. The effect of white noise is overestimated possibly due to assuming that all of the high-frequency noise components experience only a sinc^2 envelope before folding,

[6]For example, $R_1 = 600\ \Omega$, $C_1 = 200$ pF, $C_2 = 100$ fF, $I_p = 1$ mA, $M = 1$, and $K_{VCO} = 2\pi(1.5 \times 10^9)$ rad/s.

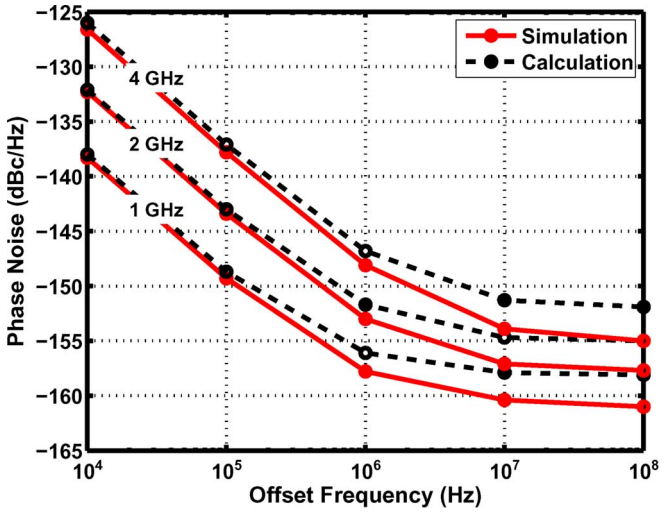

Fig. 13. Phase noise of NAND PFD at various input frequencies.

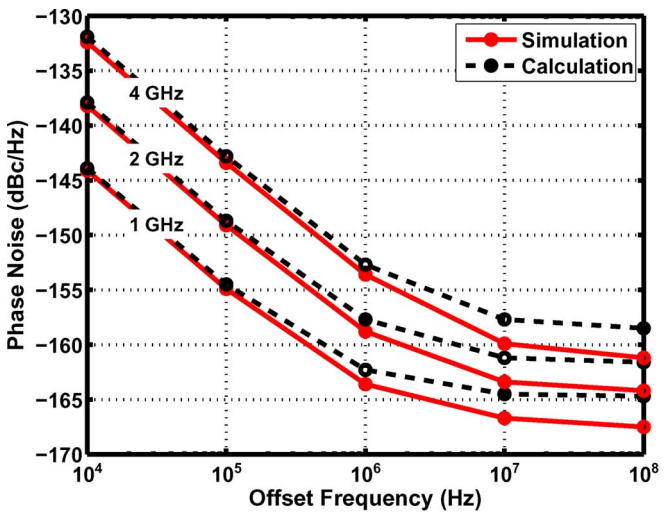

Fig. 14. Phase noise of TSPC PFD at various input frequencies.

whereas in the actual circuit, these components are also attenuated by the finite bandwidth and hence do not extend to infinity.

Fig. 14 plots similar results for the TSPC PFD. The maximum error in this case is 2.8 dB. Designed for the same power consumption as the NAND PFD, the TSPC topology exhibits about 6 dB lower phase noise.

Illustrated in Fig. 15 are the results of the optimization procedure described in Section VI. For a given power consumption, the phase noise is reduced by 4 to 8 dB for the two PFDs.

VIII. Conclusion

The phase noise of PFDs can manifest itself within the bandwidth of PLLs, corrupting the transmitted and received signal constellations. This paper analyzes the phase noise of two PFD topologies based on the approximations made for a CMOS inverter. It is also shown that the PFD phase noise is not merely that of the Up and Down pulses. Simulations using each PFD in a PLL reveal good agreement with analytical predictions, indicating, most notably, the dependence of the phase noise on the frequency of operation.

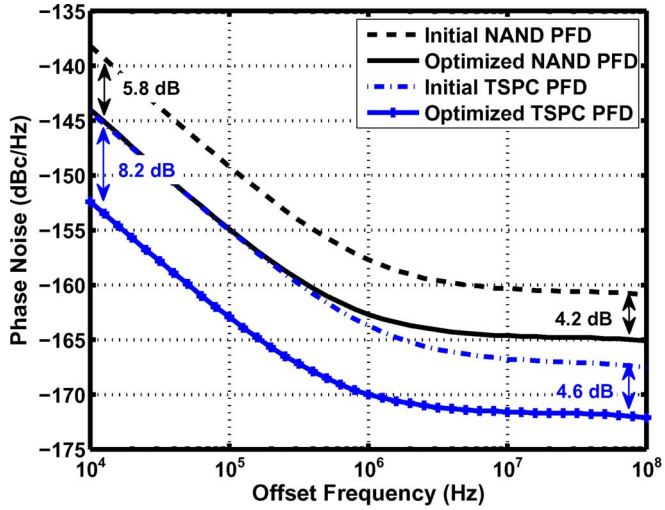

Fig. 15. Phase noise of NAND and TSPC PFDs before and after optimization.

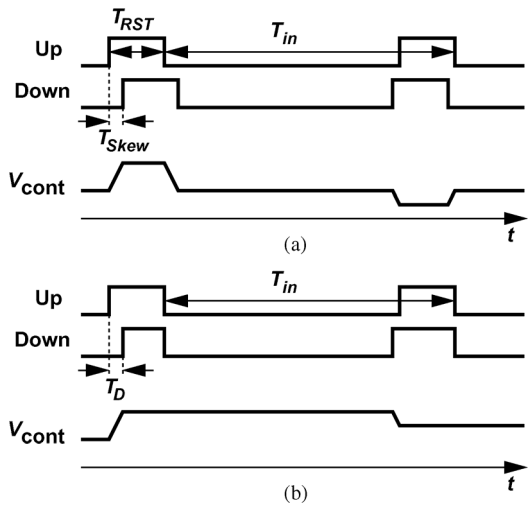

Fig. 16. Modulation of (a) position, and (b) pulsewidth of Up and Down signals.

Appendix A
Effect of Pulse Position Modulation

In this appendix, we show that if noise modulates only the position of the Up or Down pulses, the resulting phase noise is negligible. Consider the waveforms depicted in Fig. 16(a), where Up and Down have a pulsewidth of T_{RST} and a random skew of T_{skew}. Assuming an ideal charge pump, we note that the disturbance on the oscillator control voltage is in the form of a pulse with a mean width of T_{RST}. By contrast, as shown in Fig. 16(b), a pulsewidth difference of T_D between Up and Down manifests itself as a step on the control voltage, producing a much larger phase disturbance.

Appendix B
Phase Noise of Square Wave With Uncorrelated Jitters on Rising and Falling Edges

It is usually assumed that an edge displacement of ΔT translates to a phase change of $2\pi\Delta T/T_{in}$, where $T_{in} = 1/f_{in}$ denotes the period. Of course, if *all* of the edges of a square wave are displaced by ΔT, this amount of phase change arises. However, jitter affects the consecutive edges differently, requiring a closer look at the resulting phase noise.

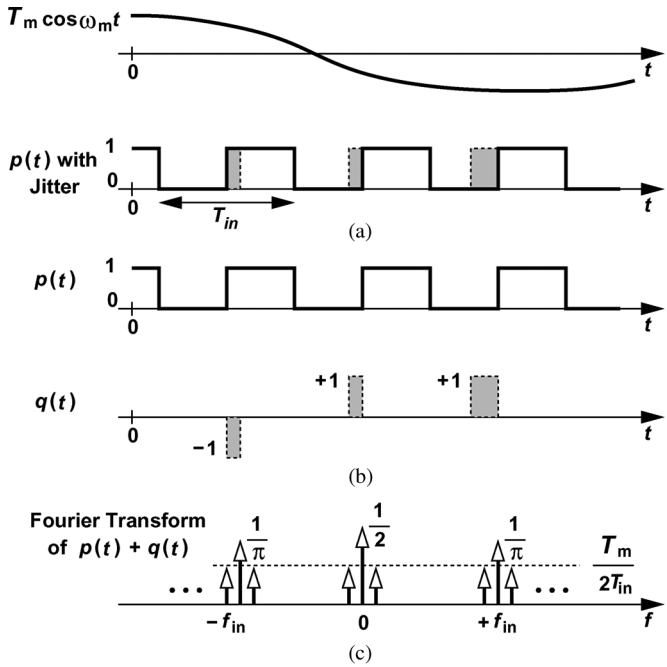

Fig. 17. (a) Square wave with modulated rising edges, (b) decomposition into two waveforms, and (c) resulting magnitude of Fourier transform.

Let us first suppose a sinusoidal jitter, $T_m \cos \omega_m t$, is applied to only the rising edges of an ideal square wave, $p(t)$. As shown in Fig. 17(a), the rising edge at kT_{in} is displaced by an amount equal to $T_m \cos(\omega_m k T_{in})$. This jittery waveform can be expressed as the sum of $p(t)$ and a train of pulses that occur at kT_{in} with a width of $T_m \cos(\omega_m k T_{in})$ [Fig. 17(b)]. If $T_m \ll T_{in}$, the latter can be approximated by a train of impulses and expressed as

$$q(t) \approx T_m \sum_{k=-\infty}^{k=+\infty} \cos(\omega_m k T_{in}) \delta(t - kT_{in}). \tag{24}$$

Adding the Fourier transforms of $p(t)$ and $q(t)$, we obtain the result shown in Fig. 17(c), where each harmonic of the square wave is surrounded by two impulses of area $T_m/(2T_{in})$ at frequency offsets of $\pm f_m = \pm \omega_m/(2\pi)$. It can be shown that these sidebands generate only phase modulation (PM).

We thus observe that a jitter spectrum consisting of two impulses having an area of $T_m/2$ produces two PM sidebands around f_{in} whose normalized magnitude is equal to $\pi T_m/(2T_{in})$. That is, a jitter of $T_m/2$ yields a phase disturbance of $(\pi/T_{in})(T_m/2)$ rather than $(2\pi/T_{in})(T_m/2)$ in this case. One may expect this result because only the rising edges have been displaced.

We now generalize the foregoing observation to random jitter, while still assuming jitter on only the rising edges. If the jitter itself in the time domain is denoted by $\sigma(t)$, then (24) is rewritten as

$$q(t) \approx \sigma(t) \sum_{k=-\infty}^{k=+\infty} \delta(t - kT_{in}). \tag{25}$$

Adding the power spectral densities of $p(t)$ and $q(t)$, we obtain the overall spectrum shown in Fig. 18. Thus, the jitter spectrum, $S_\sigma(f)$, is shifted to $\pm f_{in}$, $\pm 2f_{in}$, etc., scaled by a factor of $1/T_{in}^2$, and normalized to a carrier power of $1/\pi^2$, yielding $(\pi^2/{T_{in}}^2) S_\sigma(f \pm f_{in})$, etc., for the phase noise.[7] MATLAB simulations confirm this result.

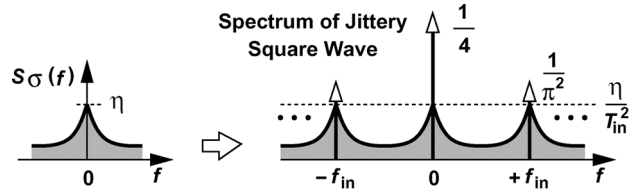

Fig. 18. Spectrum of jittery square wave.

Since the jitters on the rising and falling edges of a CMOS inverter's output are generated by different transistors and are hence uncorrelated, we write the overall phase noise of the square wave as

$$S_\Phi(f) = \frac{\pi^2}{T_{in}^2} \sum_{k=-\infty}^{k=+\infty} \left[S_{\sigma p}(f \pm k f_{in}) + S_{\sigma n}(f \pm k f_{in}) \right], \tag{26}$$

where $S_{\sigma p}$ and $S_{\sigma n}$ denote the spectra of the jitters produced by the PMOS and NMOS transistors, respectively. Note that S_σ and S_{Vn} are simply related by a factor of r_{edge}^2.

Appendix C
Spectrum of Shaped and Sampled White Noise

In this appendix, we examine the phase noise spectrum due to white noise:

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} \sum_{m=-\infty}^{m=+\infty} S_{Vn}\left(f - \frac{m}{T_{in}}\right). \tag{27}$$

Since the Fourier transform of the rectangular window, $w(t)$, is given by $\Delta T \sin(\pi f \Delta T)/(\pi f \Delta T)$, we have from (4)

$$S_{Vn}(f) = \frac{1}{C_L^2} \Delta T^2 \frac{\sin^2(\pi f \Delta T)}{(\pi f \Delta T)^2} S_{In}(f). \tag{28}$$

If $S_{In}(f)$ is white, then $S_{Vn}(f)$ has a sinc^2 shape; i.e., $S_\Phi(f)$ consists of sinc^2 functions centered at $mf_{in} = m/T_{in}$. We now prove that the sum of these sinc^2 functions is a flat line under a certain condition.

Considering only the sinc^2 shape itself, we recognize that the inverse Fourier transform of $\Delta T^2 \mathrm{sinc}^2(\pi f \Delta T)$ is a triangle, $g(t)$, with a time duration of $-\Delta T$ to $+\Delta T$ and a height of ΔT [Fig. 19(a)]. As a result of shifts of sinc^2 by mf_{in} in the frequency domain, $g(t)$ is multiplied by $\exp(j2\pi m f_{in} t)$ in the time domain:

$$g(t) \sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} \leftrightarrow \sum_{m=-\infty}^{m=+\infty} \Delta T^2 \frac{\sin^2\left[\pi \Delta T (f - m f_{in})\right]}{\left[\pi \Delta T (f - m f_{in})\right]^2}. \tag{29}$$

We also note that

$$\sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} = \frac{1}{f_{in}} \sum_{m=-\infty}^{m=+\infty} \delta(t - mT_{in}). \tag{30}$$

[7]Using Rice's approximation of random noise by a sum of sinusoids [9], it can be proved that the spectra at $\pm f_{in}$ produce only phase modulation.

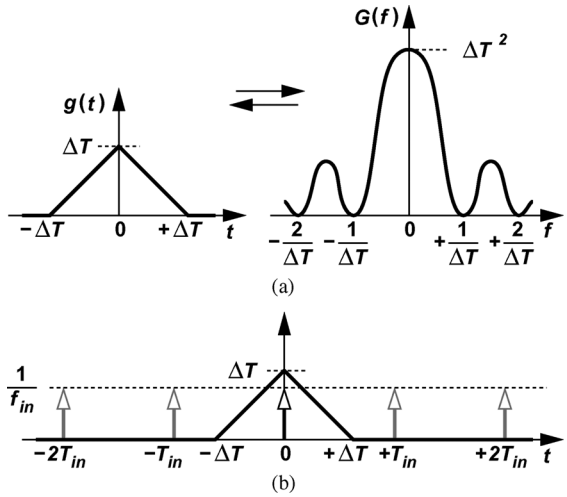

Fig. 19. Inverse Fourier transform of (a) sinc^2 function, and (b) shifted sinc^2 functions.

In other words, $g(t)$ is multiplied by a train of impulses centered at mT_{in} [Fig. 19(b)]. Thus, if the duration of $g(t)$ is short enough to enclose only the impulse at $t = 0$, we have

$$g(t)\sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} = \Delta T \frac{1}{f_{in}}\delta(t). \tag{31}$$

The Fourier transform of this result is equal to $\Delta T/f_{in}$ and hence:

$$\sum_{m=-\infty}^{m=+\infty} \Delta T^2 \frac{\sin^2\left[\pi\Delta T(f - mf_{in})\right]}{\left[\pi\Delta T(f - mf_{in})\right]^2} = \frac{\Delta T}{f_{in}}, \tag{32}$$

which is a flat line.

In summary, if the sampling period, T_{in}, is greater than the rectangular window width, ΔT, then the window-integrated and sampled white noise still has a white spectrum. Note that this result is valid for any shape chosen for $w(t)$ so long as the inverse Fourier transform of $|W(f)|^2$ has a total time duration less than $2T_{in}$, or more generally, so long as the inverse Fourier transform of $|W(f)|^2$ crosses zero at $t = mT_{in}$ except for $t = 0$.

Acknowledgment

The authors would like to thank Marco Zanuso for helpful discussions.

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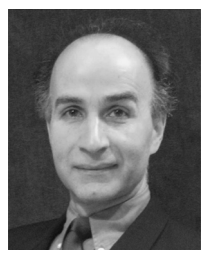

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