A Stabilization Technique for Phase-Locked Frequency Synthesizers

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***Abstract*—A stabilization technique is presented that relaxes the tradeoff between the settling speed and the magnitude of output sidebands in phase-locked frequency synthesizers. The method introduces a zero in the open-loop transfer function through the use of a discrete-time delay cell, obviating the need for resistors in the loop filter. A 2.4-GHz CMOS frequency synthesizer employing the technique settles in approximately 60 μs with 1-MHz channel spacing while exhibiting a sideband magnitude of −58.7 dBc. Designed for Bluetooth applications and fabricated in a 0.25-μm digital CMOS technology, the synthesizer achieves a phase noise of −112 dBc/Hz at 1-MHz offset and consumes 20 mW from a 2.5-V supply.**

***Index Terms*—Charge pumps, feedforward, loop stability, oscillators, phase-locked loops (PLLs), prescalers, synthesizers.**

I. Introduction

THE design of phase-locked loops (PLLs) must generally deal with a tight tradeoff between the settling time and the amplitude of the ripple on the oscillator control line. For phase-locked RF synthesizers, this tradeoff limits the performance in terms of the channel switching speed and the magnitude of the reference sidebands that appear at the output.

This paper describes a loop stabilization technique that yields a small ripple while achieving fast settling [1]. Using a discrete-time delay cell, the PLL architecture creates a zero in the open-loop transfer function. Another important advantage of the technique is that it uses no resistors in the loop filter, lending itself to digital CMOS technologies. Also, it "amplifies" the value of the loop filter capacitor, thus saving a great deal of silicon area. Realized in a 2.4-GHz CMOS synthesizer, the proposed method provides a settling time of approximately 60 reference cycles with an output sideband level of −59 dBc.

Section II of the paper develops the foundation for the proposed technique. Section III describes the 2.4-GHz synthesizer architecture and the design of its building blocks and Section IV proposes fast simulation techniques for RF synthesizers. Section V summarizes the experimental results.

II. Stabilization Technique

Consider the PLL shown in Fig. 1(a), where a voltage-controlled oscillator (VCO) is driven by a charge pump (CP) and a phase/frequency detector (PFD). Resistor R_1 provides the stabilizing zero and capacitor C_2 suppresses the glitch generated by the charge pump at every phase comparison instant. The glitch arises from: 1) the mismatch between the arrival times of the Up and Down pulses; 2) the mismatch between the widths of the Up and Down pulses; 3) the mismatch between the charge pump current sources (both random and due to channel-length modulation); and 4) the mismatch between the charge injection and clock feedthrough of the pMOS and nMOS switches in the charge pumps. Charge sharing also exacerbates the ripple [2].

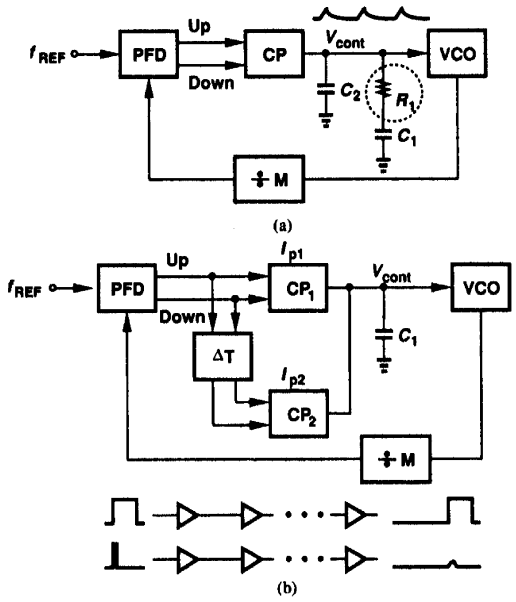

Fig. 1. (a) Conventional PLL architecture. (b) Proposed PLL architecture with delayed charge pump circuit.

The principal limitation of this architecture is that C_1 determines the settling whereas C_2 lowers the ripple on the control voltage. Since C_2 must remain below C_1 by roughly a factor of 10 so as to avoid underdamped settling, the loop must inevitably be slowed down by a large C_1 if C_2 is to sufficiently suppress the ripple. It is, therefore, desirable to seek methods of creating the stabilizing zero without the resistor so that the capacitor that defines the switching speed also directly suppresses the ripple.

A number of approaches to realizing a zero in PLLs have been reported [3]–[5]. The circuits in [3] and [4] require a transconductance amplifier, whose design for large output swings (necessary for maximizing the tuning range of *LC* VCOs) and low flicker noise becomes difficult. The synthesizer in [5] employs a voltage-controlled delay line but it mandates a large delay and a nearly rail-to-rail control voltage.

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It is important to note that the problem of ripple becomes increasingly more serious as the supply voltage is scaled down and/or the operating frequency goes up. The relative magnitude of the primary sidebands at the output of the VCO is given by $A_m K_{\rm VCO}/(2\omega_{\rm REF})$ where A_m is the peak amplitude of the first harmonic of the ripple, $K_{\rm VCO}$ is the gain of the VCO, and $\omega_{\rm REF}$ is the synthesizer reference frequency. For a given relative tuning range (e.g., $\pm 10\%$), the gain of *LC* VCOs must increase if the supply voltage goes down. If $K_{\rm VCO} = 100$ MHz/V and $f_{\rm REF} = 1$ MHz, then the fundamental ripple amplitude must be less than 63 μV to guarantee sidebands 60 dB below the carrier.

In order to arrive at the stabilization technique, consider the PLL architecture shown in Fig. 1(b). Here, the primary charge pump, CP_1, drives a single capacitor C_1 while a secondary charge pump, CP_2, injects charge after some delay ΔT. The total current flowing through C_1 is thus equal to

$$I_p = I_{p1} + I_{p2} e^{-s\Delta T} \tag{1}$$

$$\approx I_{p1} + I_{p2}(1 - s\Delta T) \tag{2}$$

where ΔT is assumed to be much smaller than the loop time constant. Consequently, the transfer function of the PFD/CP/LPF combination can be expressed as

$$\frac{V_{\rm cont}}{\Delta\phi}(s) = \frac{I_{p1} + I_{p2}}{2\pi C_1 s} - \frac{I_{p2}}{2\pi C_1}\Delta T. \tag{3}$$

Assuming $I_{p2} = -\alpha I_{p1}$, we have

$$\frac{V_{\rm cont}}{\Delta\phi}(s) = \frac{I_{p1}}{2\pi}\left(\frac{1-\alpha}{C_1 s} + \frac{\alpha\Delta T}{C_1}\right) \tag{4}$$

obtaining a zero at

$$\omega_z = \frac{1-\alpha}{\alpha}\frac{1}{\Delta T}. \tag{5}$$

Proper choice of ω_z can, therefore, stabilize the loop.

The damping factor and the settling time of the loop can be written, respectively, as

$$\zeta = \frac{\alpha\Delta T}{2}\frac{1}{C_1\sqrt{1-\alpha}}\sqrt{\frac{I_p K_{\rm VCO} C_1}{2\pi M}} \tag{6}$$

$$(\zeta\omega_n)^{-1} = \frac{2\pi C_1}{I_p \alpha \Delta T}\frac{M}{K_{\rm VCO}}. \tag{7}$$

In order to achieve a sufficiently low zero frequency, ΔT must be large or α close to unity. Since the accuracy in the definition of α is limited by mismatches between the two charge pumps, ΔT must still be a large value. For example, if $f_{\rm REF} = 1$ MHz, $C_1 = 50$ pF, $I_p = 200$ μA, $K_{\rm VCO} = 140$ MHz/V, $M = 2400$, and $\alpha = 0.9$, then a ΔT of approximately 500 ns is required to ensure a well-behaved loop response.

The architecture of Fig. 1(b) suffers from two critical drawbacks. First, it requires that the delay stage provide a very large ΔT *and* accommodate a wide range of Up and Down pulsewidths. Specifically, when the loop is locked, the Up and Down pulses are less than 500 ps wide. The tradeoff between delay and bandwidth, therefore, makes the design of the delay line difficult. As depicted in Fig. 1(b), if the bandwidth of each stage in the delay line is reduced so as to yield a large delay, then the narrow Up and Down pulses are heavily attenuated, giving rise to a dead zone. Conversely, if the bandwidth of each stage is wide enough to support such pulses, then a very large number of stages is required to obtain the necessary ΔT, demanding a high power dissipation.

The second issue relates to the variation of ΔT with process and temperature. Since ζ is directly proportionally to ΔT, such variations can greatly affect the loop stability.

To resolve the above difficulties, the architecture is modified as shown in Fig. 2(a), where a discrete-time analog delay line is placed *after* CP_2 and C_2. The delay network is realized as depicted in Fig. 2(b), consisting of two interleaved master-slave sample-and-hold branches operating at half of the reference frequency. The circuit emulates ΔT as follows. When $CK_{\rm even}$ is high, C_{s1} shares a charge packet corresponding to the previous phase comparison with C_1 while C_{s2} samples a level proportional to the present phase difference. In the next period, C_{s1} and C_{s2} exchange roles. The interleaved sampling network, therefore, provides a delay equal to the reference period $1/f_{\rm REF}$.

The discrete-time delay technique of Fig. 2 allows a precise definition of the zero frequency without the use of resistors. To quantify the behavior of a PLL incorporating this method, we assume the loop settling time is much greater than $1/f_{\rm REF}$ so that the delay network can be represented by the continuous-time model shown in Fig. 2(b). Here, $R_{\rm eq} = (f_{\rm REF} C_s)^{-1}$ approximates the interleaved branches. Equation (4) can then be rewritten as

$$\frac{V_{\rm cont}}{\Delta\phi}(s) = \frac{I_{p1}}{2\pi}\left(\frac{1}{f_{\rm REF} C_s} + \frac{I_{p1} + I_{p2}}{I_{p1}}\frac{1}{sC_2}\right) \tag{8}$$

where it is assumed $C_2 \gg C_1$ and the current through C_1 is neglected. This equation exhibits two interesting properties. First, if $I_{p2} = -\alpha I_{p1}$, then $(I_{p1} + I_{p2})/I_{p1} = 1 - \alpha$ and the value of C_2 is "amplified" by $(1-\alpha)^{-1}$. For example, if $\alpha = 0.9$, then C_2 is multiplied by a factor of 10, saving substantial area. Second, the zero frequency is equal to

$$\omega_z = \left(1 + \frac{I_{p2}}{I_{p1}}\right)\frac{C_s}{C_2} f_{\rm REF} \tag{9}$$

a value independent of process and temperature. Assuming $I_{p1} = -\alpha I_{p2} = I_p$, we obtain the damping factor and the settling time constant of the loop as

$$\zeta = \frac{1}{2 f_{\rm REF} C_s}\sqrt{\frac{I_p C_2}{2\pi(1-\alpha)}\frac{K_{\rm VCO}}{M}} \tag{10}$$

$$(\zeta\omega_n)^{-1} = \frac{4\pi f_{\rm REF} C_s}{I_p}\frac{M}{K_{\rm VCO}}. \tag{11}$$

Note that the damping factor exhibits much less process and temperature dependence than in the conventional loop of Fig. 1(a). Interestingly, for $I_{p2} = 0$, the proposed circuit resembles the topology of Fig. 1(a) but with the resistor replaced by a switched-capacitor network.

While providing insight and serving as design guidelines, the above results are obtained by a continuous-time approximation of the loop and their validity must be verified. Simulations using the values $I_p = 160$ μA, $K_{\rm VCO} = 140$ MHz/V, $C_2 = 50$ pF, and $\alpha = 0.4$ yield $\zeta = 0.36$ and $(\zeta\omega_n)^{-1} = 10.7$ μs. Equations (10) and (11) predict these parameters to be 0.31 and 13 μs, respectively. Thus, the continuous-time approximation provides a reasonably accurate estimate of the loop behavior even for

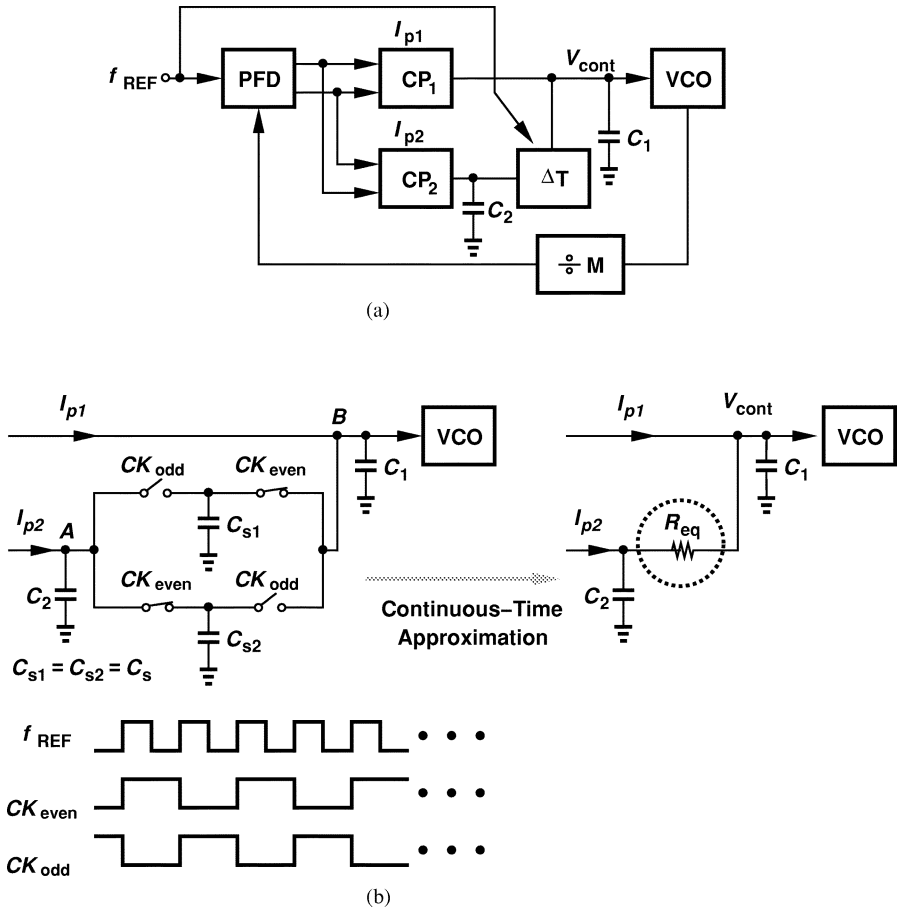

Fig. 2. Actual implementation of PLL with delay sampling circuit and continuous-time approximation of delay network.

underdamped settling (where the loop time constant is relatively short).

For RF synthesis, the delay network of Fig. 2(b) must be designed carefully so as to minimize ripple on the control voltage. Since in the locked condition, the voltages at nodes A and B are nearly equal, charge sharing between C_{s1} or C_{s2} and C_1 creates only a small ripple. Furthermore, the switches in the delay stage are realized as small, complementary devices to introduce negligible charge injection and clock feedthrough.

Comparison With Conventional Architecture In order to quantify the advantage of the proposed architecture over the conventional PLL topology, we note that capacitor C_1 in Fig. 2 appears in parallel with C_{s1} or C_{s2}. Since the sampling capacitors are typically two to three times larger than C_1, they suppress the charge pump nonidealities by about 9 to 12 dB.

The behavioral model shown in Fig. 3(a) is simulated in MATLAB for the two cases. As explained in Section IV, the reference frequency and the divide ratio are scaled by a factor of 100 to speed up the simulation. The nonideality of the charge pump is modeled by a constant current mismatch ΔI that is injected into the loop filter at each phase comparison instant.

Fig. 3(b) depicts the settling behavior and the output spectrum for the two cases. (The plots are deliberately offset for clarity). For approximately equal settling times, the proposed topology (Type A) achieves 10 dB lower sidebands than the conventional loop does.

III. Synthesizer Design

A 2.4-GHz CMOS synthesizer targeting Bluetooth applications has been designed using the stabilization technique described above. This section presents the architecture and building blocks of the synthesizer.

Shown in Fig. 4, the synthesizer uses an integer-N architecture with a feedback divider whose modulus is given by $M = NP + S + 1$[6], where $N = 4$, $P = 600$, and $S = 0$–127. With $f_{\rm REF} = 1$ MHz, the output frequency covers the 2.4-GHz ISM band. The output of the swallow counter is pipelined by the flip-flop $\rm FF_1$ to allow a relaxed design for the level converter and the swallow counter. The buffer following the VCO suppresses the kickback noise of the prescaler when the modulus changes. It also avoids limiting the tuning range of the VCO by the input capacitance of the prescaler.

A. VCO Design

The VCO topology is shown in Fig. 5(a). To provide both negative and positive voltages across the MOS varactors, the sources of M_1 and M_2 are grounded and the circuit is biased on top by I_{DD}. The inductors are realized as shown in Fig. 5(b), with the bottom spiral moved down to metal 2 so as to reduce the parasitic capacitance [7]. Each inductor is about 14 nH, occupies an area of 180 μm$\times$ 180 μm, and exhibits a Q of 4 and a parasitic capacitance of 100 fF.

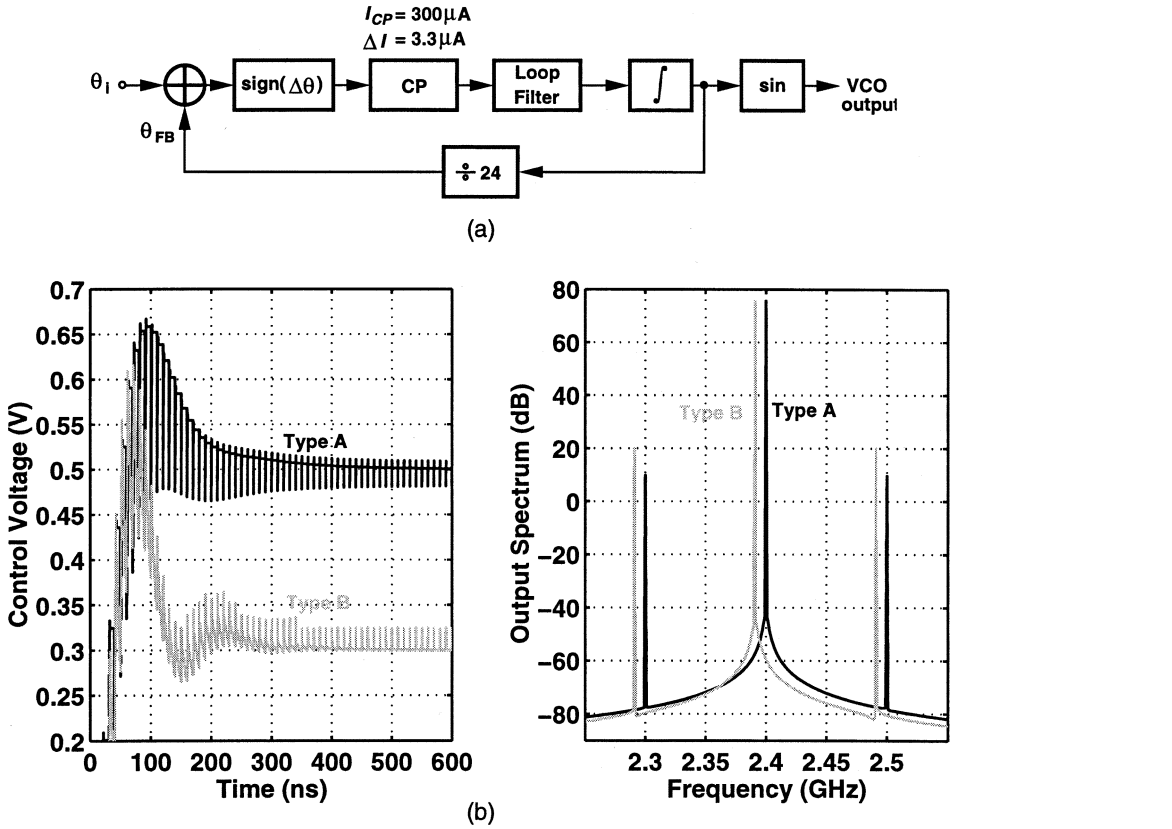

Fig. 3. (a) MATLAB behavioral simulations for the ripples on the control lines. (b) Time-domain settling and VCO output spectrum during lock for Type A (delay-sampling loop filter) and Type B (conventional loop filter).

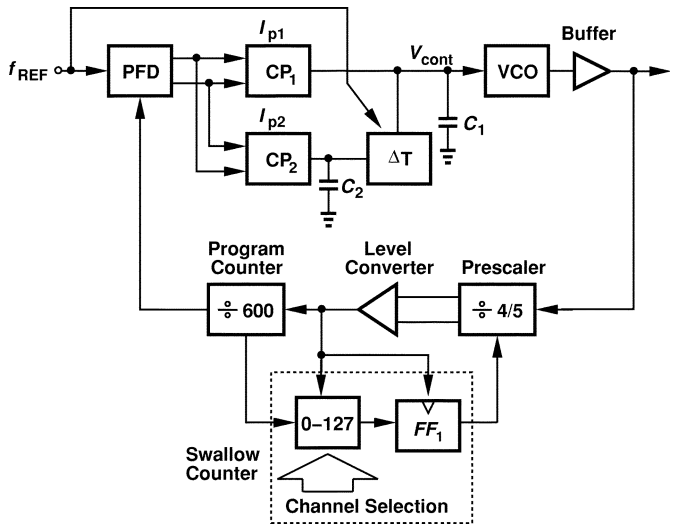

Fig. 4. Synthesizer architecture.

The varactors are implemented as accumulation-mode nMOS devices (placed inside n-well). In this design, a 160-fF varactor is employed to allow a tuning range of about 12%. The measured phase noise of the VCO is −120 dBc/Hz at 1-MHz offset.

B. Pulse-Swallow Counter

Shown in Fig. 6(a), the pulse-swallow counter consists of a prescaler, a program counter and a swallow counter. The pipelining in the swallow counter allows the use of a small divider ratio in the prescaler. Simulations suggest that a ÷4/5 topology minimizes the overall divider power dissipation.

The prescaler must divide the 2.4-GHz signal while consuming a small power dissipation. Depicted in Fig. 6(b), the circuit employs three current-steering flip-flops with diode-connected loads. The use of NOR gates obviates the need for power- and headroom-hungry level shift circuits (or large input swings) required in NAND gates. The program counter and the swallow counter incorporate static flip-flops to ensure reliable operation at low frequencies.

IV. Simulation Techniques

A 2.4-GHz synthesizer with a reference frequency of 1 MHz requires a transient simulation step of approximately 20 ps for a total settling time on the order of 100 μs, i.e., five million points. The simulation, therefore, requires an extremely long time (about 5 days on an Ultra 10 Sun Workstation) owing to both the vastly different time scales and the large number of devices (especially in the divider).

This section describes a number of techniques that reduce the simulation time by several orders of magnitude while revealing the loop dynamics with reasonable accuracy.

A. Linear Discrete-Time Model

The voltages at nodes A and B in Fig. 2(b) can be, respectively, expressed by the following discrete-time equations

$$V_A[n] = \frac{C_2 V_A[n-1] + C_s V_B[n-1]}{C_2 + C_s} + x[n]\frac{I_{p2}}{C_2 + C_s} \tag{12}$$

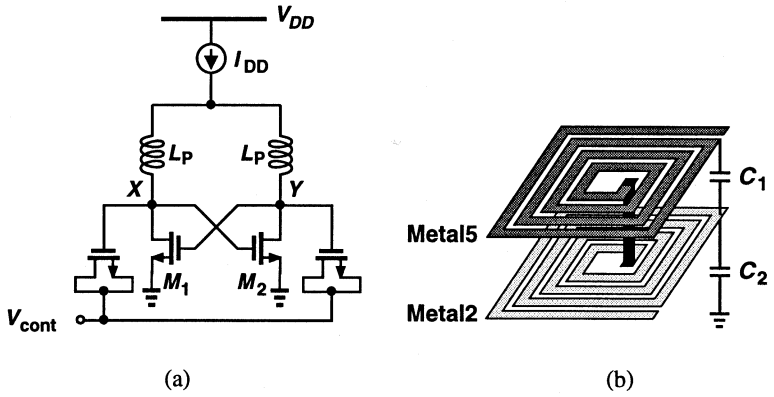

Fig. 5. (a) *LC* oscillator. (b) Two-layer stacked inductor.

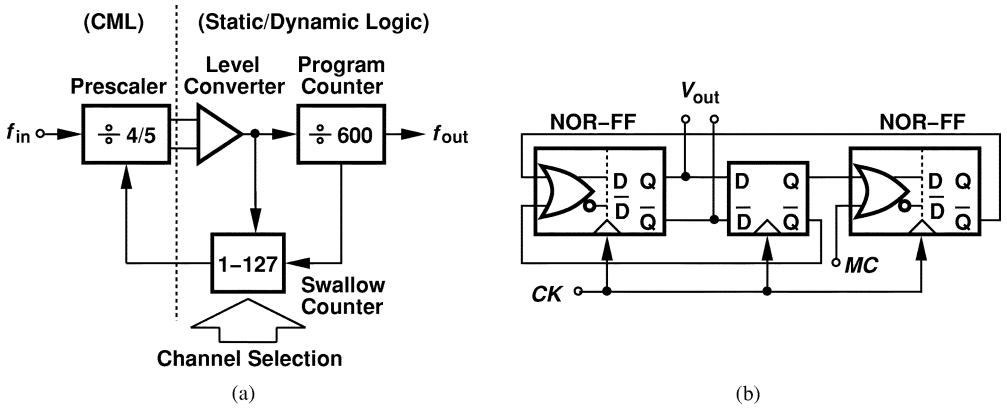

Fig. 6. (a) Divider. (b) Prescaler.

$$V_B[n] = \frac{C_1 V_B[n-1] + C_s V_A[n-1]}{C_1 + C_s} + x[n]\frac{I_{p1}}{C_1 + C_s} \tag{13}$$

where $x[n]$ denotes the input phase error. Even though the z transform of V_A and V_B can be derived, the high order of the resulting polynomials makes it difficult to derive the close-loop response in analytical form. Thus, the two equations, along with the rest of the PLL, are realized in MATLAB. The VCO is modeled as a phase accumulator, with each new value of phase obtained as the previous phase plus the product of the time interval and the new frequency. The phase detector is simply a subtractor, generating $x[n]$ for the above equations. The linear discrete-time model facilitates the choice of the charge pump current, the value of C_1, and the value of C_s for fast settling and minimum ripple on the oscillator control line.

Fig. 7 shows the settling behavior of the synthesizer as predicted by MATLAB and transistor-level implementation. The simple discrete-time model yields a moderate accuracy while requiring orders of magnitude less simulation time.

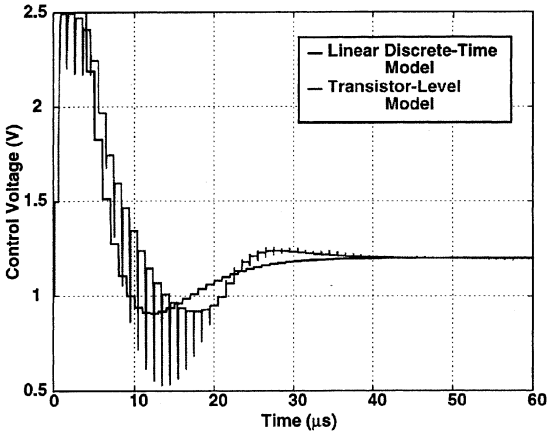

Fig. 7. Settling behavior of MATLAB and transistor-level simulations.

B. Transistor-Level Model

The impact of various PFD, CP, and VCO nonidealities upon the loop dynamics must ultimately be studied in a realistic transistor-level implementation. We present two techniques that reduce the simulation time from days to minutes.

The first method is based on "time contraction," whereby the reference frequency is scaled up by a factor of 100 and the main loop filter capacitor (C_2 in Fig. 2) and the divide ratio are scaled down by the same factor. All other loop parameters remain unchanged. From (10) and (11), we note that scaling C_2 and M by 100 maintains a constant damping factor while scaling the settling time by 100. Since the PFD operates reliably at 100 MHz with no dead zone, this method directly reduces the simulation time by a factor of 100.

Fig. 8 depicts an example of time contraction by a factor of 10. Note that the time axis has a logarithmic scale. It can be observed that the loop settling behavior scales accurately by the same factor.

In the second method, the divider is realized as a simple behavioral model in HSPICE that uses a handful of ideal devices and its complexity is independent of the divide ratio. Illustrated in Fig. 9, the principle of the behavioral divider is to pump a

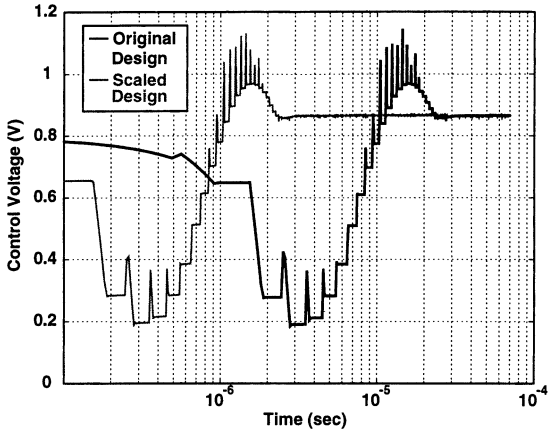

Fig. 8. Time contraction.

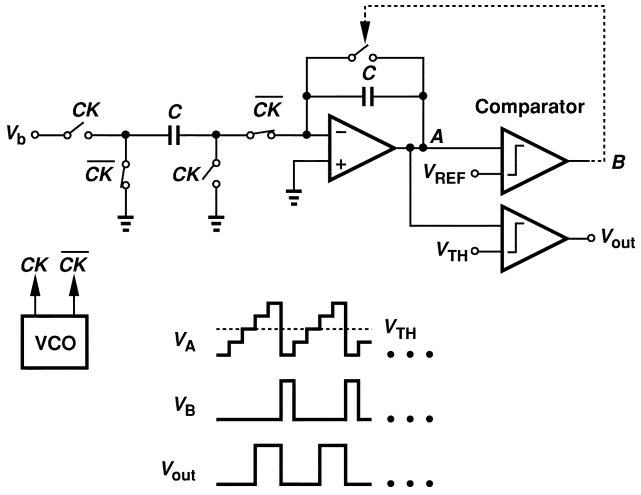

Fig. 9. Divider behavioral model.

TABLE I
FAST SIMULATION SUMMARY

	Original Design	Scaled Design
Reference Frequency	1 MHz	100 MHz
Divide Ratio	2400	24
Number of Transistors	729	157
Number of Time Steps	$5x10^6$	$5x10^4$
Simulation Time	5 days	3 mins

well-defined charge packet into an integrator in every period and reset the integrator when its output exceeds a certain level $V_{\rm REF}$. Using an ideal op amp, comparator, and switches with proper choice of V_b and $V_{\rm REF}$, the circuit can achieve arbitrarily large divide ratios. (The duty cycle of output can be controlled by $V_{\rm TH}$.) This technique yields another factor of 20 reduction in the simulation speed, allowing the synthesizer to be simulated in less than 3 min on an Ultra 10 Sun Workstation. Table I summarizes the results of the two simulation techniques.

V. Experimental Results

The frequency synthesizer has been fabricated in a digital 0.25-μm CMOS technology. Shown in Fig. 10 is a photograph

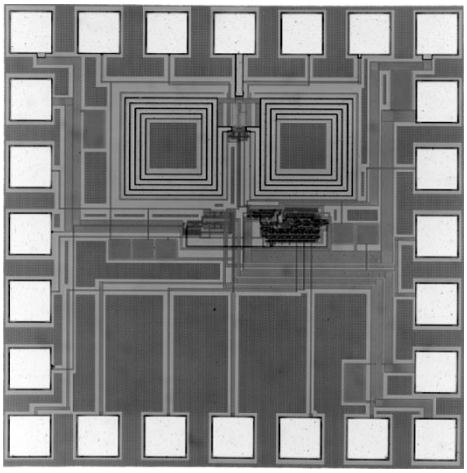

Fig. 10. Die photo.

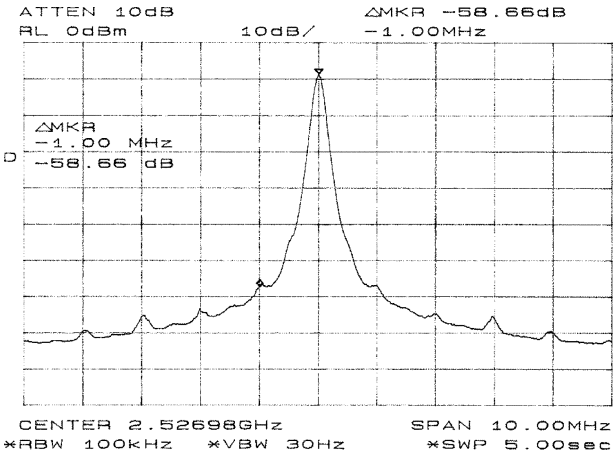

Fig. 11. Measured output spectrum of the synthesizer.

of the die, whose active area measures 0.65 mm $\times$ 0.45 mm. The circuit has been tested in a chip-on-board assembly while running from a 2.5-V power supply. The power dissipation is 20 mW.

Fig. 11 shows the output spectrum in the locked condition. The phase noise is equal to -112 dBc/Hz at 1 MHz offset, well exceeding the Bluetooth requirement. The primary reference sidebands are at approximately -58.7 dBc. This level is lower than that achieved in [8] with differential VCO control and an 86.4-MHz reference frequency. Similarly, the designs in [9] and [10] exhibit an inferior tradeoff between the settling time and the sideband magnitudes.

Fig. 12 plots the measured settling behavior of the synthesizer when its channel number is switched by 64. Here, the channel select input is periodically switched between the two end channels and the oscillator control voltage is monitored. The settling time is about 60 μs, i.e., 60 input cycles. Table II summarizes the measured performance of the synthesizer.

VI. Conclusion

A PLL stabilization technique is introduced that relaxes the tradeoff between the settling time and the ripple on the control voltage, while obviating the need for resistors in the loop filter. The proposed approach creates a zero in the open loop

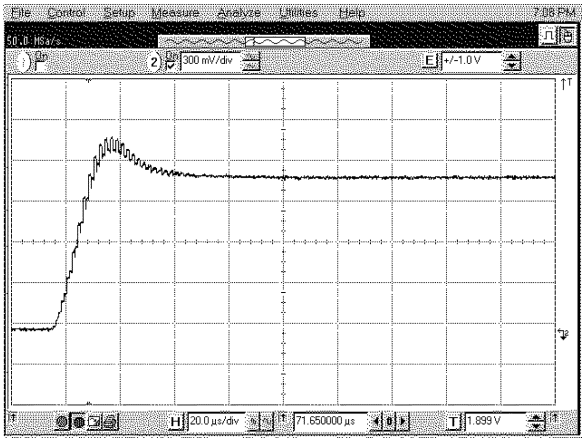

Fig. 12. Control voltage during loop settling.

TABLE II
SYNTHESIZER PERFORMANCE SUMMARY

Center Frequency	**2.4 GHz**
Channel Spacing	**1 MHz**
No. of Channels	**128**
Phase Noise at 1 MHz Offset	**–112 dBc/Hz**
Reference Sidebands	**–58.7 dBc**
Settling Time	**60 µs**
Estimated Bandwidth	**80 kHz**
Power Dissipation	
VCO	**10 mW**
VCO Buffer	**3 mW**
Divider	**6 mW**
Charge Pump	**0.5 mW**
Others	**0.5 mW**
Total	**20 mW**
Supply Voltage	**2.5 V**
Die Area	**0.65 mm x 0.45 mm**
Technology	**0.25–µm CMOS**

transfer function by adding two consecutive phase comparison results and can be extended to more consecutive samples as in a transversal filter. The method also "amplifies" the loop filter capacitor by a large number (e.g., 10), saving substantial chip area. The proposed concepts are demonstrated in a 2.4-GHz RF CMOS synthesizer.

The stabilization technique finds applications in other phase-locked systems as well. Examples include clock generators and clock and data recovery circuits.

REFERENCES

[1] T. C. Lee and B. Razavi, "A stabilization technique for phase-locked frequency synthesizers," in *VLSI Symp. Dig. Tech. Papers*, June 2001, pp. 39–42.

[2] M. G. Johnson and E. L. Hudson, "A variable delay line PLL for CPU-coprocessor synchronization," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1218–1223, Oct. 1988.

[3] I. I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and ±50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 11, pp. 1259–1265, Nov. 1995.

[4] S. Sidiropoulos, D. Liu, J. Kim, G. Wei, and M. Horowitz, "Adaptive bandwidth DLL's and PLL's using regulated supply CMOS buffers," in *VLSI Symp. Dig. Tech. Papers*, June 2000, pp. 124–127.

[5] A. Zolfaghari, A. Chan, and B. Razavi, "A 2.4-GHz 34-mW CMOS transceiver for frequency-hopping and direct-sequence applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp. 1259–1265.

[6] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-µm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, pp. 788–794, May 2000.

[7] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE J. Solid-State Circuits*, pp. 620–628, Apr. 2001.

[8] L. Lin, L. Tee, and P. R. Gray, "A 1.4-GHz differential low-noise CMOS frequency synthesizer using a wideband PLL architecture," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2000, pp. 204–205.

[9] T. K. K. Kan, G. C. T. Leung, and H. C. Luong, "A 2-V 1.8-GHz fully integrated CMOS dual-loop frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1012–1020, Aug. 2002.

[10] C.-W. Lo and H. C. Luong, "A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications," *IEEE J. Solid-State Circuits*, vol. 37, pp. 459–470, Apr. 2002.

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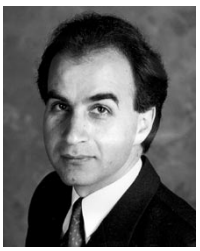

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