A Harmonic-Rejecting CMOS LNA for Broadband Radios

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***Abstract*—The local oscillator harmonics corrupt the desired signal in broadband RF receivers by downconverting interferers. This paper proposes the notion of harmonic rejection in the front-end low-noise amplifier so as to relax the stringent matching required of harmonic-reject mixers. Described are frequency response shaping techniques by feedforward and unilateral Miller capacitance multiplication for a signal bandwidth of 100 MHz to 10 GHz. A calibration algorithm is also proposed for the tuning of the frequency response. An experimental prototype fabricated in 65-nm digital CMOS technology provides at least 20 dB of rejection while consuming 8.64 mW with a 1.2-V supply.**

***Index Terms*—Broadband LNA, harmonic rejection, harmonic-rejecting LNA, notch filter, widely tunable filter.**

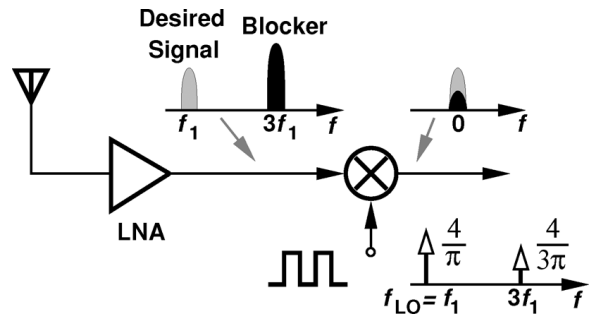

Fig. 1. Problem of LO harmonics in a direct-conversion receiver.

I. Introduction

THE potential of broadband RF transceivers for multi-standard, multi-band and/or cognitive radios has motivated extensive research in the past 10 years. It is envisioned that a radio operating from lower TV bands (around 100 MHz) to about 10 GHz could serve the communication needs in a variety of applications.

Among the issues encountered in broadband receiver design, the problem of local oscillator (LO) harmonics has received considerable attention [1]–[3] as it leads to significant signal corruption in the presence of large blockers. Absent in conventional narrowband radios, this issue tends to raise both the power dissipation and complexity of the receiver.

This paper introduces a 100-MHz to 10-GHz harmonic-rejecting low-noise amplifier (LNA) developed to relax the design of broadband receivers. The LNA incorporates notch and low-pass filtering techniques so as to reject by at least 20 dB input blockers at the third and higher harmonics of the LO. A calibration algorithm is also proposed that adjusts the frequency response so as to maximize the rejection. Realized in 65-nm digital CMOS technology, an experimental prototype provides tunable rejection from 300 MHz to 10 GHz while consuming 8.64 mW with a 1.2-V supply.

Section II provides the background for this work, emphasizing the challenges in harmonic-reject mixers (HRMs). Section III describes the LNA design, proposing frequency response shaping technique such as feedforward and unilateral Miller capacitance multiplication. Section IV deals with the calibration of the frequency response and Section V presents the experimental results.

II. Background

Consider the direct-conversion receiver in Fig. 1, where only one downconversion mixer is shown for simplicity. If optimized for noise and gain, mixers typically perform abrupt switching, thus multiplying the RF input by a square-wave LO. As a result, input blockers coinciding with the LO harmonics are also downconverted to the baseband. With differential implementations, the odd harmonics are much more pronounced but the even harmonics may warrant attention as well [4]. In this paper, we denote the desired input frequency by f_1 and a possible blocker at the third LO harmonic by $3f_1$. The principal challenge is that the LO harmonics decay only in proportion to $1/f$, posing severe rejection requirements on the receiver.

The effect of LO harmonics can be suppressed through the use of harmonic-reject mixers, as first realized by [5] in a transmitter and later demonstrated by [1]–[3] in receivers. Using 45° phases of the LO, HRMs can reject the third and fifth harmonics in proportion to the matchings in the LO path and in the RF path. For example, [1] attenuates these harmonics by 60 dB for $f_1 \leq 800$ MHz while consuming 17.1 mW in the LO distribution network. The design in [3], on the other hand, is insensitive to device mismatches but accommodates only $f_1 \leq 300$ MHz.

The problem of phase mismatch in HRMs becomes more serious as higher input frequencies are considered. It can be shown that a phase mismatch of ΔT seconds between only two phases of the LO limits the rejection at the third and fifth harmonics to the following values:

$$A_{\text{rej3}} = \frac{\sin\left(\frac{3\pi\Delta T}{T_{\text{LO}}}\right)}{3\cos\left(\frac{\pi\Delta T}{T_{\text{LO}}}\right)} \tag{1}$$

Manuscript received August 29, 2012; revised November 22, 2012; accepted December 12, 2012. Date of publication January 22, 2013; date of current version March 22, 2013.This paper was approved by Guest Editor Hideyuki Kabuo.

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Digital Object Identifier 10.1109/JSSC.2013.2237651

$$A_{\text{rej5}} = \frac{\sin\left(\frac{5\pi\Delta T}{T_{\text{LO}}}\right)}{5\cos\left(\frac{\pi\Delta T}{T_{\text{LO}}}\right)}, \quad (2)$$

where T_{LO} denotes the LO period. If ΔT is small, we have $A_{\text{rej3}} \approx A_{\text{rej5}} \approx \pi\Delta T/T_{\text{LO}}$. For example, to obtain a rejection of 60 dB for $f_1 = 2$ GHz, a ΔT of less than 150 fs is necessary, which may not be possible even with careful layout. Of course, mismatches among the other LO phases and among the RF paths further exacerbate this issue. Note that a calibration scheme that seeks to reduce the mismatch from, say, 10 ps, to, say, 50 fs, would require 200 steps and hence substantial complexity.

We should also remark that HRMs operating with 45° LO phases do not suppress higher harmonics, e.g., the seventh or ninth, a serious drawback as the input band of interest approaches or exceeds one decade. For example, in the range of 100 MHz to 10 GHz, if $f_1 = 100$ MHz, then the blockers at LO harmonics up to the *hundredth* must be rejected.

The objective of this paper is to demonstrate that the task of harmonic rejection can be partially shouldered by the LNA, thus relaxing the matching required of HRMs. A rejection of 20 dB is targetted to allow a tenfold increase in the mixers' mismatch budget.

III. Harmonic Rejection in LNA

Blockers at LO harmonics can be attenuated by means of filtering. For broadband operation, the filter must be tunable in sufficiently small steps so as to reject the blockers according to the selected LO frequency. Also, the filter *parasitics* must not degrade the LNA gain and noise figure (NF) significantly when the LNA must amplify high frequencies. These two principles govern the evolution of the LNA reported here. It is worth noting that band-pass filtering techniques based on N-path mixing [6]–[8] do not yield significant attenuation at the LO harmonics [9], [10]. Similarly, the feedforward interference cancellation techniques introduced in [11] and [12] do not provide harmonic rejection since they also use frequency mixing in the feedforward paths.

Let us contemplate an RC filter with programmable capacitors interposed between the LNA and the downconversion mixers. In order to tune the rejection from $3f_1 = 300$ MHz to 10 GHz, the capacitor value(s) must vary by about a factor of 30, e.g., from $30C_u$ to C_u. If the unit capacitor (or its switch) introduces a parasitic of, say, $0.02C_u$ in the signal path, then the circuit suffers from a total parasitic of about $0.6C_u$ when all of the units are *switched out* and the input frequency is near 10 GHz. If designed to attenuate $3f_1 = 10$ GHz by tens of decibels when one C_u is switched in, the filter unfortunately also exhibits a similar attenuation for $f_1 = 10$ GHz and a parasitic loading of $0.6C_u$. In other words, such a tunable filter inevitably produces considerable pass-band loss when programmed for high input frequencies.

The foregoing issues become even more serious for LC filter implementations due to the square-root dependence of cut-off frequencies upon the capacitor value(s). For example, the design in [13] employs an off-chip inductor to tune a band-pass filter from 65 MHz to 400 MHz.

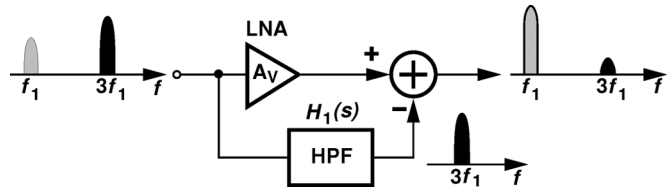

Fig. 2. Low-pass filtering by feedforward.

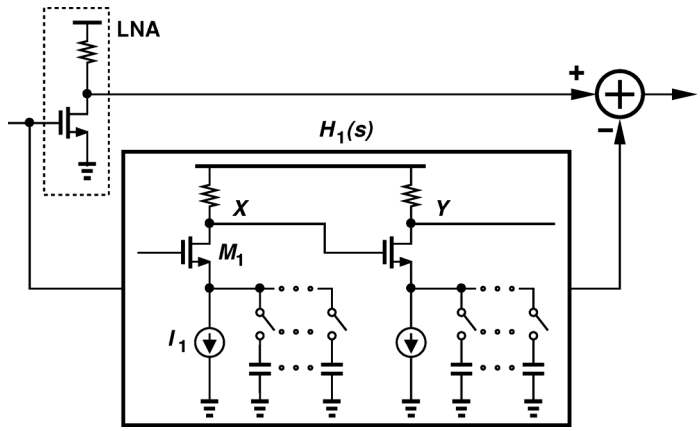

Fig. 3. LNA using capacitively-degenerated feedforward.

A. Filtering by Feedforward

Following our principle that any means of filtering must minimally load the signal path, we consider creating a low-pass response by feedforward (Fig. 2). If the high-pass filter (HPF) suppresses the desired component at f_1 and passes the blocker at $3f_1$ with no phase or gain error, then the output is free from the blocker. Now, the filter devices negligibly affect the signal path. Also, in contrast to HRMs, this approach attenuates *all* blockers lying within the HPF's passband, including those *not* at the LO harmonics.

The above scheme entails four issues: (1) the HPF input impedance may severely degrade the input matching; (2) the parasitics introduced by the filter devices in the feedforward path alter its gain and phase, prohibiting complete cancellation of the blocker(s) at the subtractor output; (3) the HPF must have a high enough order to reject the desired signal by a large factor, e.g., 10, while negligibly affecting the blocker(s); and (4) the feedforward path's noise at f_1 adds to the LNA output and must be minimized.

To address the first three issues, one can realize the HPF as a cascade of capacitively-degenerated common-source stages, as conceptually illustrated in Fig. 3. Here, the source capacitors can be programmed across a wide range and their parasitics do not attenuate the high-frequency components traveling through the feedforward path. The input capacitance of the HPF is fairly small and can be managed as explained below.

The fourth issue, namely, the HPF output noise at f_1 still persists. While the noise produced by the first stage, e.g., that due to M_1 and I_1, is attenuated roughly by the same factor as the input (at f_1) to $H_1(s)$, the noise of the subsequent stages experiences progressively less attenuation. Thus, a multi-stage HPF may degrade the overall noise figure considerably.

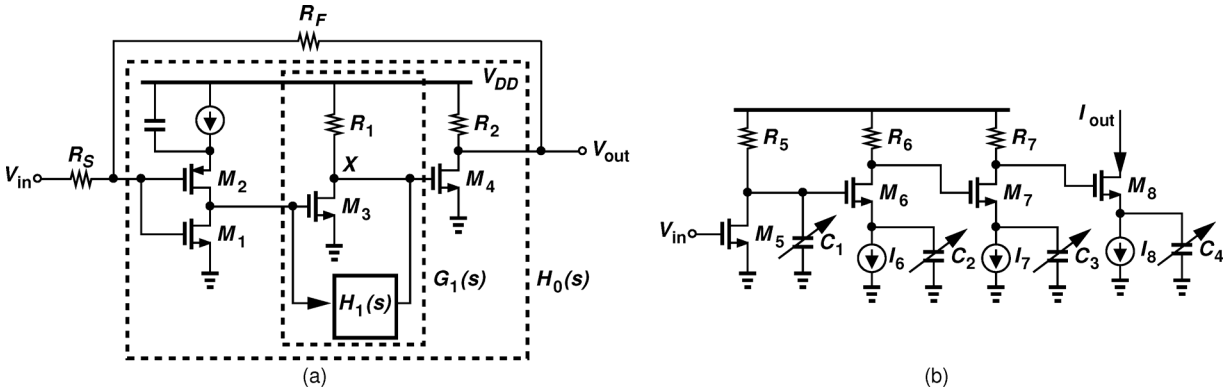

Fig. 4. (a) Resistive-feedback LNA with embedded HPF, (b) implementation of $H_1(s)$.

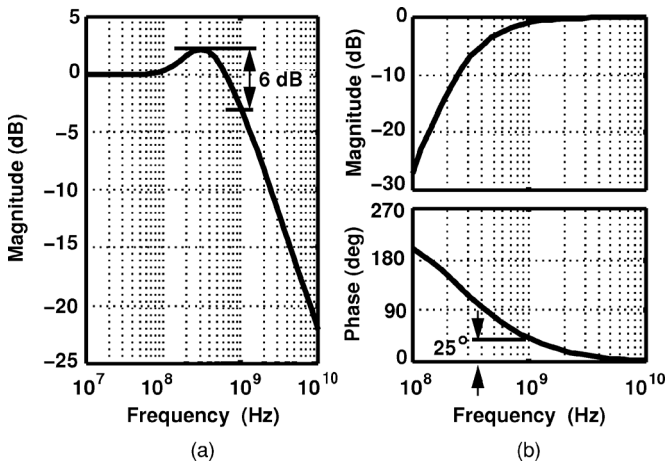

Fig. 5. Frequency response of (a) $H_0(s)$, and (b) $H_1(s)$ ($f_1 = 330$ MHz).

B. LNA With Embedded Feedforward

This section describes the evolution of the LNA design as various frequency response shaping techniques are applied to it so as to reject blockers at the LO harmonics. In each case, the simulated response is presented, issues are revealed, and methods are devised to resolve them. For most of the analysis. we assume a desired channel at $f_1 = 330$ MHz as an example.

This work employs the broadband feedback LNA described in [4] and embeds the frequency-selective feedforward within the LNA as shown in Fig. 4(a). The LNA itself is designed such that $R_F/(1 + A_0) = R_S$, where $-A_0$ denotes the open-loop gain. Preceded by a gain stage, the HPF now contributes negligibly to the NF. The active HPF implementation is depicted in Fig. 4(b), where M_5 serves as a dc interface and M_6–M_8 provide programmable high-pass filtering. Each of capacitors C_1–C_4 is formed as a 6-bit array. (The role of C_1 is described below). Ignoring C_1 for now, we can express $H_1(s) = I_{\rm out}(s)/V_{\rm in}(s)$ in Fig. 4(b) as

$$H_1(s) = -g_{m5}R_5 \cdot \frac{g_{m6}C_2 s R_6}{C_2 s + g_{m6}} \cdot \frac{g_{m7}C_3 s R_7}{C_3 s + g_{m7}} \cdot \frac{g_{m8}C_4 s}{C_4 s + g_{m8}}. \tag{3}$$

For feedforward cancellation, we choose the pass-band transconductance, $-g_{m5}R_5 g_{m6}R_6 g_{m7}R_7 g_{m8}$, equal to g_{m3}. Assuming $C_2 = C_3 = C_4 = C_f$ and $g_{m6} = g_{m7} = g_{m8} = g_{mf}$, we obtain the transfer function of the second stage of the LNA, $G_1(s)$, as follows:

$$\begin{aligned} G_1(s) &= g_{m3}R_1 \left[1 - \left(\frac{C_f s}{C_f s + g_{mf}}\right)^3\right] \\ &= g_{m3}R_1 \cdot \frac{3g_{mf}}{C_f} \cdot \frac{s^2 + \frac{g_{mf}}{C_f}s + \frac{g_{mf}^2}{3C_f^2}}{\left(s + \frac{g_{mf}}{C_f}\right)^3}. \end{aligned} \tag{4}$$

The above transfer function applies to the second stage of the *open-loop* LNA. The closed-loop transfer function is given by

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = \frac{R_F}{R_S + R_F} \cdot \frac{H_0(s)}{1 - \frac{R_S}{R_S + R_F}H_0(s)}, \tag{5}$$

where $H_0(s)$ is the overall open-loop LNA transfer function. To include the feedforward action, we write from (4)

$$H_0(s) = -A_0 \cdot \frac{3g_{mf}}{C_f} \cdot \frac{s^2 + \frac{g_{mf}}{C_f}s + \frac{g_{mf}^2}{3C_f^2}}{\left(s + \frac{g_{mf}}{C_f}\right)^3}, \tag{6}$$

where $-A_0$ denotes the low-frequency gain.[1] Since $R_F = (1 + A_0)R_S$, (5) emerges as

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = -A_0 \cdot \frac{3g_{mf}}{C_f} \cdot \frac{s^2 + \frac{g_{mf}}{C_f}s + \frac{g_{mf}^2}{3C_f^2}}{\left(1 + \frac{1}{1 + A_0}\right)s^3 + \frac{6g_{mf}}{C_f}s^2 + \frac{6g_{mf}^2}{C_f^2}s + \frac{2g_{mf}^3}{C_f^3}}. \tag{7}$$

Fig. 5(a) plots the simulated frequency response of $H_0(s)$ with the three feedforward poles in (6) placed at 280 MHz for $f_1 = 330$ MHz. The response exhibits a peaking of about 2 dB around f_1 and an attenuation of only 6 dB at $3f_1 = 1$ GHz. This deficiency originates from the phase shift caused by the zeros in (6) at $3f_1$. As illustrated in Fig. 5(b), the magnitude of the

[1]The capacitor in parallel with the current source in the first stage of the LNA does not appear in $H_0(s)$ as it is large enough to provide an ac ground above 100 MHz.

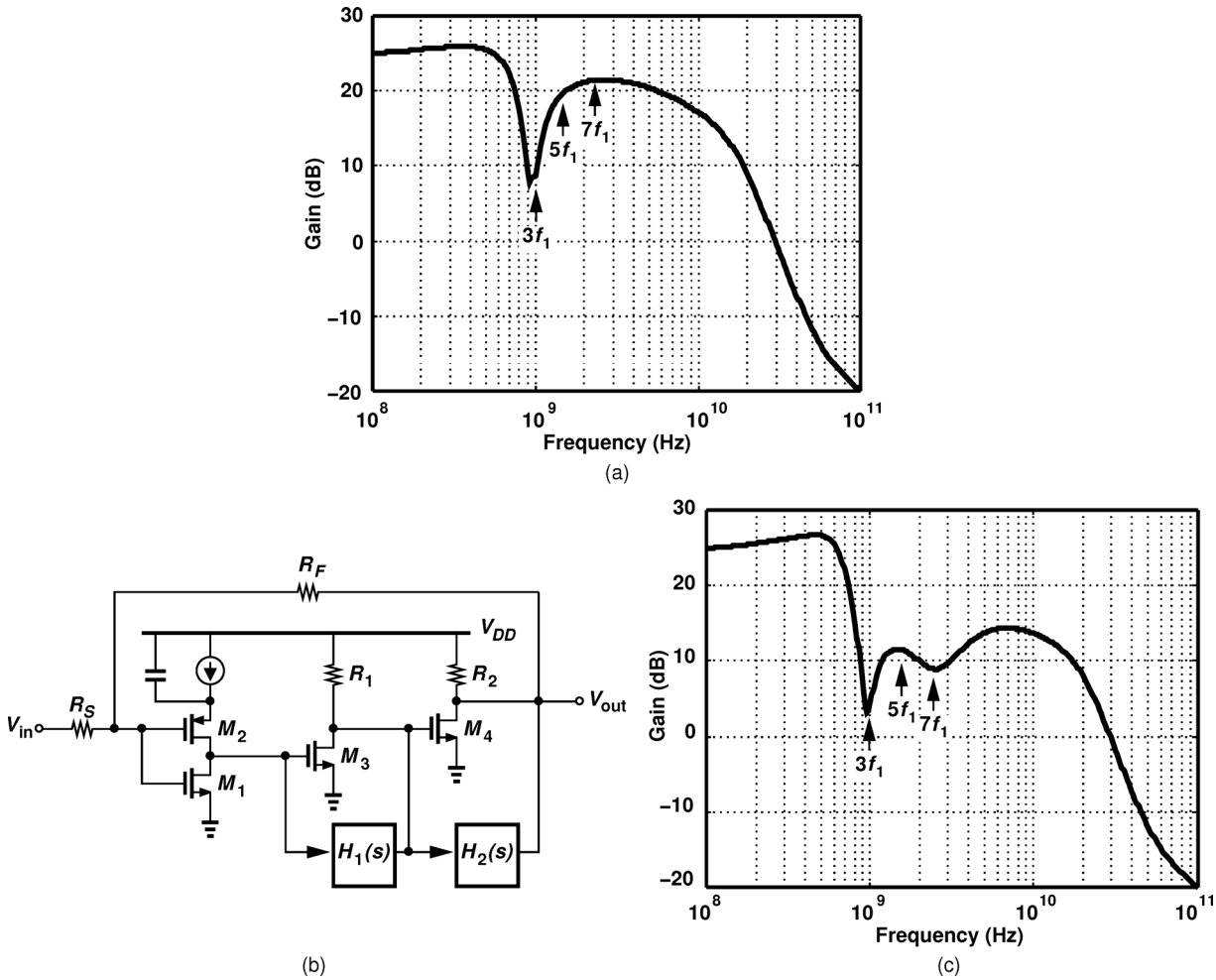

Fig. 6. (a) LNA frequency response with pole phase lag ($f_1 = 330$ MHz), (b) LNA with two HPFs, $H_1(s)$ and $H_2(s)$, (c) LNA frequency response with $H_1(s)$ and $H_2(s)$ ($f_1 = 330$ MHz).

feedforward transfer function, $|H_1(j\omega)|$, is about -0.9 dB at 1 GHz, suggesting a cancellation factor of about 10, but the phase reaches 25°, yielding a residual component with a normalized magnitude of $20\log(\sin 25°) = -7.5$ dB.

The zeros' phase lead can be compensated by a pole's phase lag, as realized by capacitor C_1 in Fig. 4(b). Also a 6-bit array, this capacitor is programmable in tandem with C_2–C_4. Fig. 6(a) shows the result of this attempt: the inserted lag now allows a rejection of about 20 dB at $3f_1$, but it also alters the phase at higher LO harmonics, creating a large hump in the LNA frequency response. Fortunately, the feedforward concept can be repeated around the *third* stage of the LNA so as to introduce zeros at the higher harmonics. Depicted in Fig. 6(b), this path, $H_2(s)$, contains three 5-bit programmable zeros but no programmable pole, yielding the response plotted in Fig. 6(c). The rejection at $5f_1$ and $7f_1$ is improved but the hump at higher harmonics is still unacceptably high. This is because the intrinsic poles of $H_1(s)$ and $H_2(s)$, e.g., those at the drains M_6 and M_7 in Fig. 4(b), collectively contribute significant phase shift even though they are located well above 10 GHz.

C. Unilateral Miller Effect

In order to further shape the LNA frequency response, we can consider the use of a Miller capacitor at the input. For example, a programmable capacitor tied between the input and output of the first stage in Fig. 4(a) could form an LPF with R_S, attenuating high frequencies and hence removing the hump in Fig. 6(c). Depicted in Fig. 7(a), this approach would violate one of the two principles mentioned at the beginning of Section III: for the capacitor to be large enough to serve at the lowest $3f_1$(=300 MHz), its parasitics would load the signal path so much that the LNA would not accommodate the highest f_1(≈10 GHz).

In order to isolate the output of the LNA's first stage from the parasitic loading of such a large capacitor, we can envision a *unilateral* Miller arrangement, whereby the feedback capacitor is driven by a buffer on the output side [Fig. 7(b)]. An ideal unity-gain buffer would yield an input pole at $\{[1 + (g_{m1} + g_{m2})(r_{o1}||r_{o2})]R_S C_{\rm mill}\}^{-1}$ but we can ask what happens if the buffer provides voltage gain. With a gain of B_0, the buffer lowers the pole frequency to

$$\omega_p = \frac{1}{[1 + B_0(g_{m1} + g_{m2})(r_{o1}||r_{o2})]\, R_S C_{\rm mill}} \tag{8}$$

thus allowing a smaller value for $C_{\rm mill}$.

Let us go one step further and ask what happens if B_0 itself is frequency-dependent. In particular, if B_0 has a high-pass response, then the Miller multiplication factor of $C_{\rm mill}$ *rises* with frequency, making $C_{\rm mill}$ a "supercapacitor." This intuition

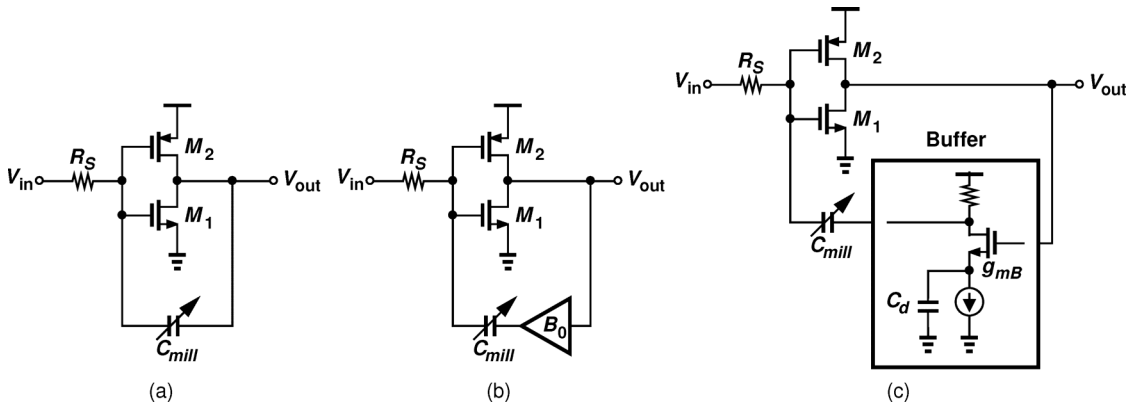

Fig. 7. (a) Conventional Miller capacitor, (b) unilateral Miller capacitor, (c) unilateral Miller "supercapacitor."

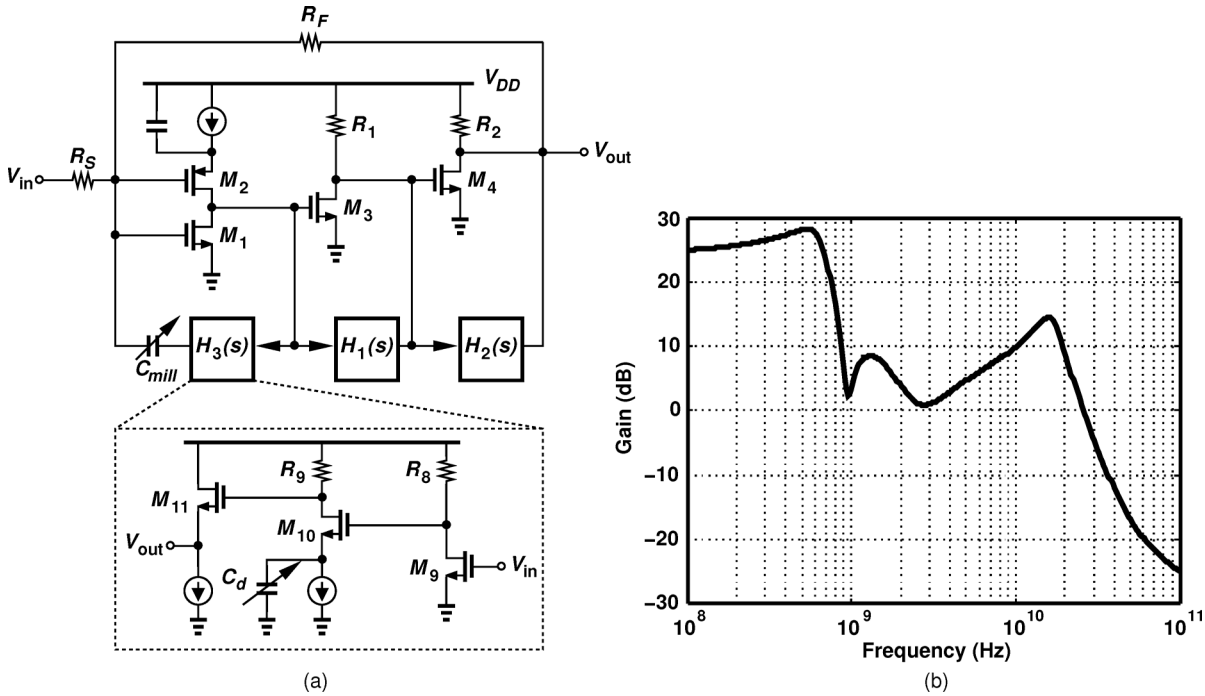

Fig. 8. (a) LNA with HPFs and the unilateral Miller path, (b) LNA frequency response with HPFs and the unilateral Miller path.

can be quantified by expressing the buffer transfer function as, for example, that of a capacitively-degenerated CS stage, $B_0C_ds/(C_ds + g_{mB})$, where C_d denotes the degeneration capacitance [Fig. 7(c)]. The LNA's first stage response is now written as

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = \frac{-g_{mF}R_L(C_ds + g_{mB})}{(1 + B_0g_{mF}R_L)R_SC_dC_{\rm mill}s^2 + (g_{mB}R_SC_{\rm mill} + C_d)s + g_{mB}} \quad (9)$$

where $g_{mF} = g_{m1} + g_{m2}$ and $R_L = r_{o1}||r_{o2}$. In this work, the pole frequencies are chosen approximately equal to $4f_1$, so that the Miller path does not degrade the NF at f_1. The zero is located around $9f_1$.

Fig. 8(a) shows the LNA circuit along with the unilateral Miller capacitance circuit. The corresponding response is plotted in Fig. 8(b), exhibiting improved rejection up to 10 GHz but still insufficient to meet the 20-dB target. The rise in the response stems from the parasitic poles within the unilateral buffer, calling for additional shaping of the frequency response.

The overall LNA incorporates two more feedback capacitors to achieve at least 20 dB of rejection at all frequencies equal to or greater than $3f_1$ for $f_1 = 100$ MHz to 3.3 GHz. As depicted in Fig. 9(a), capacitor C_6 dominates the Miller path at high frequencies. Capacitor $C_{\rm FB}$ improves both the rejection and the input matching. The black solid plot in Fig. 9(b) shows the final response.

The matching between the gains of the LNA main path and the feedforward paths ultimately determines the amount of blocker rejection that the overall circuit can provide. Fortunately, if the gain of the feedforward paths is *greater* than that of main paths, then it is still possible to obtain a high rejection by adjusting the amount of capacitive degeneration. Accordingly, in this design, the feedforward gains are deliberately chosen 20% *higher* than the necessary values. As verified

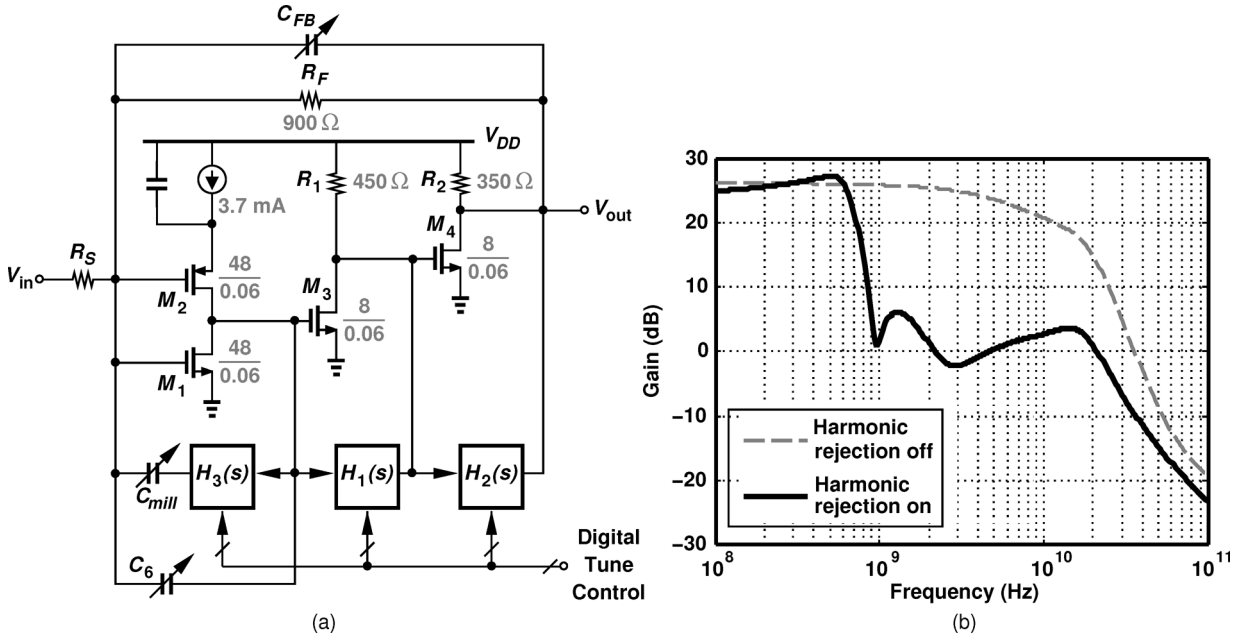

Fig. 9. (a) Final LNA topology (transistor dimensions in microns), (b) LNA frequency response with harmonic rejection off or on.

by experimental results, this skew, along with the calibration algorithm, allows the LNA to find a rejection of at least 20 dB.

D. NF Behavior

The frequency response shaping techniques described above can potentially degrade the noise figure (and input matching) of the LNA. Indeed, many other filtering methods were tried with various LNA topologies and discarded for this reason. The NF penalty arises primarily from the noise contributed by the feed-forward paths, $H_1(s)$ and $H_2(s)$, in Fig. 9(a). The unilateral Miller path only manifests itself at high harmonics, thus negligibly raising the NF in the channel of interest.

In order to quantify the NF penalty due to $H_1(s)$, we return to the implementation in Fig. 4(b) and seek the transfer functions for M_5–M_8, R_5–R_7, and I_6–I_8 to $I_{\rm out}$. The sum of these contributions is then multiplied by R_1 in Fig. 4(a) and referred to the LNA input. Upon traveling through the high-pass filter, the noise of M_5 and R_5 is suppressed along with the desired signal. The noise of the subsequent stages is attenuated less and merits investigation. For example, the noise of I_6, I_{n6}, reaches $I_{\rm out}$ according to the following transfer function:

$$\frac{I_{\rm out}}{I_{n6}}(s) = R_6 \left(\frac{g_{mf} C_f s}{C_f s + g_{mf}} \right)^2 R_7, \tag{10}$$

where the notation is the same as in (4). With the values chosen in this design, $|I_{\rm out}/I_{n6}|$ is about 0.6 and the contribution of $\overline{I_{n6}^2}$ is equal to one-eighth of the noise current of M_3, $\overline{I_{n3}^2}$, in Fig. 4(a). For the noise of I_7 and I_8 in Fig. 4(b), the contribution rises to one-fifth and one-third of $\overline{I_{n3}^2}$, respectively. Fortunately, the gain of the LNA's first stage (16 dB) suppresses these effects to an NF penalty of 0.4 dB. The penalty due to H_2 is an additional 0.3 dB. These penalties rise to 0.6 dB and 0.4 dB, respectively, for $f_1 = 3.33$ GHz.

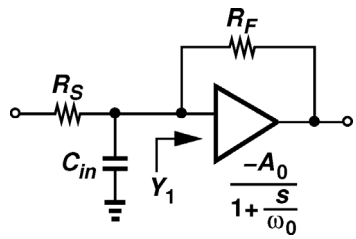

Fig. 10. Admittance of the resistive-feedback LNA.

E. S_{11} Behavior

The input matching of the feedback LNA is primarily secured by the global feedback. As explained in [4], the admittance Y_1 in Fig. 10 can be expressed as follows:

$$\frac{1}{{\rm Re}\{Y_1\}} \approx \frac{R_F\left(\omega^2 + \omega_0^2\right)}{(1 + A_0)\omega_0^2} \tag{11}$$

$${\rm Im}\{Y_1\} = \frac{-A_0\omega_0}{R_F\left(\omega^2 + \omega_0^2\right)}\omega \tag{12}$$

If the frequency of interest, ω, is much less than the core (open-loop) amplifier's -3-dB bandwidth, ω_0, then $1/{\rm Re}\{Y_1\} \approx R_F/(1 + A_0)$, which must be set equal to R_S, and ${\rm Im}\{Y_1\} \approx -(A_0/R_F\omega_0)\omega$, which must cancel $-C_{\rm in}\omega$. It follows that $R_F/A_0 \approx R_S$ if $A_0 \gg 1$ and $A_0/R_F\omega_0 = C_{\rm in}$. That is,

$$\omega_0 \cong \frac{1}{R_S C_{\rm in}}. \tag{13}$$

Such a high value of ω_0 may be difficult to achieve in the LNA. For example, for $R_S = 50\ \Omega$ and $C_{\rm in} \approx 75$ fF, ω_0 must reach $2\pi \times (42\ {\rm GHz})$. We therefore conclude that practical values of ω_0 degrade the S_{11} at high input frequencies. This phenomenon

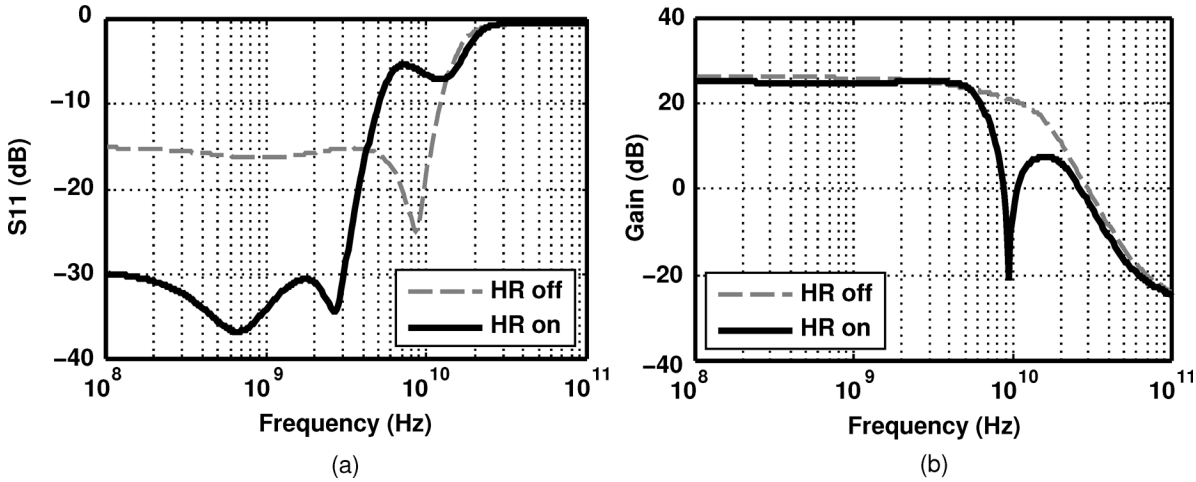

Fig. 11. LNA performance with harmonic rejection on and off ($f_1 = 3.33$ GHz): (a) S_{11}, (b) LNA gain.

occurs because a low ω_0 makes the input reactance excessively inductive.

It is possible to alleviate this issue by means of a feedback capacitor [$C_{\rm FB}$ in Fig. 9(a)]. The input admittance now emerges as

$$\frac{1}{\mathrm{Re}\{Y_1\}} \approx \frac{R_F\left(\omega^2+\omega_0^2\right)}{(1+A_0)\omega_0^2 + A_0 R_F C_{\rm FB}\omega_0\omega^2} \tag{14}$$

$$\mathrm{Im}\{Y_1\} = \frac{-A_0\omega_0 + R_F C_{\rm FB}\left[(1+A_0)\omega_0^2+\omega^2\right]}{R_F\left(\omega^2+\omega_0^2\right)}\omega \tag{15}$$

If $\omega \ll \omega_0$ and $\mathrm{Im}\{Y_1\}$ is to cancel $-C_{\rm in}\omega$, then

$$\frac{A_0}{R_F\omega_0} - (1+A_0)C_{\rm FB} = C_{\rm in} \tag{16}$$

and hence

$$\omega_0 = \frac{1}{R_S[C_{\rm in} + (1+A_0)C_{\rm FB}]}. \tag{17}$$

Thus, a lower ω_0 can still guarantee matching if $(1+A_0)C_{\rm FB}$ is large enough to satisfy the equation. Capacitor C_6 in Fig. 9(a) plays a similar role.

Fig. 11(a) plots the simulated S_{11} with harmonic rejection (HR) off and on for $f_1 = 3.33$ GHz. We observe that S_{11} remains below -20 dB up to f_1. Fig. 11(b) plots the corresponding LNA frequency response, demonstrating a rejection of about 30 dB at $3f_1$ and that the frequency response shaping devices negligibly affect the LNA performance when they are switched out.

IV. Calibration

A. Tuning Resolution

Due to the discrete tuning of the LNA, the valley of the notch in the frequency response may not exactly coincide with $3f_1$, limiting the amount of rejection. Thus, the resolution of the capacitor arrays must be chosen according to the notch "bandwidth," i.e., the frequency range around the minimum point across which the rejection is still acceptable. We further remark that the rejection must hold within the entire RF blocker *channel* bandwidth, which, in the worst case, is that of IEEE802.11a/g and equal to 20 MHz. Fig. 12(a) illustrates this situation, suggesting that the rejection at one edge of the channel may become problematic.

Fig. 12(b) plots the simulated notch "half bandwidth" defined as shown in Fig. 12(a). A conservative choice here is to ensure that the tuning step size is *less* than the notch half bandwidth. As illustrated in Fig. 12(c), this choice guarantees at least one tuning code with 20 dB of rejection. In this work, the step size varies from 5 MHz at $3f_1 = 300$ MHz to 1 GHz at $3f_1 = 10$ GHz.

B. Calibration Algorithm

An RF receiver utilizing the proposed LNA must automatically impose the capacitor settings according to the LO frequency. However, the frequency shaping varies with process and temperature, requiring that calibration be first performed for all LO frequencies and the results be stored in look-up tables.[2] In order to determine the optimum capacitor tuning code for a given f_1, we can apply to the LNA input a sinusoid at $3f_1$, measure the output amplitude, and adjust the settings so as to minimize this amplitude. But this approach demands a peak detector operating from 300 MHz to 10 GHz, a complex circuit. We propose another approach that readily lends itself to a direct-conversion receiver environment and requires minimal overhead.

As illustrated in Fig. 13, to calibrate the notch for a frequency of $3f_1$, the receiver sets the LO frequency to $3f_1$ (rather than f_1) and feeds a small fraction to the LNA. Upon traveling through the LNA and mixing with the LO, this input produces at x_I (or x_Q) a dc level proportional to the LNA output amplitude at $3f_1$. This dc value is subsequently digitized by the baseband analog-to-digital converter (ADC) and fed as an error to a least-mean-square (LMS) machine, which controls the capacitor settings. The loop now adjusts the notch frequency so as to drive the error toward zero.

[2]For calibration, a single control word is applied to all of the capacitor arrays in Fig. 9(a) simultaneously, with $H_2(s)$ using only 5 MSBs and $C_{\rm FB}$ and C_6 only 3 MSBs. The resistances and transconductances remain constant.

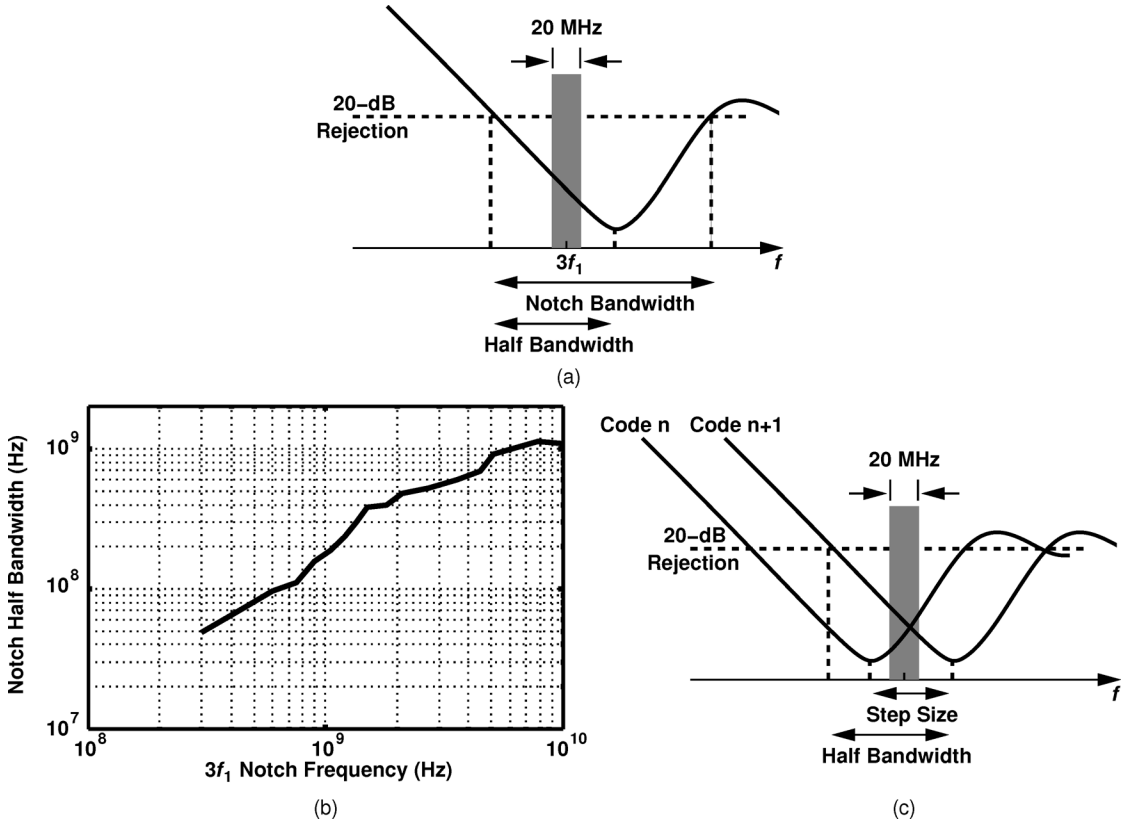

Fig. 12. (a) Definition of notch half bandwidth, (b) notch half bandwidth as a function of $3f_1$, (c) notch step size and 20-dB rejection region.

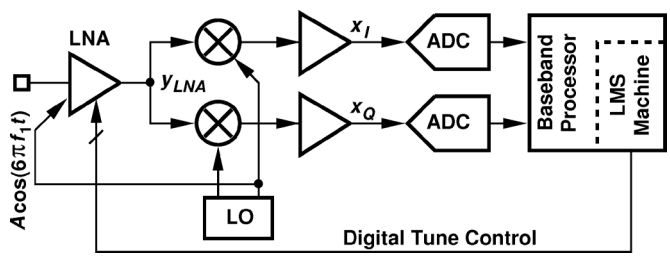

Fig. 13. Notch frequency calibration loop.

This foreground calibration entails a number of issues. First, if the phase shift through the LNA at $3f_1$ happens to be around 90°, then x_I (or x_Q) falls to zero, yielding no information and prohibiting convergence of the loop. Fortunately, $x_I^2 + x_Q^2$ can be used as the error to avoid this issue. Since the calibration can be performed at low baseband clock speeds, this operation may be implemented using compact logic.

Second, the injection port for $A\cos(6\pi f_1 t)$ in Fig. 13 merits attention as it is undesirable to disconnect the main LNA input from the antenna (or the preselect filter). Fortunately, the signal can be injected as a current (by means of a transistor) into the output node of the first or second stage in Fig. 9(a). Simulations confirm that such an injection experiences the same notch frequency as does the main input. Third, the injection level must produce a sufficiently large dc value (in the baseband) that can be digitized with reasonable resolution by the ADCs. For example, a gain of 40 dB from $y_{\rm LNA}$ to x_I in Fig. 13 would require a peak amplitude of a few millivolts at the LNA output so as to produce a dc value of several hundred millivolts at the ADC input. Such an amplitude can be readily obtained.

Fourth, the dc offset due to LO self-mixing, the mismatch between the I and Q paths, and the harmonics of the input signal must also be considered. As shown in Appendix I, these imperfections negligibly affect the calibration.

V. Experimental Results

The proposed harmonic-rejecting LNA has been fabricated in TSMC's 65-nm digital CMOS technology. Fig. 14 shows the LNA core die, which measures about 100 μm × 120 μm. Operating with a 1.2-V supply, the main path of the circuit draws 7.54 mW and the three auxiliary paths a total of 1.1 mW. The unit capacitors in the programmable arrays vary from 18 fF to 1.68 pF. The total capacitance is 16.6 pF, occupying an area of around 70 μm × 70 μm. The die is directly mounted on and bonded to a printed-circuit board, but the RF input and output pads are accessed by high-frequency probes. An on-chip serial bus controls the capacitor arrays.

Fig. 15 plots the measured LNA gain as a function of frequency for various tuning codes. The harmonic rejection is at least 20 dB for all settings. The dip in the response around 700 MHz is attributed to the resonance between the supply bond wire inductance and the on-chip bypass capacitor.

Fig. 16 plots the measured noise figure and S_{11} while harmonic rejection is off. The NF remains below 3 dB from 300 MHz to around 4 GHz. The NF rises at low frequencies due to the flicker noise of the current mirror for the 3.7-mA source in Fig. 9(a) and at high frequencies due to the roll-off in the

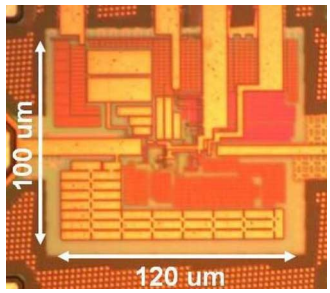

Fig. 14. LNA die photograph.

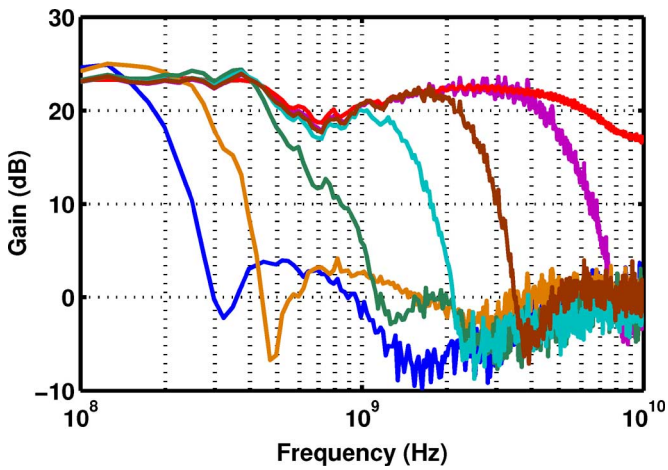

Fig. 15. Measured LNA gain for various tuning codes.

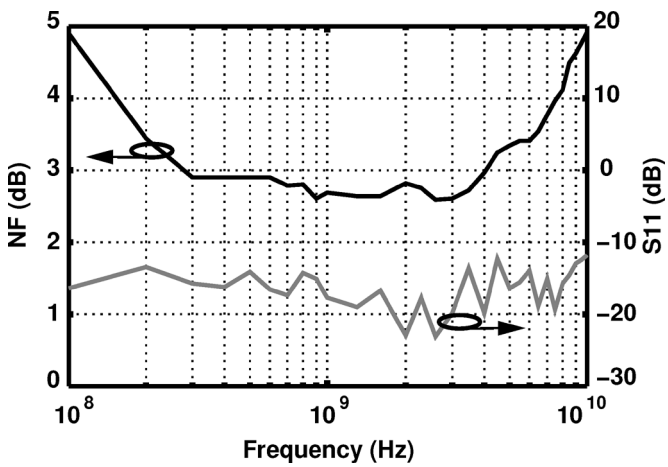

Fig. 16. Measured NF and S_{11} with harmonic rejection off.

open-loop gain. The S_{11} is less than -12 dB across the entire band.

Fig. 17 plots the measured noise figure when harmonic rejection is on and off. With harmonic rejection, the noise figure is measured at the input frequency of f_1 while the notch frequency, $3f_1$, varies from 300 MHz to 10 GHz. The worst-case NF degradation due to frequency response shaping occurs for f_1 around 750 MHz. This is because for higher values of f_1, $H_2(s)$ and $H_3(s)$ in Fig. 9(a) are turned off, contributing no noise. Fig. 18 plots the measured NF and S_{11} for this case, revealing about

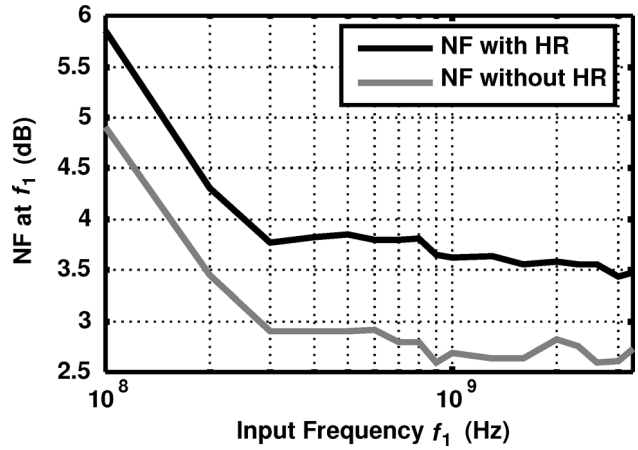

Fig. 17. Measured NF at f_1 when harmonic rejection on and off (HR remains off for $f_1 > 3.3$ GHz).

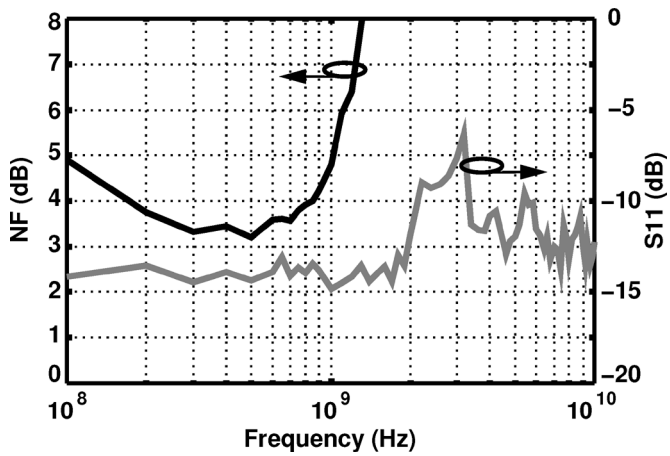

Fig. 18. Measured NF and S_{11} with harmonic rejection on ($f_1 = 750$ MHz).

1 dB of noise penalty at 750 MHz. According to measurements, S_{11} is less than -10 dB for all capacitor settings.

Fig. 19 plots the measured noise figure in the presence of an out-of-band blocker at $3f_1 = 2.2$ GHz as a function of the blocker level. As expected, for blocker levels higher than the 1-dB compression point, the circuit experiences substantial nonlinearity, exhibiting a higher NF. That is, as the blocker at the LO harmonic exceeds approximately -25 dBm, the receiver sensitivity begins to degrade. However, if a receiver sensing such a blocker level targets an LO harmonic rejection of, say, 60 dB, then it cannot operate properly with desired input levels below roughly -95 dBm anyway and hence does not require such a low noise figure.

The calibration algorithm proposed in Section IV has also been verified experimentally. In this test, the LNA input and output are connected to an RF generator and a spectrum analyzer, respectively, and the remainder of the system shown in Fig. 13 is realized in Matlab. The loop controls the notch frequency through the on-chip serial bus. Fig. 20 shows how the LMS algorithm evolves for $3f_1 = 2.4$ GHz. Plotted here is $10\log(x_I^2+x_Q^2)$ as a measure of the LNA's rejection at $3f_1$ as the calibration proceeds and the loop converges. Starting from the smallest tuning code (the highest notch frequency), the system

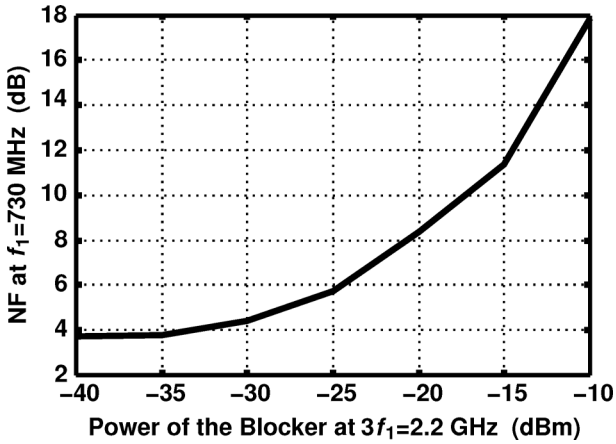

Fig. 19. Measured NF at f_1 with blocker at $3f_1$ ($f_1 = 730$ MHz).

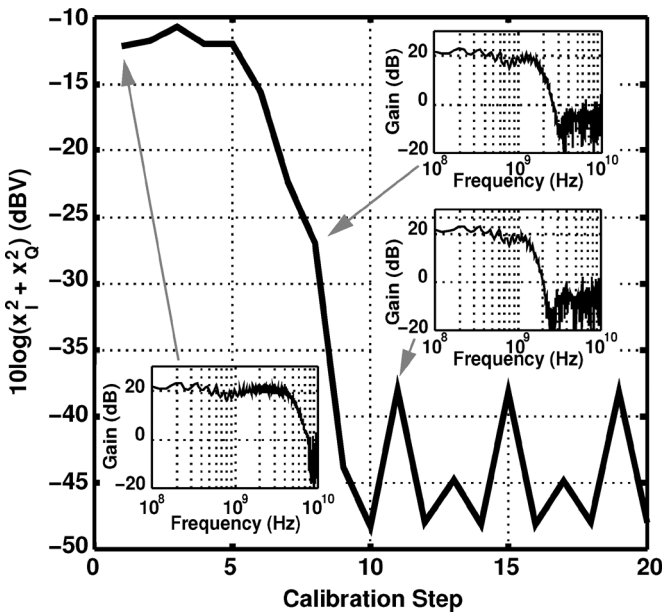

Fig. 20. Time evolution of calibration loop with a 2.4-GHz test signal.

increases the capacitances until it finds the minimum error. In this example, the loop converges after 10 iterations. The insets show the measured LNA frequency response for some of the steps to confirm the correlation between $x_I^2+x_Q^2$ and the amount of rejection. We observe that $x_I^2 + x_Q^2$ drops by 25 dB from the beginning to the maxima in the steady state, yielding a similar attenuation for $3f_1$. Rejection swings between 25 dB and 35 dB in the steady state.

It is difficult to make a fair comparison between this work and prior art as LNAs typically do not provide harmonic rejection. Nevertheless, as a reference, the design in [14] is compared with our work in Table I. We observe that, in addition to harmonic rejection, our LNA achieves nearly twice the bandwidth at 62% of the power consumption and with comparable noise figure while sacrificing linearity.

It is worth noting that the overall linearity of most RF receivers is limited by the downconversion mixers and the baseband amplifiers rather than by the LNA. For example, with an LNA gain of 24 dB and an IIP_3 of -15 dBm, the mixers must

TABLE I
LNA PERFORMANCE SUMMARY AND COMPARISON

	This Work	[14]
Frequency Band	0.1 ~ 10 GHz	0.2 ~ 5.2 GHz
Notch Frequency	0.3~10 GHz	N/A
Harmonic Rejection	> 20 dB	N/A
Supply Voltage	1.2 V	1.2 V
Power Consumption	8.64 mW	14 mW
Gain	17 ~ 24 dB	13 ~ 15.6 dB
NF (HR off, 100 MHz ~ 10 GHz)	2.59 ~ 4.92 dB	< 3.5 dB
NF (HR on, 100 MHz ~ 3.3 GHz)	3.5 ~ 5.84 dB	N/A
S_{11}	–23 ~ –11.7 dB	< –10 dB
IIP_2	1 ~ 5 dBm	> 20 dBm
IIP_3	–15 ~ –12 dBm	> 0 dBm
CMOS Technology	65 nm	65 nm

exhibit an IIP_3 of greater than $+18$ dBm if they must not degrade the receiver IP_3 by more than 0.5 dB. Such high mixer IP_3 values are extremely difficult to achieve. Thus, our LNA is unlikely to limit the receiver linearity.

VI. CONCLUSION

The problem of harmonic rejection in broadband RF receivers can be greatly relaxed if the LNA attenuates blockers at the LO harmonics. This paper presents a number of frequency response shaping techniques and a calibration algorithm that allow tuning the rejection frequency from 300 MHz to 10 GHz. A feedback LNA incorporates feedforward and unilateral Miller capacitor multiplication with sufficient resolution to attenuate blockers with channel bandwidths as much as 20 MHz. The calibration algorithm utilizes a direct-conversion receiver environment to derive a dc error and force it toward zero.

APPENDIX I

In this Appendix, we study the stability behavior of the LNA before and after harmonic-rejection frequency response shaping. In each case, a root locus is constructed with the design values shown in Fig. 9(a) while the feedback factor, β, is varied from 0 to the nominal value of 0.0526. This is accomplished by varying R_F from infinity to 900 Ω.

The open-loop LNA core exhibits a transfer function, $H_0(s)$, with three poles at 8 GHz, 17 GHz, and 26 GHz:

$$H_0(s) = -\frac{A_0}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)\left(\frac{s}{p_3}+1\right)}. \tag{18}$$

Fig. 21(a) plots the root locus as R_F varies, indicating a phase margin of 74° for $\beta = 0.0526$.

We now consider the effect of C_{FB} in Fig. 9(a). Breaking the loop at the gates of M_1 and M_2, we observe that the open-loop transfer function is now multiplied by $R_S(R_F C_{\mathrm{FB}} s + 1)/(R_S R_F C_{\mathrm{FB}} s + R_S + R_F)$, acquiring a new zero at $-1/(R_F C_{\mathrm{FB}})$ and a new pole at

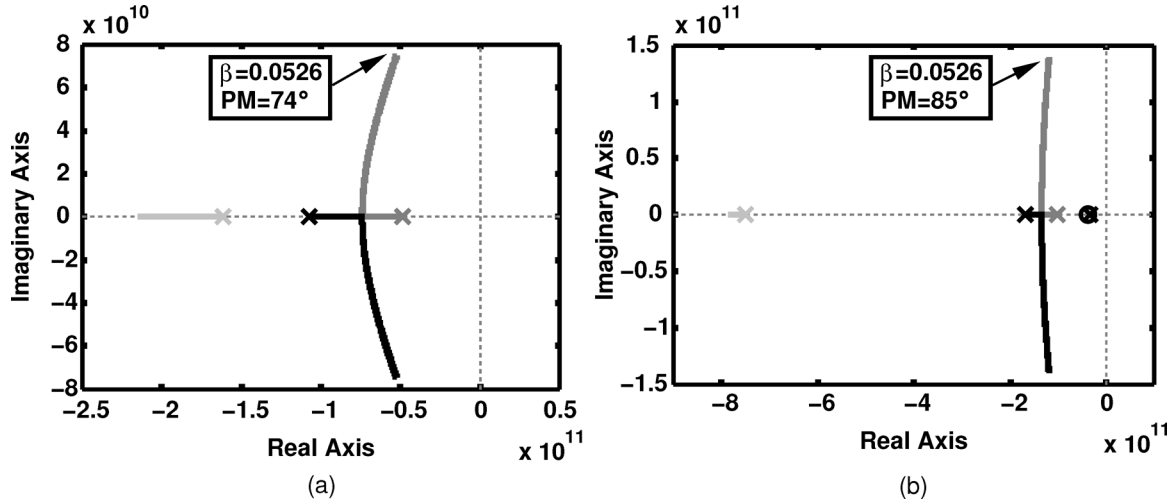

Fig. 21. Root locus of (a) $H_0(s)$, (b) $H_0(s)$ with $C_{\rm FB}$.

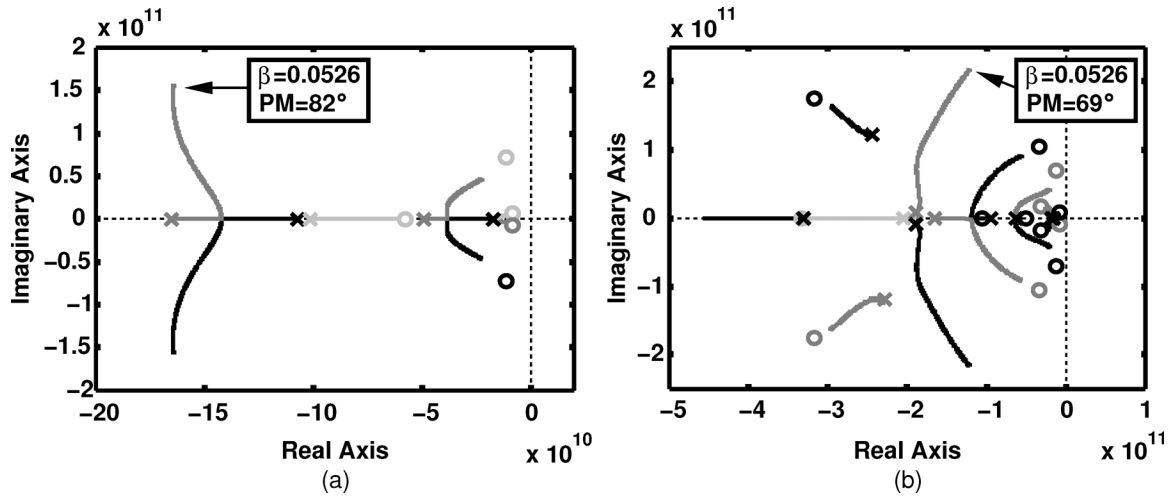

Fig. 22. Root locus of (a) $H_0(s)$ with $H_1(s)$. (b) entire LNA.

$-(R_S + R_F)/(R_S R_F C_{\rm FB})$. For example, if $C_{\rm FB} = 20$ fF, then the zero and the pole lie at 8.8 GHz and 160 GHz, respectively, with the former compensating the phase lag due to the poles and improving the stability. Fig. 21(b) plots the root locus for this case. Capacitor C_6 in Fig. 9 plays a similar role.

Let us next include the first feedforward stage, $H_1(s)$, in Fig. 9(a). The simulated root locus for $3f_1 = 1$ GHz is depicted in Fig. 22(a), revealing a phase margin of 82° for $\beta = 0.0526$. The phase margin changes negligibly because the overall feedback is relatively weak. For the entire harmonic-rejecting design, the simulated root locus emerges as shown in Fig. 22(b), still exhibiting reasonable stability.

Appendix II

This Appendix deals with the effect of receiver imperfections on the calibration algorithm described in Section IV.

The dc offsets arising from LO self-mixing add to x_I and x_Q in Fig. 13. These offsets can be measured when the LO injection into the LNA is zero and subtracted out from x_I and x_Q. This approach assumes that the LO self-mixing does not vary with the capacitor settings in the LNA, which may not be valid if all of the capacitors are first disconnected and subsequently connected one unit at a time. However, two factors ameliorate these issues. First, since simulations provide a rough knowledge of capacitor settings for a given value of $3f_1$, the calibration need not begin with all of the capacitors disconnected. Second, the baseband dc value corresponding to the LNA output amplitude is more than one order of magnitude larger than the dc offset.

Next, we study the effect of I and Q phase imbalance, $\Delta\phi$, on the calibration (The gain imbalance has little effect.) Suppose the LNA incurs a phase shift of θ at $3f_1$, producing an output given by $A_0\cos(\omega_{\rm LO}t + \theta)$. The error component driving the LMS machine is thus given by

$$\begin{aligned} x_I^2 + x_Q^2 &= \alpha A_0^2\left[\cos^2\theta + \sin^2(\theta - \Delta\phi)\right] \\ &= \alpha A_0^2\left[1 + \frac{1}{2}\cos 2\theta - \frac{1}{2}\cos(2\theta - 2\Delta\phi)\right], \end{aligned} \tag{19}$$

where α is related to the conversion gain of the mixers. In the ideal case, only A_0 varies with the tuning code, but in practice, θ does, too. With $\Delta\phi = 0$, the change in θ would not matter and $x_I^2 + x_Q^2$ would remain a monotonic function of the tuning

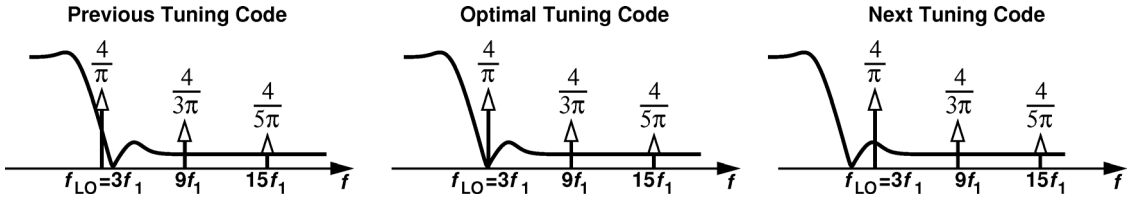

Fig. 23. Harmonics of the test signal around the optimal tuning code.

code. Equation (19) suggests that the effect of $\Delta\phi$ is maximum for $\theta = 45^\circ$ (because the slope of $\cos 2\theta$ is maximum at this angle). To avoid this issue, the worst-case change in $x_I^2 + x_Q^2$ must still be monotonic. Since A_0 and θ vary by as much as 15% and 20° for consecutive codes, we have

$$\alpha A_0^2 \left[1 + \frac{1}{2}\cos 90^\circ - \frac{1}{2}\cos(90^\circ - 2\Delta\phi)\right] < \alpha(1.15A_0)^2 \left[1 + \frac{1}{2}\cos 110^\circ - \frac{1}{2}\cos(110^\circ - 2\Delta\phi)\right], \tag{20}$$

and hence

$$\Delta\phi < 25^\circ \tag{21}$$

This upper bound on I and Q phase mismatch is fairly easy to guarantee.

The last issue relates to the harmonics of the the test signal. Since the LO waveform, especially at frequencies below a few gigahertz, may contain significant harmonics, we must determine their effect after they are mixed with the LO harmonics. Fortunately, as illustrated in Fig. 23, the harmonics of the test signal are heavily attenuated by the LNA in the vicinity of the optimal tuning code. If the tuning code is far from optimum, the sinc envelope of the harmonics still guarantees that $x_I^2 + x_Q^2$ varies monotonically with the code.

ACKNOWLEDGMENT

The authors gratefully appreciate Lincoln Laboratory for supporting this research and the TSMC University Shuttle Program for chip fabrication.

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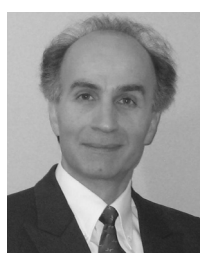

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