Substitute the following in (B1), (B2), and (B3) in Theorem 3.3: $A \to A$; $B \to BN^{T^{-1}}M^T$; $C \to MC$; $[(I-V)D] \to 2MK^{-1}N^{-1}M^T$. Now, (A) yields the following frequency domain condition which is identical to that in [17]:

$$NK^{-1} + [\frac{1}{2}[N + (z-1)S]G(z)] - \frac{1}{2}|z-1|^2 \cdot G^*(z)M^T MG(z) \geq 0, \ \forall z \in \mathcal{T}_q. \quad (4.2)$$

## V. Conclusion and Final Remarks

What may be considered the DT counterpart of positive-realness and the corresponding algebraic necessary and sufficient conditions (Theorem 3.3) have been presented. This latter result facilitates the proof of Jury-Lee criterion and can be thought of as the DT counterpart of the KY Lemma, thus successfully addressing an outstanding research problem [7-9]. It is also expected to find use in generalizing the Jury-Lee criterion and in various other areas of study, such as, network synthesis, spectral factorization, etc.

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# Impact of Distributed Gate Resistance on the Performance of MOS Devices

Behzad Razavi, Ran-Hong Yan, and Kwing F. Lee

***Abstract*—This paper describes the impact of gate resistance on cut-off frequency ($f_T$), maximum frequency of oscillation ($f_{max}$), thermal noise, and time response of wide MOS devices with deep submicron channel lengths. The value of $f_T$ is proven to be independent of gate resistance even for distributed structures. An exact relation for $f_{max}$ is derived and it is shown that, to predict $f_{max}$, thermal noise, and time response, the distributed gate resistance can be divided by a factor of 3 and lumped into a single resistor in series with the gate terminal.**

## I. Introduction

The remarkable improvement in the performance of CMOS circuits as a result of scaling has motivated extensive research on deep submicron MOS devices [1], [2]. While short channel effects such as velocity saturation and threshold voltage variation become significant for dimensions below approximately 2 $\mu$m, other nonidealities manifest themselves for only very small channel lengths. In particular, the gate resistance of a short-channel device can substantially affect its performance if the transistor width is increased to attain high current drive or large transconductance. This effect becomes especially noticeable in line drivers and output buffers used in digital systems and low-noise, high-gain amplifiers employed in analog applications, all of which typically require wide MOSFETs.

Even though the overall gate resistance can be lowered through silicidation or the use of multiple gates, these remedies have certain limitations. For example, the thickness of gate silicide must scale with channel length, thereby yielding a higher sheet resistivity for shorter devices [1]. Also, increasing the number of gates (to allow narrower devices for a given total width) tends to increase the source or drain junction capacitance and degrade circuit density.

This paper describes the impact of distributed gate resistance on four aspects of the performance of deep submicron devices: cut-off frequency ($f_T$), maximum frequency of oscillation ($f_{max}$), input-referred thermal noise, and time response. The primary goal is to quantify this impact with relatively simple expressions, thus allowing technologists and circuit designers to easily determine the maximum gate resistance that can be tolerated in a given application. The analyses are performed for an NMOS transistor whose gate is contacted only at one end, but the results can be readily applied to all field effect devices and structures with multiple gate contacts as well.

The next section of the paper analyzes the effect of gate resistance on $f_T$. Sections III to V, respectively, formulate the dependence of $f_{max}$, thermal noise, and time response on the gate resistance. Section VI summarizes the results.

## II. Cut-off Frequency

Defined as the frequency at which the short-circuit small-signal current gain of a transistor drops to unity, $f_T$ is a measure of the speed of the intrinsic device excluding its junction parasitics. If the gate resistance is modelled as a lumped resistor in series with the

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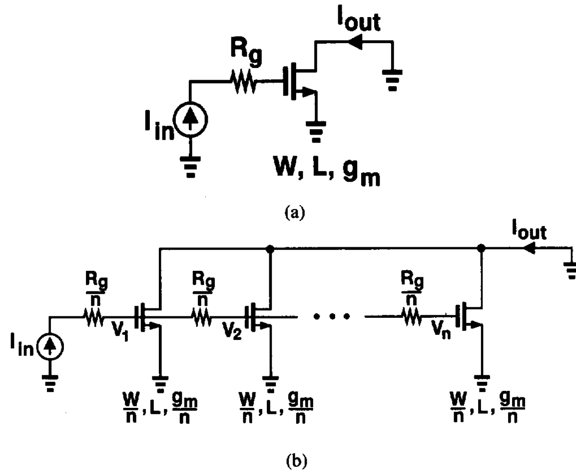



Fig. 1. Small-signal ac equivalent circuit of $f_T$ measurement configuration: (a) lumped model; (b) distributed model.

gate terminal, then it has no effect on $f_T$ because it appears in series with an ideal current source in the $f_T$ measurement configuration (Fig. 1(a)). In reality, however, the gate resistance is distributed across the width of the device, resulting in the equivalent circuit shown in Fig. 1(b). Here, the transistor is decomposed into $n$ devices, each with a width of $W/n$, a transconductance of $g_m/n$, a length of $L$, and a gate resistance of $R_g/n$. The small-signal output current of the circuit is equal to

$$I_{out} = \frac{g_m}{n}(V_1 + V_2 + \cdots + V_n) \tag{1}$$

where $I_{out}$ and $V_j$ are expressed in the frequency domain. Equation (1) represents the behavior of the actual device if $n \to \infty$. This model may suggest that, because $V_1, \ldots, V_n$ have different phase shifts, the drain currents of the unit transistors do not add in phase and hence their vector sum may drop at a rate higher than 20 dB/dec as a function of frequency. However, the following analysis shows that for a uniformly distributed MOS structure, the current gain still drops at a rate of 20 dB/dec and $f_T$ is therefore independent of the gate resistance.

The input network of the above circuit can be modelled as a uniform RC ladder, depicted in Fig. 2, with unit resistance of $R = R_g/n$ and unit capacitance of $C = c_g/n$. For small-signal operation, R and C are constant and the following equation holds:

$$I_{in} = (V_1 + V_2 + \cdots + V_n)Cs. \tag{2}$$

From (1) and (2), it follows that

$$\frac{I_{out}}{I_{in}} = \frac{g_m}{nCs} \tag{3}$$

$$= \frac{g_m}{c_g s} \tag{4}$$

indicating that the current gain is independent of $R_g$. Circuit simulations using a 32-section version of Fig. 1(b) confirm this result.

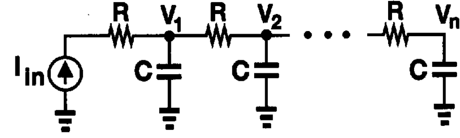



Fig. 2. Small-signal equivalent circuit of the input network of Fig. 1.

In practice, a finite gate resistance may still introduce errors in the $f_T$ measurement. For example, the effect of pad parasitics —often cancelled by subtracting the proper Y parameters— becomes more critical as $R_g$ increases, often leading to a measured $f_T$ lower than the actual value [3].

## III. Maximum Frequency of Oscillation

The frequency at which the unilateral power gain of a device drops to unity determines the maximum frequency of an oscillator ($f_{max}$) employing that device [4]. Using various approximations, several authors have calculated $f_{max}$ for MESFETs with finite gate resistance [5], [6]. However, these approximations do not take into account the distributed nature of this resistance and may also yield inaccurate results for deep submicron MOSFETs because of the substantial overlap capacitance and low output impedance observed in such devices. In this section, we derive an exact relation for $f_{max}$.

Consider the small-signal equivalent circuit shown in Fig. 3. The Y parameters of this circuit are

$$Y_{11} = \frac{(c_{gs} + c_{gd})s}{D} \tag{5}$$

$$Y_{22} = \frac{(1 + g_m R_g + R_g c_{gs} s)c_{gd} s}{D} + \frac{1}{r_o} + c_{db} s \tag{6}$$

$$Y_{12} = -\frac{c_{gd} s}{D} \tag{7}$$

$$Y_{21} = \frac{-c_{gd} s + g_m}{D} \tag{8}$$

where $D = R_g(c_{gs} + c_{gd})s + 1$. The unilateral gain, U, is equal to

$$U = \frac{|Y_{12} - Y_{21}|^2}{4(ReY_{11}ReY_{22} - ReY_{12}ReY_{21})}, \tag{9}$$

which, from (5) to (8), assumes the form shown at the bottom of the page in (10). To calculate $\omega_{max}(= 2\pi f_{max})$, we equate (10) to unity, thus obtaining

$$a\omega_{max}^4 + b\omega_{max}^2 + c = 0 \tag{11}$$

where

$$a = 4R_g^3(c_{gs} + c_{gd})^2\left[c_{gd}^2(1 + g_m r_o) + c_{gs}^2 + (2 + g_m r_o)c_{gd}c_{gs}\right] \tag{12}$$

$$b = R_g(c_{gs} + c_{gd})\left[(c_{gs} + c_{gd})(4 - g_m^2 r_o R_g) + 4g_m r_o c_{gd}\right] \tag{13}$$

$$c = -g_m^2 r_o. \tag{14}$$

Equation (11) can be solved for $\omega_{max}^2$, and hence $\omega_{max}$, with any set of device parameters.

It is possible to find a simpler expression for $\omega_{max}$ if typical device parameters are considered. For example, a 6$\mu$m/0.15$\mu$m NMOS

$$U = \frac{g_m^2 r_o}{4R_g(c_{gs} + c_{gd})\omega^2} \cdot \frac{1 + R_g^2(c_{gs} + c_{gd})^2\omega^2}{R_g^2(c_{gs} + c_{gd})[c_{gd}^2(1 + g_m r_o) + c_{gs}^2 + (2 + g_m r_o)c_{gs}c_{gd}]\omega^2 + c_{gs} + (1 + g_m r_o)c_{gd}}. \tag{10}$$

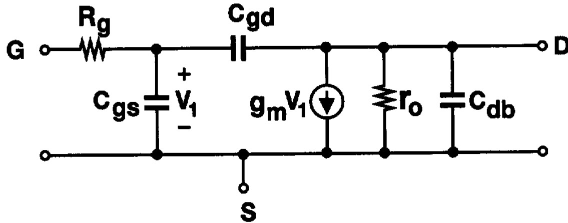



Fig. 3. Small-signal model of a MOSFET.

transistor with 40-Å gate oxide typically exhibits the following parameter values: $R_g = 150\Omega$, $g_m = 0.003\Omega^{-1}$, $r_o = 2000\Omega$, $c_{gs} = 9$ fF, and $c_{gd} = 2.4$ fF, which, from (11), yield an $f_{max}$ of approximately 56 GHz. With these values, we note that

$$R_g^2(c_{gs} + c_{gd})^2\omega_{max}^2 \ll 1 \tag{15}$$

and

$$R_g^2(c_{gs} + c_{gd})[c_{gd}^2(1 + g_m r_o) + c_{gs}^2 + (2 + g_m r_o)c_{gs}c_{gd}]\omega_{max}^2 \ll c_{gs} + (1 + g_m r_o)c_{gd}. \tag{16}$$

Thus, (10) reduces to

$$U(\omega = \omega_{max}) \approx \frac{g_m^2 r_o}{4R_g(c_{gs} + c_{gd})[c_{gs} + (1 + g_m r_o)c_{gd}]\omega_{max}^2} \tag{17}$$

and hence

$$\omega_{max}^2 \approx \frac{g_m^2 r_o}{4R_g(c_{gs} + c_{gd})[c_{gs} + (1 + g_m r_o)c_{gd}]}. \tag{18}$$

This result agrees with that obtained from (11) with less than 5% error. Also note that for $r_o = \infty$ or $c_{gd} = 0$, (18) reduces to expressions reported previously [7], [4].

Equation (18) furthermore reveals some trends as the gate resistance or the device width vary. First, it indicates that if the sheet resistivity of the gate material varies while other parameters remain constant, then

$$\omega_{max} \propto \frac{1}{\sqrt{R_g}}. \tag{19}$$

Second, it shows that if $g_m, R_g, c_{gs}$, and $c_{gd}$ scale linearly with the width ($W$) and $g_m r_o$ is constant, then

$$\omega_{max} \propto \frac{1}{W}. \tag{20}$$

Equations (19) and (20) are of course well known [7], but our formulation confirms them with greater accuracy.

Note that the above analysis assumes the gate resistance can be lumped into a single resistor in series with the gate terminal. For a distributed model, the mathematics becomes intractable, but it is possible to use simulations to gain more insight. To this end, for the equivalent circuit of Fig. 3, we can perform an ac analysis in SPICE and utilize the postprocessor Nutmeg to plot $U$ from (9) versus frequency. As the number of sections in the distributed model increases, we can see how $f_{max}$ deviates from its lumped-model value and what value it approaches as the number of sections becomes large.

Fig. 4 plots the resulting values for $f_{max}$ as the number of sections in the equivalent circuit varies from 1 to 64. (The simulations use the typical MOS device parameters mentioned above.) This plot yields two important results. First, the $f_{max}$ of the lumped model (one section) closely agrees with that obtained from (18). Second, for a distributed model, the effect of $R_g$ is divided by 3, i.e., Equation (18) predicts $\omega_{max}$ accurately if $R_g$ is replaced with $R_g/3$.

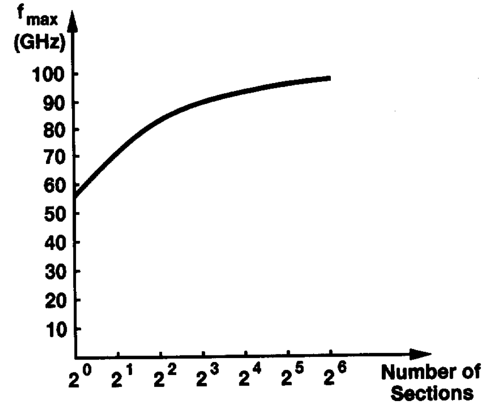



Fig. 4. Simulated value of $f_{max}$ versus number of sections in distributed model.

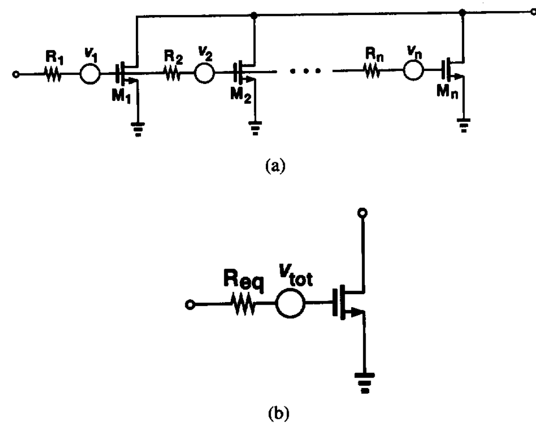



Fig. 5. Circuit for calculating thermal noise generated by gate resistance: (a) distributed model; (b) lumped model.

## IV. Thermal Noise

The gate resistance of a MOSFET directly contributes to the input-referred thermal noise. For a uniformly distributed MOS structure, it is possible to find an equivalent lumped resistance that can be placed in series with the gate terminal to represent the thermal noise of the gate material. In this section, we calculate this resistance.

Consider the distributed model shown in Fig. 5(a), where the thermal noise of each resistor is modelled as a series voltage source. The drain noise current arises from both the gate resistance and the channel resistance. To calculate the equivalent lumped resistance, we determine the total drain noise current *due to only the gate resistance* and refer it back to the gate terminal of a lumped MOSFET as a voltage source (Fig. 5(b)).

The drain noise current of $M_1$ resulting from the gate resistance is

$$i_1 = g_{m1}v_1 \tag{21}$$

where $v_1$ is the noise voltage of $R_1$. Similarly,

$$i_2 = g_{m2}(v_1 + v_2) \tag{22}$$

where $v_2$ is the noise voltage of $R_2$. Thus, for transistor $M_j$, we have

$$i_j = g_{mj}(v_1 + v_2 + \cdots + v_j) \tag{23}$$

and the total drain noise current is

$$i_{tot} = i_1 + i_2 + \cdots + i_n \tag{24}$$
$$= g_{m1}v_1 + g_{m2}(v_1 + v_2) + \cdots + g_{mn}(v_1 + v_2 + \cdots + v_n). \tag{25}$$

If $g_{m1} = g_{m2} = \cdots = g_{mn} = g_m/n$, then

$$i_{tot} = \frac{g_m}{n}[nv_1 + (n-1)v_2 + \cdots + v_n]. \tag{26}$$

Assuming $v_1, \ldots, v_n$ are uncorrelated, we can express the mean square noise current as

$$\overline{i_{tot}^2} = \frac{g_m^2}{n^2}[n^2\overline{v_1^2} + (n-1)^2\overline{v_n^2} + \cdots + \overline{v_n^2}]. \tag{27}$$

If $R_1 = R_2 = \cdots R_n = R_g/n$, then $\overline{v_1^2} = \overline{v_2^2} = \cdots = \overline{v_n^2} = 4kTBR_g/n$, where $k$ is Boltzmann constant, $T$ is absolute temperature, and $B$ is the bandwidth. Equation (27) then reduces to

$$\overline{i_{tot}^2} = \frac{g_m^2}{n^2}\frac{4kTBR_g}{n}[n^2 + (n-1)^2 + \cdots + 1] \tag{28}$$
$$= g_m^2(4kTB)R_g\frac{n(n+1)(2n+1)}{6n^3}. \tag{29}$$

As $n \to \infty$,

$$\overline{i_{tot}^2} = g_m^2(4kTB\frac{R_g}{3}) \tag{30}$$

which can be referred to the input as

$$\overline{v_{tot}^2} = \frac{\overline{i_{tot}^2}}{g_m^2} \tag{31}$$
$$= 4kTB\frac{R_g}{3}. \tag{32}$$

This relation indicates that, for noise calculation purposes, the distributed structure of Fig. 5(a) can be replaced with a single MOS device of transconductance $g_m$ and a lumped gate resistance of $R_g/3$ (Fig. 5(b)). Circuit simulations with $n = 32$ confirm this result.

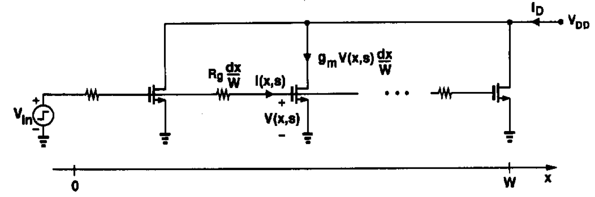
In addition to $v_{tot}$ given by (32), channel resistance of the transistor also contributes to the overall thermal noise. Therefore, the relative significance of the gate resistance can be determined by comparing $R_g/3$ with $1/g_m$.

## V. Transient Response

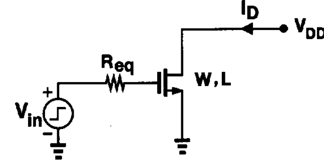
The gate resistance of a MOSFET together with its gate-source and gate-drain capacitance introduces a time constant that may be significant if the device is driven by a low output impedance circuit. As a first-order approximation, this time constant is equal to $R_gC_{in}$, where $C_{in}$ is the average input capacitance. However, in the distributed model of Fig. 6(a), the transistors closer to the input terminal see less gate resistance than those near the end; thus, the overall gate time constant is smaller than $R_gC_{in}$. In this section, we obtain an equivalent lumped circuit (Fig. 6(b)) that exhibits approximately the same transient response as the distributed model.

Consider the distributed circuit of Fig. 6(a), where an infinitesimal section of the transistor has a width of $\mathrm{d}x$, gate resistance of $R_g\mathrm{d}x/W$, input capacitance of $c_g\mathrm{d}x/W$, transconductance of $g_m\mathrm{d}x/W$, and drain current of $g_mV(x,s)\mathrm{d}x/W$. For this circuit, we have

$$\frac{\partial V(x,s)}{\partial x} = \frac{R_g}{W}I(x,s) \tag{33}$$
$$\frac{\partial I(x,s)}{\partial x} = \frac{c_gs}{W}V(x,s) \tag{34}$$



(a)



(b)

Fig. 6. Circuit for analyzing time response of an NMOS transistor (a) distributed model, (b) lumped model.

subject to boundary conditions $V(x=0,s) = V_{in}(s)$ and $I(x = W, s) = 0$. Solving these equations for $V(x,s)$ yields

$$V(x,s) = -V_{in}(s)\tanh\sqrt{R_gc_gs}\sinh(\sqrt{R_gc_gs}\frac{x}{W}) + V_{in}(s)\cosh(\sqrt{R_gc_gs}\frac{x}{W}). \tag{35}$$

The total drain current is given by

$$I_D(s) = \int_{x=0}^{W}\frac{g_m}{W}V(x,s)\mathrm{d}x, \tag{36}$$

which, from (35), is equal to

$$I_D(s) = g_m\frac{\tanh\sqrt{R_gc_gs}}{\sqrt{R_gc_gs}}V_{in}(s). \tag{37}$$

Equation (37) can be simplified if we assume $R_gc_gs \ll 1$. As $1/R_gc_g$ is typically greater than 200 GHz, this assumption is valid for most circuit applications in current technology. Since for small $\epsilon$,

$$\tanh\epsilon \approx \epsilon - \frac{\epsilon^3}{3} \tag{38}$$
$$\approx \frac{\epsilon}{1+\frac{\epsilon^2}{3}} \tag{39}$$

(37) reduces to

$$I_D(s) \approx \frac{g_m}{1+\frac{R_gc_gs}{3}}V_{in}(s). \tag{40}$$

Note that the error resulting from this approximation is less than 2% even for $R_gc_gs = 1$. Equation (40) indicates that the distributed circuit of Fig. 6(a) can be modelled with the lumped circuit of Fig. 6(b) if $R_{eq} = R_g/3$. Circuit simulations using a 32-section version of Fig. 6(a) confirm this result.

It follows from the above discussion that the gate resistance influences the device time response if the output impedance of the circuit preceding the device is comparable with $R_g/3$.

It should be mentioned that the $f_T$ measurement configuration depicted in Fig. 1(b) and characterized by (1) and (2) can also be described by (33) and (34) with boundary conditions $I(x=0,s) = I_{in}(s)$ and $I(x = W, s) = 0$, leading to the same conclusion as that reached in Section II.

## VI. Conclusion

The distributed gate resistance of wide MOS devices becomes increasingly critical as channel lengths are scaled to deep submicron dimensions. The impact of this resistance on cut-off frequency, maximum frequency of oscillation, thermal noise, and time response of field effect devices has been studied and quantified. It is shown that the cut-off frequency is independent of the gate resistance even for distributed structures. It is also demonstrated that, for $f_{max}$ calculation and thermal noise and transient analyses, the distributed gate resistance can be divided by 3 and lumped into a single resistor in series with the gate terminal.

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# Chaos, Torus and Synchronization from Three Coupled Relaxation Oscillators

Toshimichi Saito and Yoshiaki Matsumoto

***Abstract*— This paper analyzes fundamental phenomena from three coupled relaxation oscillators. The system nonlinearity is a piecewise linear hysteresis comparator and we can explicitly calculate the return map and its Lyapunov exponents. Then we clarify generation of chaos, 2-torus, 3-torus and various kinds of synchronizations. Also, a rough bifurcation diagram is given. It indicates that 3-torus is popular for weak coupling and chaos is popular for relatively strong coupling. Some of the phenomena are confirmed by laboratory measurements.**

## I. Introduction

Coupled oscillators are important to approach rich dynamics from large scale circuits and systems. They can exhibit various kinds of chaos, tori, periodicities and related bifurcations [1]-[6]. Also, they deeply relate to artificial neural systems [7], [8], chaotic secure communication systems [9], [10] and so on. For continuous-time coupled oscillators [2]-[5], [9], there are some interesting results on fundamental synchronization phenomena. However, more complicated phenomena (e.g. chaos) have begun to be analyzed experimentally for up to four coupled oscillators [4], [5], [9]. Systematic analysis of dynamics from N coupled oscillators are very hard because of complex nonlinearity. We should focus on some simple three coupled oscillators and try to analyze its global dynamics.

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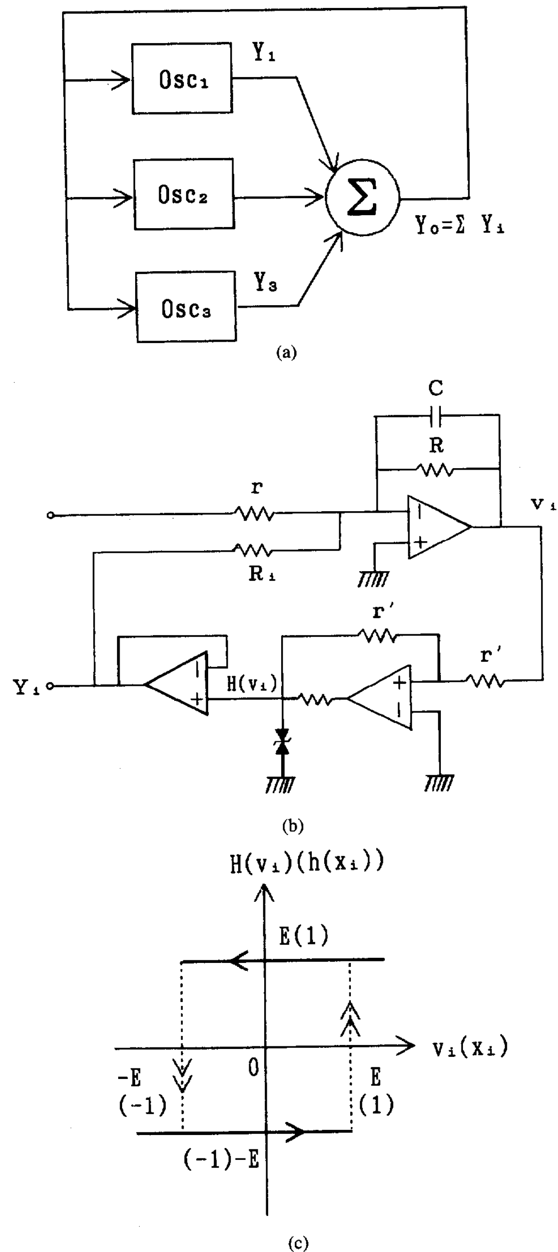


Fig. 1 Simulation circuit: (a) Three coupled oscillators, (b) element oscillator, (c) hysteresis characteristic.

This paper analyzes continuous-time three coupled relaxation oscillators. If the oscillator number is enlarged and if parameters are adjusted to have some equilibria, the system can operate as an efficient associative memory [8]. Then we consider the case where the three oscillators have different self-running frequencies and the cross coupling is uniform. Since the system nonlinear elements are

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