A Receiver Architecture for Dual-Antenna Systems

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***Abstract*—The signals received by two antennas can be processed by a single time-shared receiver but only in the absence of interferers and channel-select filters. A low-IF receiver architecture is introduced that translates two antenna signals to positive and negative frequencies in the complex domain, reducing the number of baseband A/D converters by a factor of two. A dual-receiver prototype designed and fabricated in 0.18-μm CMOS technology provides a sensitivity of -72 dBm with an EVM of -25 dB for 64 QAM signals while drawing 60.2 mW from a 1.8-V supply.**

***Index Terms*—CMOS receivers, IEEE 802.11a, low-IF, MIMO, orthogonal frequency division multiplexing (OFDM), wireless local area network (WLAN).**

I. Introduction

THE USE OF multiple antennas and receivers can substantially boost the performance in wireless communication. For example, antenna diversity and beamforming techniques improve the link budget considerably. Moreover, multiple-input-multiple-output (MIMO) systems can raise the channel capacity in the presence of multipath fading and have been adopted by the IEEE 802.11n standard. Since the brute force method of duplicating the entire receive path for each additional antenna entails a significant area and power penalty, it is desirable to share as much of the receiver among the antennas as possible.

In this paper, it is shown that receiver multiplexing faces serious issues in the presence of interferers and/or shared channel-select filters. A two-antenna receiver architecture is then described that halves the number of baseband analog-to-digital converters (ADCs) while requiring a single frequency synthesizer. Designed for the 5-GHz band in 0.18-μm CMOS technology, the receiver achieves a sensitivity of -72 dBm for 64 QAM signals while consuming 30.1 mW per channel [1].

Section II of the paper deals with receiver multiplexing issues. Section III introduces the dual-receiver architecture and Section IV describes the design of the building blocks. Section V presents the experimental results.

II. Receiver Multiplexing

Recent work has demonstrated the use of two independent receive paths driven by a single synthesizer to process two antenna signals [2]. Realized in SiGe BiCMOS technology, the two receive chains provide a noise figure of 7.5 dB in the 5-GHz band while drawing about 880 mW [2]. Also, the work in [3] incorporates four independent receivers while achieving a noise figure of 15 dB and consuming 45 mW per receiver (with no channel-selection filtering). The design in [4] employs two receivers in 90-nm CMOS technology while draining 170 mW per receiver [including local oscillator (LO) generation circuitry].

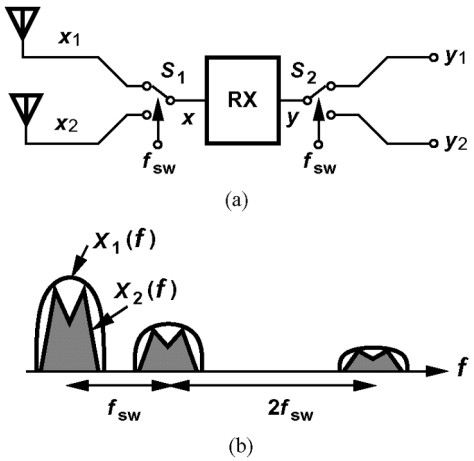

Fig. 1. Sharing the entire receive path between two antennas.

In order to process two antenna signals having the same carrier frequency, one may naturally conceive the arrangement shown in Fig. 1(a), where a single receive (RX) path (including RF and baseband sections) is shared[1] and the switching is performed at a rate of at least the RF channel bandwidth, $f_{\rm ch}$, to avoid aliasing. The receiver input signal, $x(t)$, can be expressed as the sum of two terms:

$$x(t) = x_1(t)p_1(t) + x_2(t)p_2(t) \tag{1}$$

where $p_1(t)$ is equal to one when S_1 is at the top antenna and zero when S_1 is at the bottom antenna. The function $p_2(t)$ is the logical complement of $p_1(t)$. Defining the function $Sq(t)$ as a periodic waveform toggling between $+1$ and -1 we can express $p_1(t)$ and $p_2(t)$ as

$$p_1(t) = \frac{1}{2} + \frac{1}{2}Sq(t) \tag{2}$$

$$p_2(t) = \frac{1}{2} - \frac{1}{2}Sq(t) \tag{3}$$

and hence $x(t)$ as

$$x(t) = x_1(t)\left[\frac{1}{2} + \frac{1}{2}Sq(t)\right] + x_2(t)[\frac{1}{2} - \frac{1}{2}Sq(t)]. \tag{4}$$

In the frequency domain, the antenna signals $X_1(f)$ and $X_2(f)$ are convolved with the spectra of $p_1(t)$ and $p_2(t)$, respectively, and summed together. This superimposes and distributes $X_1(f)$ and $X_2(f)$ over the harmonics of $Sq(t)$ [Fig. 1(b)]. Thus, we require that the switching rate $f_{\rm sw} > f_{\rm ch}$.

[1]In practice, the antennas may be immediately followed by low-noise amplifiers (LNAs) to suppress the noise due to switching.

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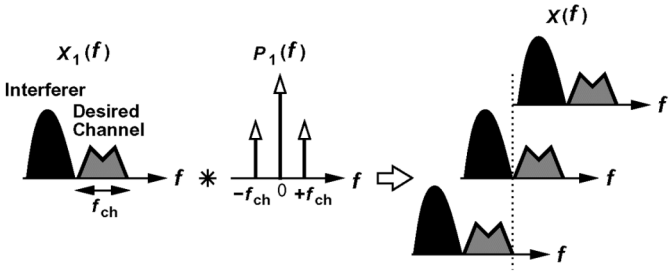

Fig. 2. Receiver input spectrum when signal from the first antenna is accompanied by a large interferer.

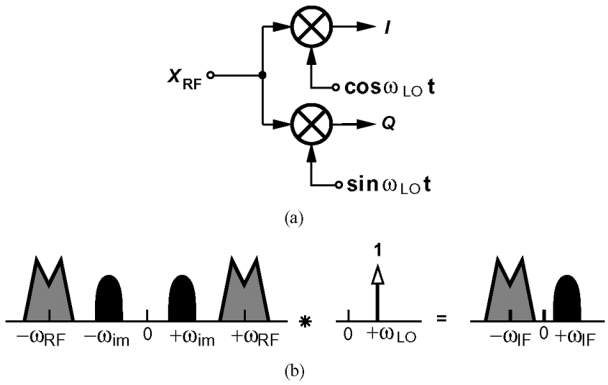

Fig. 3. Quadrature mixer. (a) Block diagram. (b) Frequency domain operation.

A. Ideal Case: No Interferers, No Filtering

Consider an ideal case where no interferers exist and no filtering is performed in the receive path. Allowing for frequency translation in the receiver, we consider the output y "equivalent" to the input and write

$$\begin{aligned} y(t) &\equiv x(t) \\ &= x_1(t)\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right]+x_2(t)\left[\frac{1}{2}-\frac{1}{2}Sq(t)\right]. \quad (5) \end{aligned}$$

As evident from Fig. 1(a), the recovered signal from the first antenna, $y_1(t)$, is obtained by multiplying the receiver output by the switching function $p_1(t)$:

$$\begin{aligned} y_1(t) &= y(t)p_1(t) \\ &= \frac{1}{4}[1+Sq(t)]^2x_1(t)+\frac{1}{4}[1-Sq^2(t)]x_2(t). \quad (6) \end{aligned}$$

Similarly,

$$\begin{aligned} y_2(t) &= y(t)p_2(t) \\ &= \frac{1}{4}[1-Sq^2(t)]x_1(t)+\frac{1}{4}[1-Sq(t)]^2x_2(t). \quad (7) \end{aligned}$$

Since no filtering is performed in the receive path, all harmonics of $Sq(t)$ are preserved and hence $Sq^2(t)=1$. That is, y_1 and y_2 remain free from corruption by x_2 and x_1, respectively.

B. Effect of Interferers

Suppose for simplicity that $x_2(t) = 0$ and hence $x(t) = x_1(t)[1+Sq(t)]/2$. Also, assume $f_{\rm sw} = f_{\rm ch}$ and the desired signal from the first antenna, $x_1(t)$, is accompanied by a large interferer in the adjacent channel (Fig. 2). In the frequency domain, the signal spectrum is convolved with impulses that are apart by the RF channel bandwidth, yielding the three spectra shown on the right. In other words, $X(f)$ is corrupted by the shifted versions of the interferer even before entering the common receive path.

The above observation suggests that, for any switching rate, there exists an interferer that corrupts the desired signal. In principle, out-of-band interferers are suppressed by the band-select filters following the antennas, but those within the band persist, dictating a switching rate greater than the total receive bandwidth!

In the presence of interferers, channel-select filtering becomes necessary. It is shown in Appendix I that such filtering creates substantial "cross-interference" between the two received signals if the switching rate is chosen to avoid the above aliasing effects.

In summary, our analysis in this section suggests that receive path multiplexing is possible only if it excludes channel-select filtering. Since each antenna typically requires a dedicated LNA, only the downconversion mixers and possibly baseband variable-gain amplifiers can be time-shared—provided they contain no narrowband filtering. In fact, since the mixer outputs typically interface with the baseband filters, time-sharing the mixers may not be possible.

III. Proposed Receiver Architecture

The architecture proposed here processes complex signals in positive and negative frequencies. We therefore define a notation that helps describe the architecture. Consider the quadrature mixer shown in Fig. 3(a). We view the two phases of the local oscillator as the real and imaginary parts of a complex exponential, $\exp(j\omega_{\rm LO}t)=\cos\omega_{\rm LO}t+j\sin\omega_{\rm LO}t$, whose spectrum is one-sided and contains one impulse at only $+\omega_{\rm LO}$. Similarly, we express the two downconverted components as one complex signal, $x_{\rm RF}\cos\omega_{\rm LO}t+jx_{\rm RF}\sin\omega_{\rm LO}t$. The resulting spectra are depicted in Fig. 3(b), where $\omega_{\rm IF}$ denotes the intermediate frequency (IF).

The principle introduced in this paper is based on downconverting the two antenna signals in a low-IF architecture such that one appears in the positive frequency range and the other in the negative frequency range, thus allowing their direct summation and hence digitization by only one pair of ADCs. Fig. 4 depicts the dual-receiver architecture. Each path consists of a low-noise amplifier (LNA), quadrature mixers, a complex channel-select filter, and a voltage summer. The mixers are driven by the same LO frequency, except that one of the quadrature phases is negated for the top path. Also, note that the complex bandpass filters (BPFs) operate on different frequency polarities.

The architecture processes the signals as follows. In the top path, quadrature mixing yields a complex signal containing X_1 at $+\omega_{\rm IF}$ and its image ($\approx$adjacent channel) at $-\omega_{\rm IF}$. The complex BPF thus suppresses the adjacent channel while maintaining X_1 at $+\omega_{\rm IF}$. The bottom path, on the other hand, translates X_2 to $-\omega_{\rm IF}$ and performs the filtration such that the image, located at $+\omega_{\rm IF}$, is removed. Now, I_1 and Q_1 contain only X_1 at $+\omega_{\rm IF}$, and I_2 and Q_2 contain only X_2 at $-\omega_{\rm IF}$.

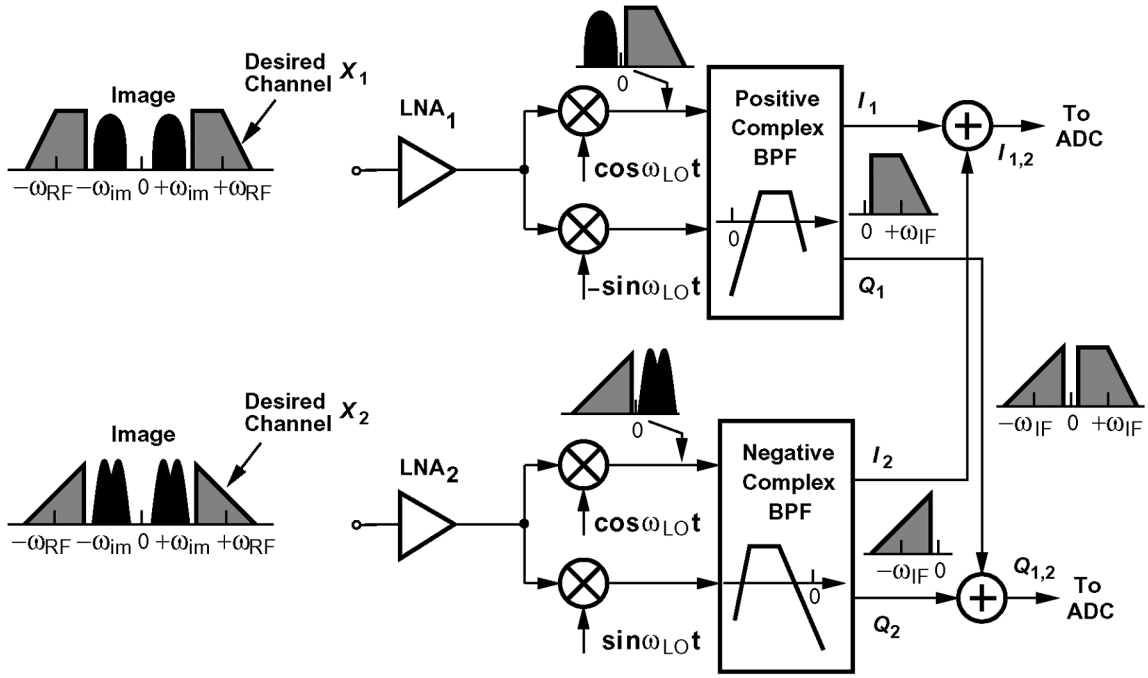

Fig. 4. Proposed dual-antenna receiver architecture.

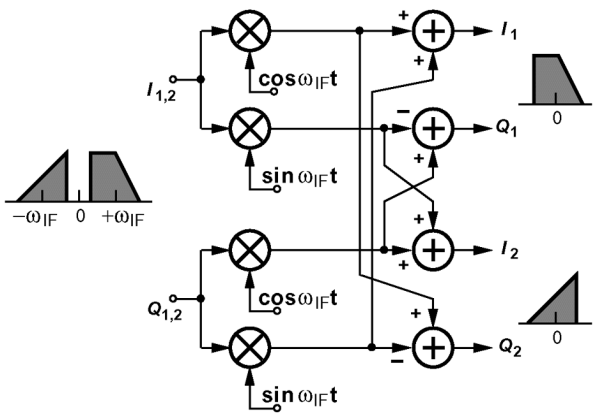

Fig. 5. Baseband processing to recover $X_1 = [I_1\ Q_1]$ and $X_2 = [I_2\ Q_2]$.

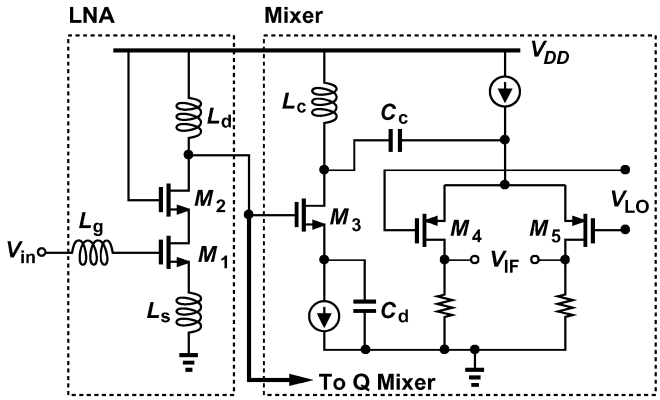

Fig. 6. Receiver front end.

Summation of these voltages halves the number of signals to be digitized while introducing no corruption.

After digitization, the two sets of quadrature signals corresponding to X_1 and X_2 can be reconstructed in the digital domain as shown in Fig. 5. In this work, IF = 13 MHz (rather than 10 MHz) to minimize the effect of flicker noise in the baseband.

As with other low-IF receivers [5], the image rejection ratio of this architecture is limited by the gain and phase mismatches in the quadrature paths. Thus, if the anticipated adjacent channel level is high, some means of I/Q calibration may be necessary [6].[2]

The finite image rejection in the downconversion process of Fig. 4 places a small fraction of X_1 at $-\omega_{\rm IF}$ and a small fraction of X_2 at $+\omega_{\rm IF}$. As a result, some "coupling" arises between the two signals. However, as shown in [9], coupling factors as high as -20 dB between MIMO receivers are benign. Thus, with typical raw image rejection ratios of 30 dB, this effect negligibly degrades the performance.

Another source of corruption relates to the mismatches within the summers in Fig. 4. While the digital reconstruction in Fig. 5 assumes equal weights for all components, analog mismatches in the I_1 and I_2 (or Q_1 and Q_2) paths in Fig. 4 alter their weightings, thus introducing an error. Nonetheless, since the summers employ resistors having mismatches below 0.5%, this "crosstalk" remains negligible.

In comparsion with two direct-conversion receivers, the proposed architecture reduces the area occupied by ADCs and offers the generic advantages of low-IF reception, e.g., ease of dc offset removal and lower susceptibility to flicker noise. The power dissipation is expected to be comparable in both cases.

While reducing the number of ADCs by a factor of two, the proposed architecture still duplicates much of the receive path, potentially consuming a high power. In the next section, we present RF and baseband circuit techniques that lead to a power dissipation of 30.1 mW per receiver—60% less than that of prior IEEE802.11a receivers in 0.18-μm CMOS technology [10].

[2]It is possible to add the I and Q outputs of a low-IF receiver in the analog domain to save on ADC, but at the cost of prohibiting further image rejection in the digital domain. For example, the low-IF receivers in [7] and [8] exploit both I and Q outputs to perform image rejection.

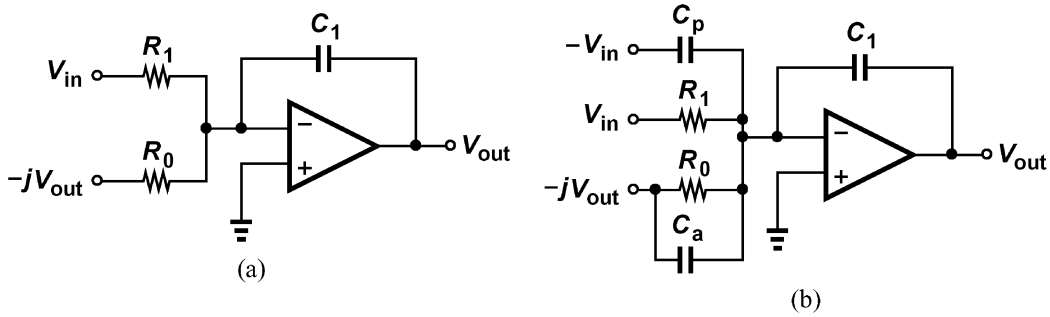

Fig. 7 (a) Conventional and (b) proposed integrator topologies for I block.

IV. Building Blocks

A. Receiver Front End

Fig. 6 depicts the front end of each receive path. A cascode LNA with a voltage gain of 29 dB is followed by two quadrature mixers. For simplicity, only the I channel mixer is shown. Each mixer incorporates a voltage-to-current converter, M_3, with capacitive degeneration so as to improve the linearity without degrading the noise figure. The high-pass network L_c and C_c also rejects low-frequency beat components that arise from even-order distortion in the LNA and in M_3, thus raising the IP_2. To provide an output common-mode level compatible with the subsequent filter and as well as reduce $1/f$ noise, the switching pair employs pMOS devices.

Simulations indicate that the front end exhibits a noise figure of 4.5 dB, a voltage gain of 32 dB and an IIP_3 of -23 dBm while consuming 19.1 mW from a 1.8-V supply.

B. Complex Bandpass Filter

In order to perform adequate channel selection with IEEE 802.11a adjacent channel specifications, a Chebyshev filter of fifth order is necessary. With an IF of 13 MHz and 1.7-MHz unused guard bands on each side of the channel, the filter passband must span 4.7 MHz to 21.3 MHz. This work incorporates an op amp-RC realization.

The principal challenge in the design of the complex bandpass filter (BPF) stems from the large number of op amps that must provide a broad bandwidth while driving heavy capacitive and resistive loads. The fifth-order complex I/Q BPF requires 10 integrators, and hence 20 op amps for the dual-antenna receiver. Thus, the op amp gain, bandwidth, and noise requirements must be quantified carefully to minimize the power dissipation.

Since the upper corner of the BPF lies at 21.3 MHz, we must first determine the minimum acceptable op amp bandwidth that provides negligible peaking in the filter response at this frequency. The peaking in the passband of most common integrator-based filters can be estimated as [11]

$$\Delta A_{\max} < 13.65N\frac{f_2}{\mathrm{BW}}\frac{1}{Q_I}\ \mathrm{dB} \tag{8}$$

where N denotes the order of the filter, f_2 the upper corner frequency, BW the bandwidth, and Q_I the integrator quality factor. The quality factor itself is a function of frequency and is given by

$$Q_I = \frac{\omega_t}{\omega}, \text{for } \omega \gg \omega_b \tag{9}$$

where ω_t and ω_b are the unity-gain and the -3-dB bandwidths of the op amp, respectively. It follows that, if $\Delta A_{\max} \leq 0.5$ dB, and $\mathrm{BW} = 16.6$ MHz, Q_I must exceed 175 at 21.3 MHz, requiring a unity-gain bandwidth of 3.7 GHz.

In addition to the required bandwidth, the first integrator in the filter must also exhibit negligible noise. With a front-end gain of 32 dB, the input resistors of this integrator must remain below roughly 1.7 kΩ, dictating an integrating capacitor of 1 pF to establish the necessary filter characteristic. An op amp having a bandwidth of 3.7 GHz and driving a load capacitance of 1 pF demands a bias current of about 5 mA in 0.18-μm CMOS technology. The two complex filters in the dual receiver would therefore consume more than 150 mW.

This paper introduces a feedforward technique that relaxes the op amp requirements, allowing a ten-fold reduction in the power consumed by the filters. Consider the integrator shown in Fig. 7(a), where the branch consisting of $-jV_{\mathrm{out}}$ (the output of the Q channel) and R_0 shifts the complex filter frequency response to the right by $\omega_0 = 1/(R_0C_1)$. Inadequate op amp bandwidth here creates substantial peaking in the filter response near the upper edge (23 MHz). Fig. 7(b) depicts a modification that can suppress the high-frequency peaking. With the addition of C_p and C_a to the signal paths, the filter transfer function (for an ideal op amp) is given by

$$\left|\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(j\omega)\right| = \sqrt{\frac{1+\omega^2{R_1}^2{C_p}^2}{{R_1}^2{C_1}^2(\omega-\omega_0)^2+\omega^2{R_1}^2{C_a}^2}} \tag{10}$$

suggesting that C_a reduces the peaking due to the limited bandwidth of the op amp, and C_p compensates the high-frequency droop introduced by C_a. For an actual op amp with a unity-gain bandwidth of 900 MHz, a C_a/C_p of 9 lowers the passband ripple to 0.4 dB. This performance is achieved with an op amp supply current of 0.5 mA.[3]

Fig. 8 shows a slice of the positive complex filter and its connections to the preceding and following slices. For the negative complex filter, the R_0-C_a branch in Fig. 7(b) is connected to $+jV_{\mathrm{out}}$.

Fig. 9 plots the simulated frequency response of the fifth-order Chebyshev positive complex BPF with a two-stage op amp having a bias current of 0.5 mA and unity-gain bandwidth of 900 MHz. As expected, the response of the conventional integrator suffers from a peaking of 23 dB at the upper edge of the

[3]The thermal noise of resistors R_1 and R_0 in Fig. 7(b) still dominates.

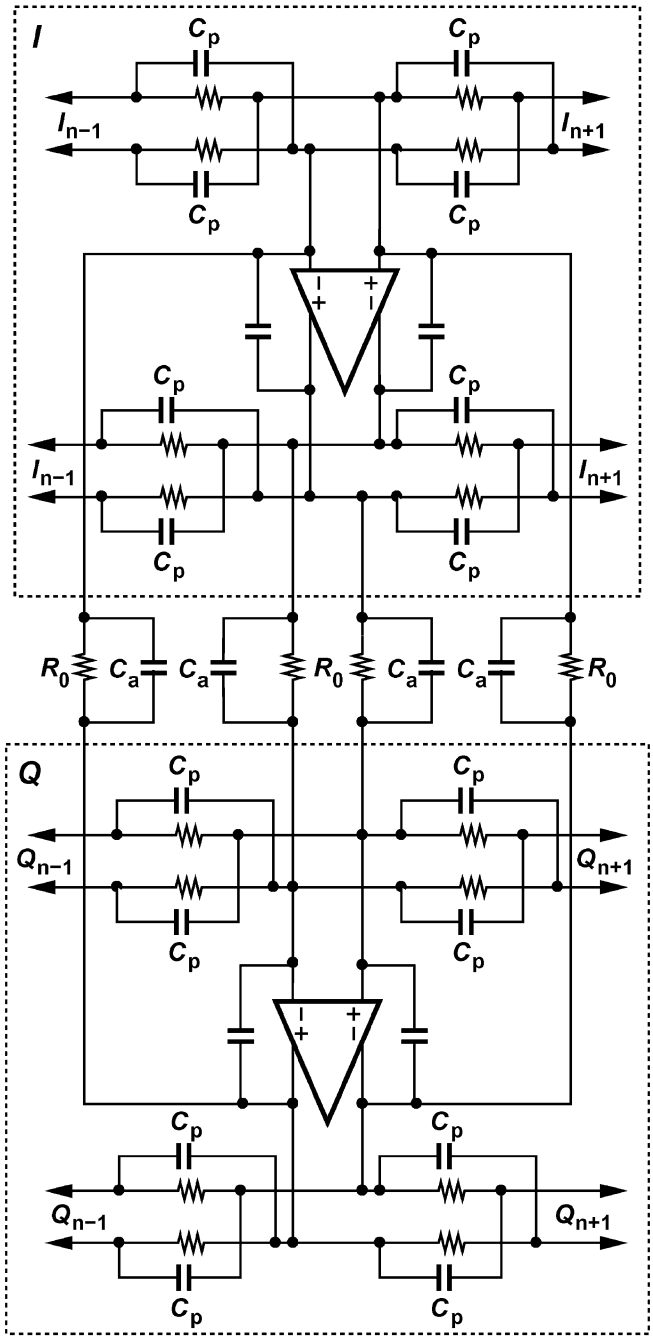

Fig. 8. One slice of complex filter.

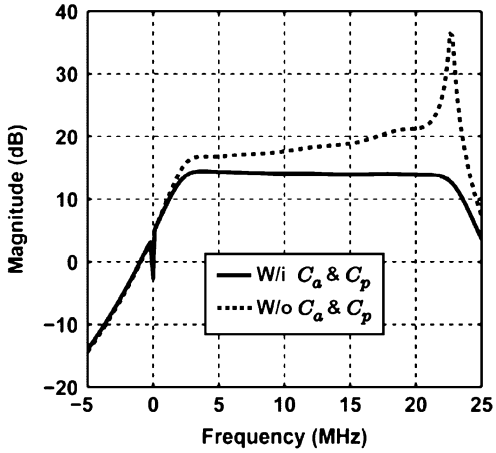

Fig. 9. Effect of C_a and C_p on the positive complex BPF frequency response.

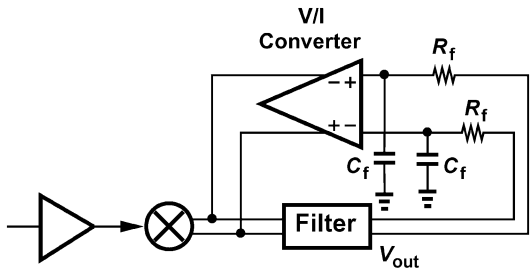

Fig. 10. Offset cancellation loop.

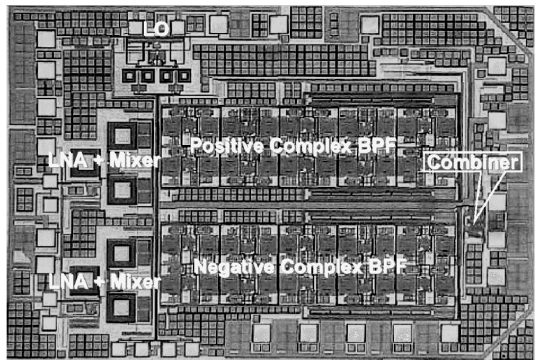

Fig. 11. Dual-antenna receiver die photograph.

passband.[4] On the other hand, with $C_a/C_p = 9$, the passband ripple falls to 0.4 dB. This ratio is relatively independent of the absolute value of the resistors. Note that this technique can be exploited with only complex BPFs.

Simulations indicate that if C_a/C_p deviates from 9 by about 10%, then the ripple increases to 0.6 dB. To allow precise setting of this ratio as well as tuning the filter for process and temperature variations, the circuit incorporates programmable 4-bit capacitor arrays, achieving a capacitor tuning accuracy of 6%. All capacitors are realized as lateral fringe (rather than sandwich) structures to minimize the area.

[4]The notch in the vicinity of zero frequency results from the offset cancellation network.

To suppress the noise of the latter stages and subsequent summing amplifiers, the filter employs a nominal voltage gain of 14 dB in the passband, thereby requiring cancellation or removal of the low-frequency noise and mixer-induced dc offsets that could saturate the following stages. Since ac coupling dictates linear (low-density) capacitors, a very large area would become necessary to achieve a lower corner frequency below 1 MHz because the input resistance of each integrator is on the order of a few kilo-ohms. In this work, the offset is cancelled by negative feedback (Fig. 10) through the use of grounded MOS capacitors. With $R_f = 200$ kΩ and $C_f = 27$ pF, the resulting high-pass characteristic exhibits a -3 dB corner of 600 kHz, well below the lower edge of the channel (4.7 MHz).

Each complex bandpass filter displays an input-referred noise voltage of 18.3 nV/$\sqrt{\text{Hz}}$ and, together with its offset cancellation loops, consumes 10.1 mW.

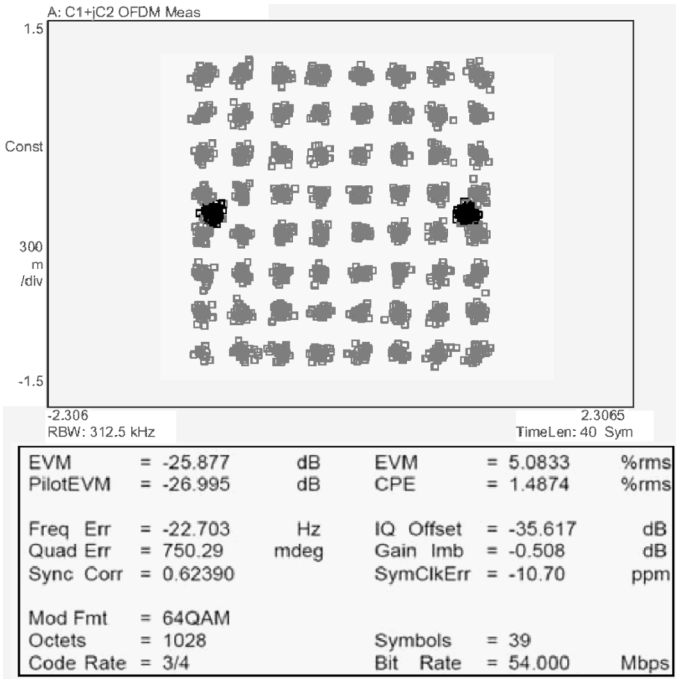

Fig. 12. Sensitivity measurement for one receiver.

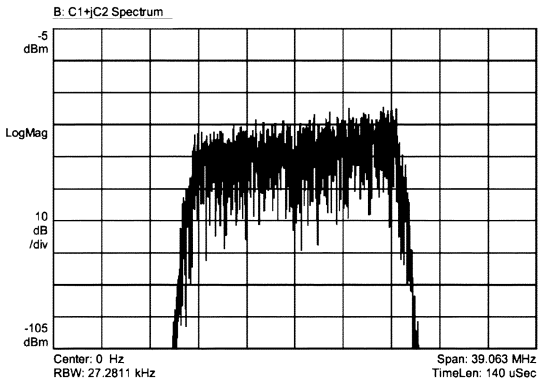

Fig. 13. Measured 64 QAM spectrum.

TABLE I
MEASURED RECEIVER PERFORMANCE

Voltage Gain	43 dB
Noise Figure	5.5 dB
Sensitivity	−72 dBm
Power Dissipation per Channel	30.1 mW
Supply Voltage	1.8 V
Technology	Digital 0.18-μm CMOS
Active Area	1.9 mm × 1.3 mm

V. EXPERIMENTAL RESULTS

The dual-antenna receiver has been fabricated in a digital 0.18-μm CMOS technology with six layers of metal. Fig. 11 shows the die photograph, whose active area measures 1.9 mm × 1.3 mm. The quadrature LO phases are generated on-chip by means of a polyphase filter. The measured noise figure and voltage gain are 5.5 dB and 43 dB, respectively. Each receiver consumes 30.1 mW with a 1.8-V supply, about 60% lower than that of the state of the art [10].[5]

The sensitivity is measured by applying a 5.4-GHz modulated IEEE 802.11a signal to the input and capturing the IF output by means of a digital oscilloscope. The sampled data is then fed to the Advanced Design System (ADS), which downconverts it to baseband and performs detection. Fig. 12 shows the measured 64 QAM constellation produced by one receiver in response to an RF input level of −72 dBm. The EVM is −25 dB.

Fig. 13 depicts the measured IF spectrum, revealing the frequency response of the complex filter. A few decibels of peaking is observed near the upper edge of the passband. Table I summarizes the measured performance of each receiver. This peaking appears benign as the EVM exceeds the standard's specification.

[5]For a fair comparison, only the receive path power consumption of [10] is considered and the synthesizer is excluded.

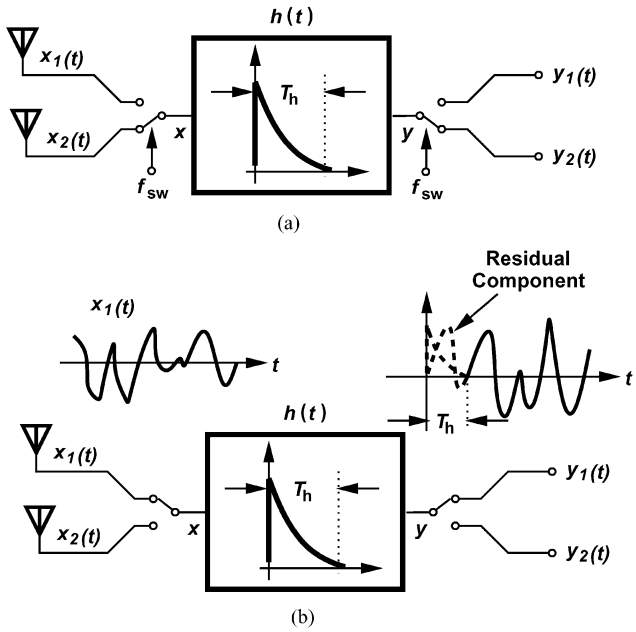

Fig. 14. A different view of filtering in the receive path: (a) switch positioned at the second antenna, and (b) switch positioned at the first antenna.

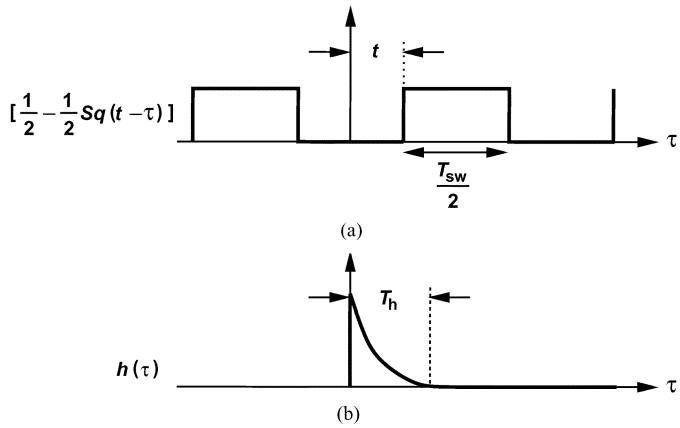

Fig. 15. Graphical representation of (a) switching function as a function of τ, and (b) filter impulse response.

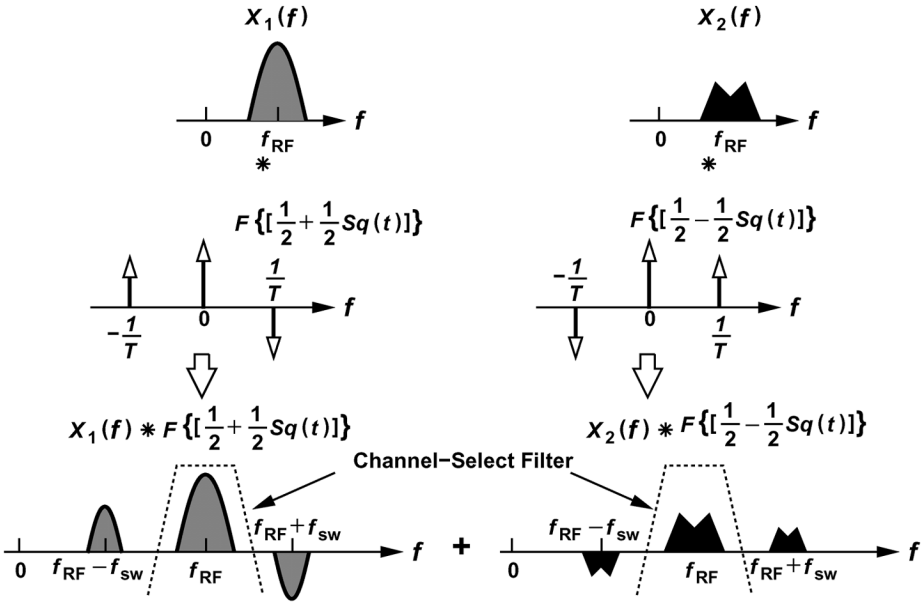

Fig. 16. Receiver input spectrum with filtering in the receive path.

A test is also performed wherein the same 5.4-GHz 64 QAM signal is applied to both receivers and the outputs are reconstructed as explained above. The resulting constellations and EVMs are the same as those depicted in Fig. 12. Note that the coupling between the two receive paths through the substrate and supply lines can be as high as -20 dB with negligible impact on the performance [9].

VI. Conclusion

This work identifies and quantifies two fundamental issues with respect to switching between two antennas, namely, effects of interferers and filtering. A new low-IF receiver architecture is presented that allows halving the number of baseband A/D converters by processing signals in positive and negative frequencies. The proposed complex integrator topology reduces the filter power consumption by a factor of 10, yielding a total power dissipation of 30.1 mW per receiver.

Appendix I

A. Effect of Filtering

Suppose the switching rate is chosen such that interferers do not corrupt the received signal. These interferers must now be removed in the receiver by channel-select filtering. Assume the receiver contains a filter having an impulse response $h(t)$ with a decay time of approximately T_h seconds [Fig. 14(a)], and the switches are initially positioned at x_2 and y_2. When the switches change position, the states within the filter take about T_h seconds to vanish, thus introducing a residual component or "cross interference" in $y_1(t)$ [Fig. 14(b)]. We may therefore expect that T_h must be much less than $1/(2f_{\rm ch})$ for this interference to remain negligible.

To quantify the above phenomenon, we write $y(t) = x(t) * h(t)$ and substitute for $x(t)$ from (4):

$$y(t) = \left\{x_1(t)\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right]\right\} * h(t) + \left\{x_2(t)\left[\frac{1}{2}-\frac{1}{2}Sq(t)\right]\right\} * h(t). \quad (11)$$

Since $y_1(t) = y(t)p_1(t)$, we obtain

$$y_1(t) = \left(\left\{x_1(t)\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right]\right\} * h(t)\right)\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right] + \left(\left\{x_2(t)\left[\frac{1}{2}-\frac{1}{2}Sq(t)\right]\right\} * h(t)\right)\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right] \quad (12)$$

As predicted, $y_1(t)$ is corrupted by $x_2(t)$. Ignoring the common switching factor $[1+Sq(t)]/2$, we write the cross interference as

$$I(t) = \left\{x_2(t)\left[\frac{1}{2}-\frac{1}{2}Sq(t)\right]\right\} * h(t), = \int x_2(t-\tau)\left[\frac{1}{2}-\frac{1}{2}Sq(t-\tau)\right]h(\tau)d\tau. \quad (13)$$

To gain more intuition, we assume $x_2(t) = 1$ as the worst-case condition and consider the product of the other two terms as depicted in Fig. 15. It is observed that if $t \approx 0$, the cross product of the two terms is significant. As t approaches T_h, this product falls to zero and remains at zero for $T_h < t < T_{\rm sw}/2$. In other words, for negligible corruption, $T_h \ll T_{\rm sw}/2$ and hence the filter bandwidth must be much greater than $2f_{\rm sw}$.

In conjunction with the analysis in Section II-B, the above observation suggests that the filter bandwidth must well exceed $2f_{\rm sw}$, and $f_{\rm sw}$ must be large enough to accommodate the interferers. That is, the filter bandwidth cannot be so narrow as to perform channel selection. In fact, a simple analysis reveals

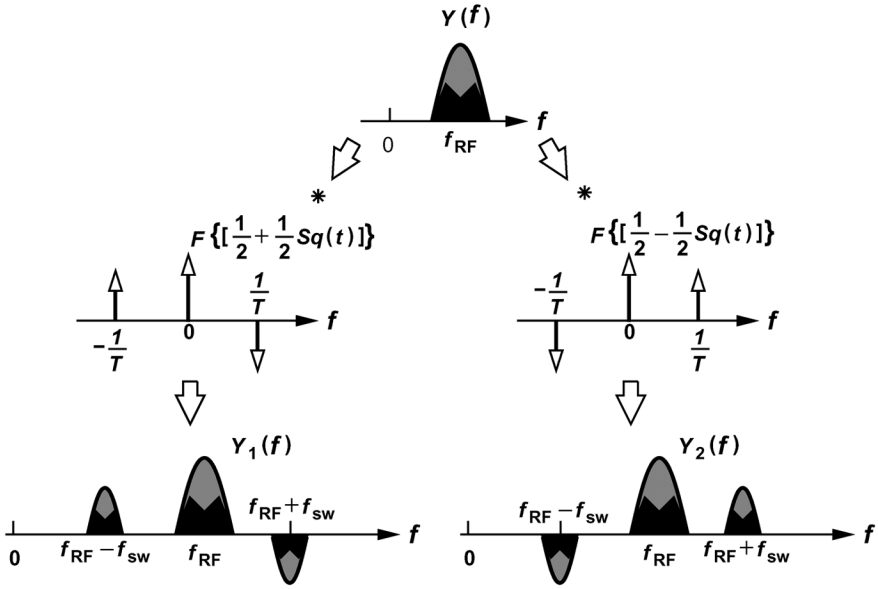

Fig. 17. First and second antenna recovered signals.

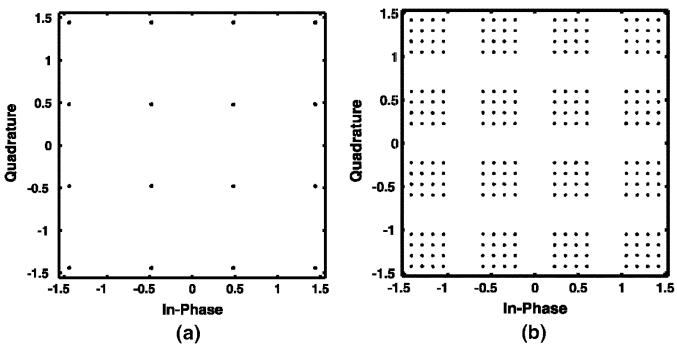

Fig. 18. Effect of channel select filtering when filter bandwidth is (a) 8 times and (b) 1.3 times the switching rate.

what happens if the filter bandwidth *is* equal to the RF channel bandwidth. Referring to (9), we express the spectrum of $x(t)$ as

$$X(f) = X_1(f) * \mathcal{F}\left\{\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right]\right\} + X_2(f) * \mathcal{F}\left\{\left[\frac{1}{2}+\frac{1}{2}Sq(t)\right]\right\} \quad (14)$$

where $\mathcal{F}\{\cdot\}$ denotes the Fourier transform. Fig. 16 illustrates the operations expressed by (14), implying that, if the filter indeed selects the RF channel, the components at $f_{\rm RF} \pm f_{\rm sw}$ are removed, possibly making it difficult to recover the individual signals. Reconstructing $Y_1(f)$ and $Y_2(f)$ as depicted by Fig. 17, we note that each is corrupted by 100% of the other.

To investigate the effect of channel-select filtering on the signal constellation, $x_1(t)$ and $x_2(t)$ in Fig. 14(a) are represented by two identical but phase-shifted 5-GHz 16QAM signals each occupying a bandwidth of 20 MHz. The switching rate is 25 MHz. Fig. 18 shows the results as predicted by Matlab. In Fig. 18(a), the filter bandwidth is eight times the switching rate, yielding a nearly ideal constellation. In Fig. 18(b), on the other hand, the bandwidth is reduced to 1.3 times the switching rate, revealing significant corruption.

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