Analysis of Metastability in Pipelined ADCs

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***Abstract*—A critical issue in the design of high-speed ADCs relates to the errors that result from comparator metastability. Studied for flash architectures in the past, this phenomenon assumes new dimensions in pipelined converters, creating far more complex error mechanisms. This paper presents a comprehensive analysis of comparator metastability effects in pipelined ADCs and develops a method to predict the error behavior for a given input signal PDF Different error mechanisms are identified and formulated to obtain the probability of error versus the magnitude of error. An 8-bit 600 MS/s ADC fabricated in 65 nm CMOS technology has been used to assess the validity of the analytical results.**

***Index Terms*—Average conductance, metastability, multi-bit stage, multiplying DAC, pipelined ADCs, sub-ADC.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) have continued to provide a high performance despite device and supply scaling. Unlike flash converters, however, these ADCs do not lend themselves to comparator pipelining in the main signal path, thus potentially exhibiting a high error rate due to metastability. While occurring not so frequently as to degrade the signal-to-noise ratio (SNR), such errors nonetheless prove problematic in extracting data from digitally modulated waveforms. For example, applications such as instrumentation and serial link receivers require a bit error rate (BER) of less than 10^{-12} [1]–[3].

This paper offers a comprehensive analysis of metastability-induced errors in pipelined ADCs. Several error mechanisms are identified and their resulting error rates are computed. It is also shown that a multi-bit pipelined stage can reduce the error rate considerably.

Sections II and III present the concept of comparator metastability and its effects in a pipeline environment. Circuit models are introduced in Section IV and error mechanisms are formulated in Section V. Section VI deals with calculating the probability of error and Section VII demonstrates the experimental results.

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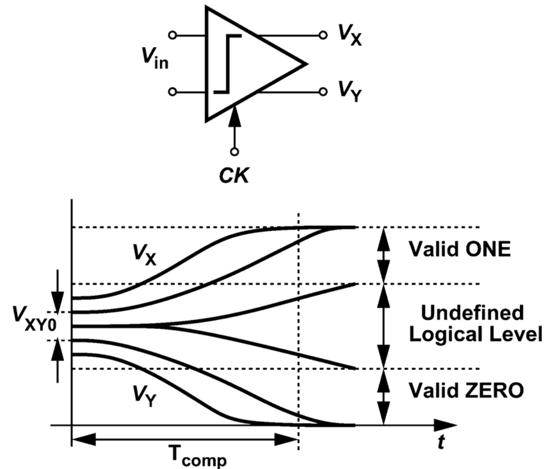

Fig. 1. Outputs of a typical clocked comparator regeneratively depart from an initial value.

II. Background

Comparators typically incorporate a regenerative feedback with clocking so as to provide fast amplification in a certain time period. As illustrated in Fig. 1, the clock, CK, is applied at $t = 0$, and the outputs, V_X, and V_Y, regeneratively depart from an initial difference of V_{XY0}. For an excessively small V_{XY0}, the outputs fail to reach valid logical levels within the allotted time, $T_{\rm comp}$, possibly causing metastability errors in the subsequent stages.

The impact of metastability upon the performance of flash ADCs is well known; if the signal has a uniform distribution between, say, 0 and $V_{\rm REF}$, then the probability of metastable errors is given by

$$P_E = \frac{2(2^N - 1)V_0}{A_1 V_{\rm REF}} \exp \frac{-T_{\rm conv}}{\tau_{\rm reg}} \tag{1}$$

where N is the converter's resolution, V_0 is the minimum output voltage considered a valid logical level, A_1 is the voltage gain of the amplifier preceding the regenerative latch, and $\tau_{\rm reg}$ is the regeneration time constant.

The above probability of error implicitly assumes that the magnitude of the error itself is always the same; otherwise, one would need to express the probability as a function of the error magnitude. Indeed, in a well-designed flash ADC, proper encoding can ensure that a metastable state produces an error of only 1 LSB [4]. Moreover, comparators and/or the encoding logic can be pipelined to reduce P_E. In pipelined ADCs, on the other hand, the situation is far more complex because the comparator metastability can also propagate along the *analog* signal path.

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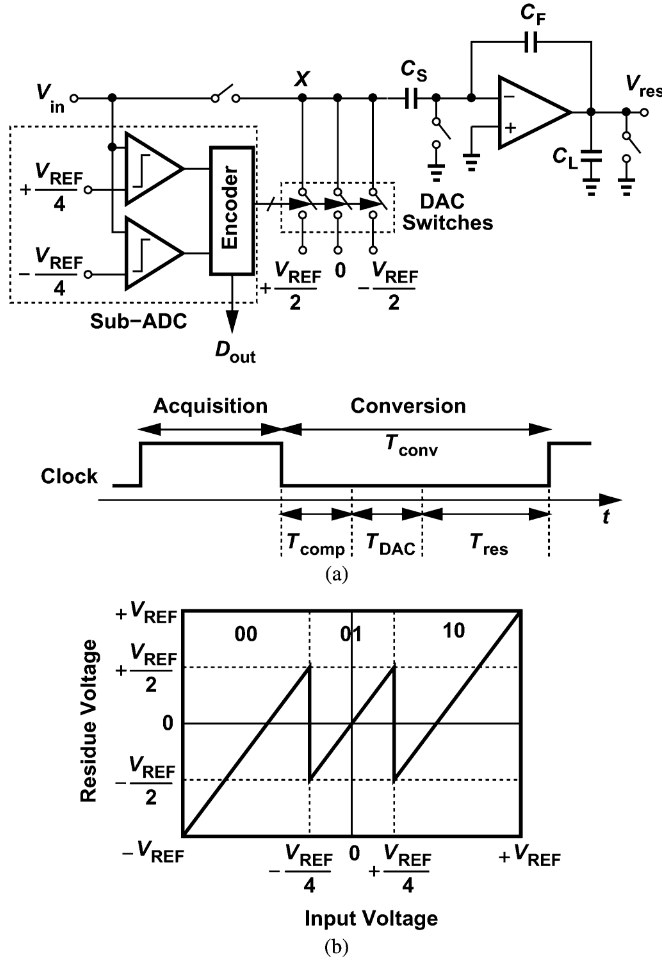


Fig. 2. (a) Block diagram of a non-flip-around 1.5-bit pipelined stage, and (b) its residue characteristic.

III. Metastability in Pipelined ADCs: Qualitative View

In our preliminary qualitative examination, we consider a 1.5-bit non-flip-around stage such as the simplified realization in Fig. 2(a). Here, after acquisition is completed, the sub-ADC comparators compare the differential input with $\pm V_{\rm REF}/4$ and accordingly swing the left plate of C_S to 0 or $\pm V_{\rm REF}/2$. The multiplying digital-to-analog converter (MDAC) thus produces the amplified residue. The conversion time must accommodate the comparison time, $T_{\rm comp}$, (more generally, the sub-ADC conversion time), the DAC settling time, $T_{\rm DAC}$, and the residue amplification time, $T_{\rm res}$. In practice, $T_{\rm DAC}$ and $T_{\rm res}$ may not be readily distinguishable and can be merged into one.

What happens if $V_{\rm in}$ is close to one of the sub-ADC decision thresholds,$-V_{\rm REF}/4$ or $+V_{\rm REF}/4$? The corresponding comparator becomes metastable, affecting both $D_{\rm out}$ and the selection signals driving the three DAC switches. Note that due to multiple stages of latching and pipelining in the aligning logic, the final $D_{\rm out}$ can reach a valid logic level. The DAC selection signals, on the other hand, are on the signal path and cannot be pipelined. We identify three distinct error mechanisms. 1) The metastability is so severe that the corresponding DAC switch does not turn on by the end of $\rm T_{conv}$, i.e., $T_{\rm comp} > T_{\rm conv}$. Node X in Fig. 2(a) therefore floats, and the residue remains near zero. In this case, the ADC digital output may incur an error as high as $\pm V_{\rm REF}/4$. For example, if $V_{\rm in}$ in Fig. 2(b) is close to $-V_{\rm REF}/4$, the sub-ADC may produce 00 or 01, while with a zero residue, the overall ADC interprets the input to be near $-V_{\rm REF}/2$ or zero. 2) The metastable state eventually turns one of the DAC switches on while leaving little time for DAC settling and residue amplification. 3) The encoder results reaching the DAC in Fig. 2(a) are inconsistent with $D_{\rm out}$. This mechanism may occur if the encoder incorporates different paths and logical functions to produce $D_{\rm out}$ and to drive the DAC. Due to noise and offset, these paths may interpret the metastable state inconsistently.

It is worth noting that [3] considers only the first mechanism. This error is the largest, but as explained in Section VI-A, extremely rare. We should also remark that [5] computes the effect of metastability on SNR, a negligible issue in practice.

A critical observation that emerges here is that metastability in pipelined ADCs can lead to *different* amounts of error, an attribute in stark contrast to the behavior of flash ADCs. It is therefore necessary to derive the probability of the error, P_E, in terms of the magnitude of the error, E. This attribute also complicates the design of communication systems employing pipelined ADCs; given the signal and noise characteristics, one must utilize the plot of $P_E(E)$ to determine the overall bit error rate of the system.

IV. Circuit Models for Error Calculations

The error mechanisms outlined in the previous section entail nonlinear phenomena that can lead to intractable algebra. In order to quantify these mechanisms in a manner that provides insight as well as designer-friendly results, we develop in this section simplified models of the circuitry in the signal path. The soundness of our approximations is ultimately tested by transistor-level simulations and experimental results.

A. Comparator Model

Fig. 3 shows the comparator model used in this work. For a metastable comparator, it is assumed that a preamplifier having a linear gain of A_1 drives a regenerative latch with a linear gain of A_2 and a regeneration time constant of $\tau_{\rm reg}$. The logic interposed between the comparator and the DAC switch(es) is also assumed to have a linear gain of A_3 in this condition. The output voltage is thus expressed as

$$V_{\rm logic}(t) = A_1 \left(A_2 \exp \frac{t}{\tau_{\rm reg}} \right) A_3 V_{\rm in}. \tag{2}$$

As shown in [6], this model is feasible even for a circuit as nonlinear as a StrongArm latch. Simulations suggest that, even though A_3 does not come with infinite speed, this simple model accurately predicts the behavior in the metastable regime, when the comparator outputs are near their common-mode level and the subsequent logic is fast enough to provide gain. The preamplifier gain, on the other hand, may take its own time, as discussed below.

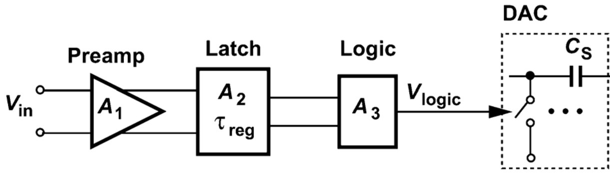


Fig. 3. Sub-ADC comparator outputs driving the DAC switch.

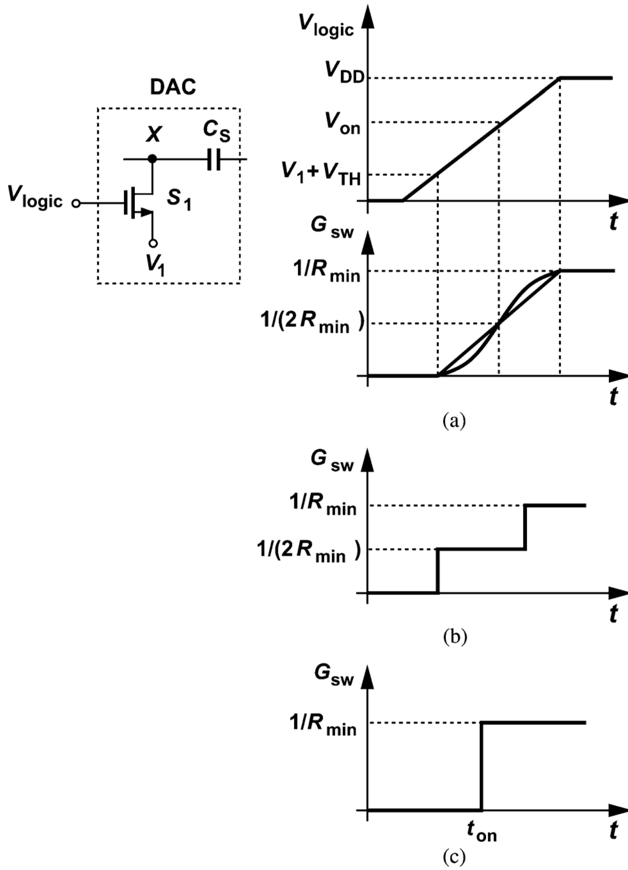


Fig. 4. (a) Behavior of the DAC switch conductance during its gradual turn-on along with its piecewise-linear model, (b) staircase model, and (c) equivalent simplified model.

B. DAC Switch Model

If the metastable state turns on a DAC switch slowly, then the DAC time constant varies significantly with time, making the analysis difficult. Fig. 4(a) illustrates this behavior for one branch of the DAC that nominally applies V_1 ($= 0$, or $\pm V_{\rm REF}/2$) to node X. As the gate voltage of S_1 exceeds V_1 plus one threshold, $V_{\rm TH}$, and reaches $V_{\rm DD}$, the switch conductance goes from zero to $1/R_{\min}$, where $R_{\min}$ denotes the on-resistance with maximum overdrive voltage.

To arrive at our model, we progressively simplify the behavior of the switch: the time dependence of $G_{\rm sw}$ can be represented by 1) a linear change from 0 to $1/R_{\min}$ [the gray curve in Fig. 4(a)], 2) a piecewise-linear approximation going from 0 to $1/(2R_{\min})$ to $1/R_{\min}$,[1] or 3) a one-bit approximation going from 0 to $1/R_{\min}$ at $t = t_{\rm on}$, when the actual switch conductance reaches half of its maximum [Fig. 4(c)]. In other words, we model the turn-on behavior by an abrupt but *delayed* jump. We denote by $V_{\rm on}$ the switch gate voltage that provides an on-resistance of $1/(2R_{\min})$.

The above model allows us to consider the comparator's decision completed once $V_{\rm logic}$ in Fig. 4(a) crosses $V_{\rm on}$. From (2), we have

$$T_{\rm comp} = \tau_{\rm reg} \ln \frac{V_{\rm on}}{A_{\rm tot}|V_{\rm in} \pm V_{\rm REF}/4|} \tag{3}$$

where $A_{\rm tot} = A_1 A_2 A_3$. In addition to the regeneration time, comparators typically require a short preamplification time (to turn on the latch operation), $T_{\rm pre}$, as well. The total time consumed by the comparator is thus equal to $T_{\rm pre} + T_{\rm comp}$, and the available time for DAC and residue settling is

$$T_{\rm MDAC} = T_{\rm conv} - (T_{\rm pre} + T_{\rm comp}). \tag{4}$$

C. MDAC Model

After one of the DAC switches in Fig. 2(a) turns on, two transients take place: the DAC capacitor(s), e.g., C_S, must charge to a voltage, e.g., $V_{\rm REF}/2$, and the output must settle. Shown in Fig. 5(a) is a simplified model of the circuit, where $R_{\rm DAC}$ denotes the switch on-resistance plus the reference generator's output resistance, a critical component in high-speed low-power designs. The small-signal equivalent in Fig. 5(b) allows us to solve the circuit, but the resulting transfer function is of second order, complicating our metastability analysis. Instead, we approximate the DAC and residue settling as follows. First, we recognize that the op amp is typically much slower than the DAC and hence the DAC path can be simplified as shown in Fig. 5(c). Note that V_1 can be written as $D_{\rm sub} V_{\rm REF}/2$, where $D_{\rm sub}$ represents the sub-ADC decision and can be -1, 0, or $+1$. Since V_X begins from the sampled analog input, $V_{\rm in}$, and aims for $D_{\rm sub} V_{\rm REF}/2$, we have

$$V_X(t) = V_{\rm in} \exp \frac{-t}{\tau_{\rm DAC}} + \frac{D_{\rm sub} V_{\rm ref}}{2} \left(1 - \exp \frac{-t}{\tau_{\rm DAC}}\right) \tag{5}$$

where

$$\tau_{\rm DAC} = R_{\rm DAC} C_{\rm eq} \tag{6}$$

and $C_{\rm eq}$ is the total capacitance seen at node X in Fig. 5(c). Next, due to the fast settling of the DAC, the op amp perceives that V_X abruptly jumps from $V_{\rm in}$ to V_1, producing a residue equal to

$$V_{\rm res}(t) = A_{\rm res}(V_{\rm in} - V_1) \left(1 - \exp \frac{-t}{\tau_{\rm res}}\right) \tag{7}$$

where $A_{\rm res}$ and $\tau_{\rm res}$ would be the residue gain and time constant, respectively, if $R_{\rm DAC}$ were zero.[2]

[1]For simplicity, we view $1/(2R_{\min})$ as the average switch conductance even though the actual time average may be somewhat different.

[2]We neglect the slewing time of the op amp.

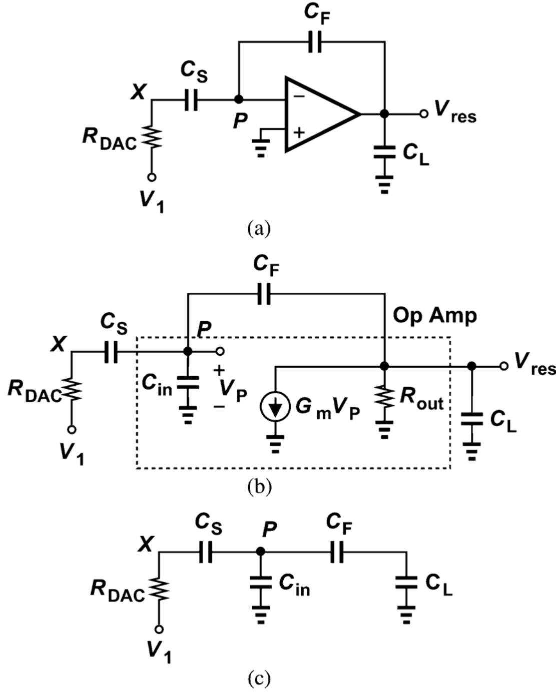


Fig. 5. (a) Simplified MDAC circuit, (b) small-signal MDAC model, and (c) simplified DAC path.

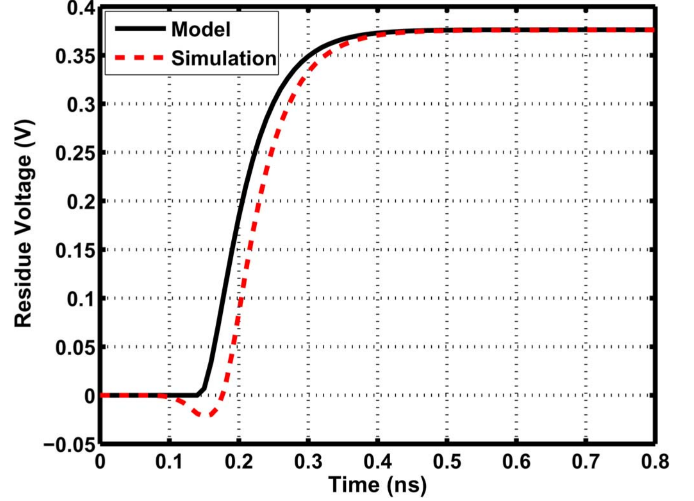


Fig. 6. Residue settling behavior in the second stage of the ADC prototype obtained by transistor-level simulations and proposed model when clocked at $t = 0$.

In the last step of our approximation, we replace $V_{\rm in} - V_1$ in (7) by its actual time-varying value, $V_{\rm in} - V_X(t)$, where $V_X(t)$ is obtained from (5).The amplified residue is therefore given by

$$V_{\rm res}(t) \approx A_{\rm res}\left[V_{\rm in} - V_{\rm in}\exp\frac{-t}{\tau_{\rm DAC}} - \frac{D_{\rm sub}V_{\rm REF}}{2}\left(1-\exp\frac{-t}{\tau_{\rm DAC}}\right)\right]\left(1-\exp\frac{-t}{\tau_{\rm res}}\right). \quad (8)$$

To check the validity of these approximations, Fig. 6 plots the simulated residue settling behavior in the ADC prototype described in Section VII against that predicted by (8). We observe a reasonable agreement between the two.

V. Formulation of Error Mechanisms

With the circuit models developed above, we can now analyze the three error mechanisms described in Section III. We compute the amount of error in this section and the probability of error in Section VI.

A. DAC Switch Remains Off

If the ADC input voltage is sufficiently close to one of the sub-ADC decision thresholds, then the corresponding comparator fails to turn on one of the DAC switches. The zero residue thus translates to a large error.

Let us assume a certain time constant, $\tau_{\rm reg}$, for the comparator and a conversion time, $T_{\rm conv}$, for the entire pipelined stage [Fig. 2(a)]. If the comparator and its subsequent logic produce an output voltage less than $V_{\rm on}$ in $T_{\rm conv}$ seconds [Fig. 4(a)], then the first error mechanism occurs. Eq. (3) implies that a small differential input, ε_1, fails to turn on the DAC switch if

$$|\varepsilon_1| \le \frac{V_{\rm on}}{A_{\rm tot}\exp\frac{T_{\rm conv}}{\tau_{\rm reg}}}. \quad (9)$$

In other words, for a voltage range of $\pm\varepsilon_1$ around $-V_{\rm REF}/4$ or $+V_{\rm REF}/4$ in Fig. 2(b), the overall ADC incurs a large error. This behavior is illustrated in Fig. 7, where the residue remains at zero across each metastability region. For the ADC design described in Section VII with a 0.85 V supply, simulations suggest $V_{\rm on} = 0.7$ V, $A_{\rm tot} = 3.5$, $T_{\rm pre} = 170$ ps, and $\tau_{\rm reg} = 22$ ps, yielding $\varepsilon_1 = 1\times10^{-13}$ V if $T_{\rm conv} = 790$ ps. The value of ε_1 in this example reveals that the first mechanism is extremely rare and hence not a dominant source of errors in typical designs, especially with a nominal supply of 1.2 V.

The amount of error in this case can be computed as follows. Suppose, for example, that $V_{\rm in}$ is very close to $-V_{\rm REF}/4$ in Fig. 7. Then, the sub-ADC may generate 00, while the residue remains equal to zero.[3] In the absence of metastability, on the other hand, a sub-ADC output of 00 with a zero residue would correspond to $V_{\rm in} = -V_{\rm REF}/2$. The input-referred error magnitude is therefore equal to $V_{\rm REF}/4$. If the sub-ADC generates 01, the same error magnitude results. Note that this amount is independent of the residue gain.

In a more general case, we can consider the above phenomenon for the nth stage in a pipeline. The maximum input-referred error in this case is given by

$$|E| = \frac{1}{A_{{\rm res},1}A_{{\rm res},2}\cdots A_{{\rm res},n-1}}\frac{V_{\rm REF}}{4}. \quad (10)$$

B. Incomplete Settling

If the input voltage lies outside, but not far from, the $2\varepsilon_1$ regions in Fig. 7, then the DAC switch turns on slowly, leaving

[3]The digital values 00, 01, and 10 in this case correspond to the $D_{\rm sub}$ values -1, 0, and $+1$, respectively.

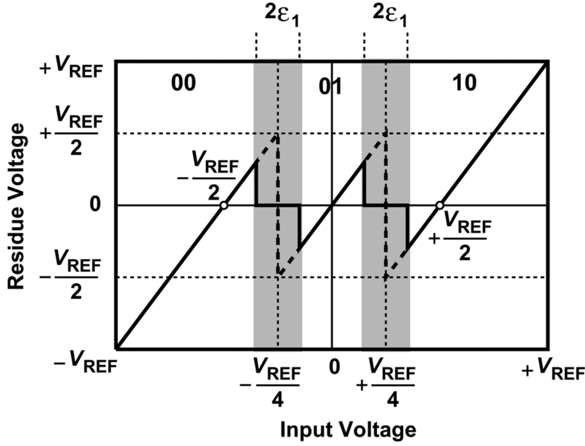
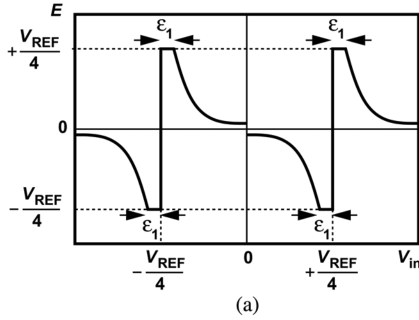
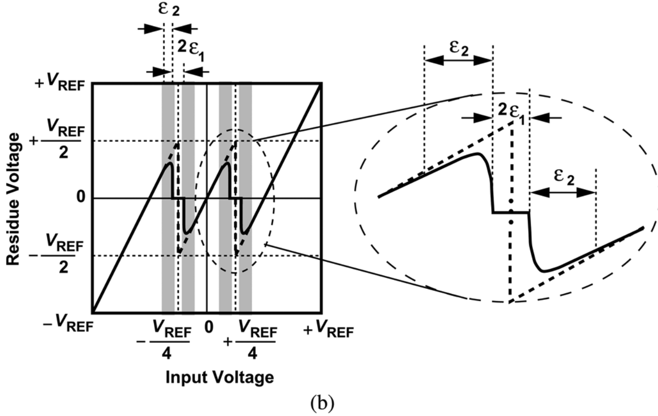


Fig. 7. Residue error for a 1.5-bit stage when MDAC does not receive any decision from the sub-ADC.



(a)



(b)

Fig. 8. (a) Behavior of E across the input range (curves not to scale), and (b) exaggerated residue error for a 1.5-bit stage due to the incomplete reference acquisition and op amp settling.

insufficient time for DAC and residue settling. Since $V_{\rm in}$ is still close to $-V_{\rm REF}/4$ or $+V_{\rm REF}/4$ and $D_{\rm sub} = -1$, 0, or $+1$, we identify the following cases: (a) $V_{\rm in} \approx -V_{\rm REF}/4$ and $D_{\rm sub} = -1$ or 0, (b) $V_{\rm in} \approx +V_{\rm REF}/4$ and $D_{\rm sub} = +1$ or 0. Now we rewrite (8) as follows:

$$V_{\rm res}(t) = A_{\rm res}\left(V_{\rm in} - D_{\rm sub}\frac{V_{\rm REF}}{2}\right) \pm A_{\rm res}\frac{V_{\rm REF}}{4} \times \left[\exp\frac{-t}{\tau_{\rm DAC}} + \exp\frac{-t}{\tau_{\rm res}} - \exp\left(\frac{-t}{\tau_{\rm DAC}} + \frac{-t}{\tau_{\rm res}}\right)\right] \quad (11)$$

where the positive sign holds for $D_{\rm sub} = 0$ and $V_{\rm in} \approx -V_{\rm REF}/4$ or $D_{\rm sub} = +1$ and $V_{\rm in} \approx +V_{\rm REF}/4$ and the negative sign otherwise. Recognizing the first term on the right-hand side as the ideal residue, we consider the reminder as the error once t reaches the available time for the MDAC, $T_{\rm MDAC}$:

$$|E| = \frac{V_{\rm REF}}{4}\left|\exp\frac{-T_{\rm MDAC}}{\tau_{\rm DAC}} + \exp\frac{-T_{\rm MDAC}}{\tau_{\rm res}} - \exp\left[-T_{\rm MDAC}\left(\frac{1}{\tau_{\rm DAC}} + \frac{1}{\tau_{\rm res}}\right)\right]\right| \quad (12)$$

where E is the input-referred error magnitude and hence independent of $A_{\rm res}$. As expected, the error falls exponentially as $T_{\rm MDAC}$ increases.

Equation (12) presents a general relation between the residue error and $T_{\rm MDAC}$. In fact, if $V_{\rm in}$ lies within the $2\varepsilon_1$ regions in Fig. 7, then $T_{\rm MDAC} = 0$ and (12) reduces to $V_{\rm REF}/4$. If $V_{\rm in}$ is outside these regions, then we recall from Section IV-B that $T_{\rm MDAC} = T_{\rm conv} - (T_{\rm pre} + T_{\rm comp})$. Assuming $T_{\rm pre}$ is negligible and $V_{\rm in}$ is close to $-V_{\rm REF}/4$ or $+V_{\rm REF}/4$, we have from (3)

$$T_{\rm MDAC} \cong T_{\rm conv} - \tau_{\rm reg}\ln\frac{V_{\rm on}}{A_{\rm tot}|V_{\rm in} + \beta V_{\rm REF}/4|} \quad (13)$$

where $\beta = -1$, or $+1$ for $V_{\rm in} \approx -V_{\rm REF}/4$ and $V_{\rm in} \approx +V_{\rm REF}/4$, respectively. This expression holds outside the $2\varepsilon_1$ regions. The error given by (12) now reduces to

$$|E| = \frac{V_{\rm REF}}{4}\left|\alpha^{\frac{1}{\tau_{\rm DAC}}} + \alpha^{\frac{1}{\tau_{\rm res}}} - \alpha^{1/\tau_{\rm res}+1/\tau_{\rm DAC}}\right| \quad (14)$$

where

$$\alpha = \left(\frac{V_{\rm on}}{A_{\rm tot}|V_{\rm in} + \beta V_{\rm REF}/4|}\right)^{\tau_{\rm reg}} e^{-T_{\rm conv}}. \quad (15)$$

This equation expresses the error magnitude in terms of known circuit parameters for a given difference between $V_{\rm in}$ and one of the sub-ADC decision thresholds, $-V_{\rm REF}/4$ or $+V_{\rm REF}/4$ so long as $V_{\rm in}$ is outside the $2\varepsilon_1$ regions. In a typical design, $\tau_{\rm res} \gg \tau_{\rm DAC}$ and $\alpha^{1/\tau_{\rm res}}$ dominates.

It is instructive to sketch the above error as a function of $V_{\rm in}$ and examine its effect on the residue plot. Fig. 8(a) illustrates the behavior of E and Fig. 8(b) shows the resulting residue. We denote the second metastability regions by ε_2. That is, we define ε_2 such that, if the difference between $V_{\rm in}$ and $-V_{\rm REF}/4$ or $+V_{\rm REF}/4$ is greater than $\varepsilon_1 + \varepsilon_2$, then the residue error is negligible, e.g., around 0.1 LSB. With this criterion, one can set $|E|$ in (14) to $0.1 \times 2V_{\rm REF}/2^N$, where N is the overall ADC resolution, and numerically compute the corresponding $V_{\rm in} + \beta V_{\rm REF}/4$.

We conclude this section with two observations. First, in a typical pipelined stage, $\tau_{\rm DAC} \ll \tau_{\rm res}$, allowing (14) to be simplified to

$$|E| = \frac{V_{\rm REF}}{4}\left(\frac{V_{\rm on}}{A_{\rm tot}|V_{\rm in} + \beta V_{\rm REF}/4|}\right)^{\frac{\tau_{\rm reg}}{\tau_{\rm res}}} \exp\left(-\frac{T_{\rm conv}}{\tau_{\rm res}}\right). \quad (16)$$

While somewhat similar to (1), (16) yields the *magnitude* of the error, a pipelined specific attribute; $\tau_{\rm res}$ [and $\tau_{\rm DAC}$ in the general form by (14)] are specific to pipelined ADCs and have no counterpart in flash architectures. Second, for metastability

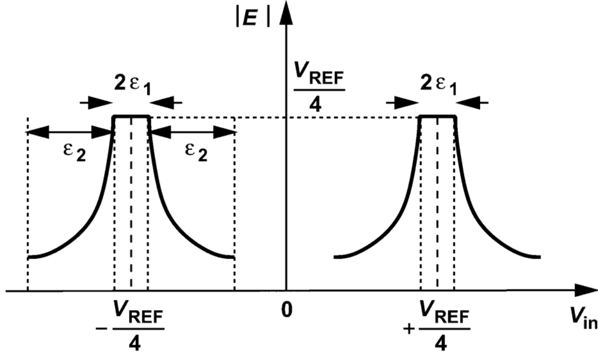


Fig. 9. Summary of the metastability error magnitude for a non-flip-around 1.5-bit stage.

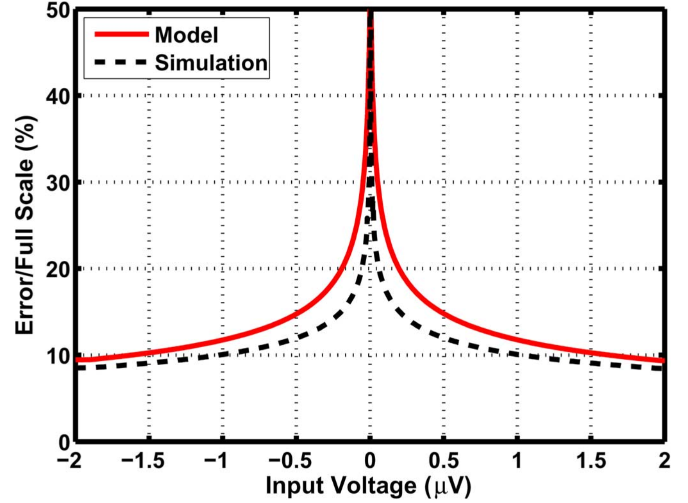


Fig. 10. Comparison between Cadence simulation results of metastability error in a 1-bit stage with results obtained by the proposed model.

in the n-th stage of a pipeline, (14) and (16) still hold, but in a manner similar to (10), they must be divided by the gain of the preceding stages.

C. Encoder Inconsistency

As explained in Section III, the third type of metastability error occurs if the encoder produces inconsistent results for the DAC and $D_{\rm out}$ in Fig. 2(a). For example, if a resistor-ladder DAC is driven by a 1-of-n code while $D_{\rm out}$ is generated by an adder that directly senses the thermometer code, then the two results may disagree in the presence of metastability. This mechanism can nonetheless be suppressed by careful design of the encoder, reducing the occurrence of this error to only the very rare case when the DAC switch does not turn on. For example, the design in [7] converts the thermometer code to a 1-of-n code and applies the result to both the DAC and a ROM-based decoder, ensuring more consistent decisions. (In the analysis of the second mechanism described above, we have assumed this type of logic and hence no contribution by the third mechanism).

D. Simulation Results

Fig. 9 pictorially summarizes the results of our metastability study thus far, assuming a 1.5-bit non-flip-around stage. We should remark that (a) for a 1-bit stage, a similar behavior is expected but with only one error curve around $V_{\rm in} = 0$ and a maximum error of $V_{\rm REF}/2$, and (b) for stage resolutions greater than 1.5 bits, the error curve repeats around each sub-ADC threshold and has a maximum value that is exponentially lower.

The validity of the models and approximations presented in the previous sections has been confirmed using Cadence simulations. Fig. 10 plots the error magnitude around the decision threshold of a 1-bit stage, demonstrating a reasonable agreement. For higher stage resolutions, similar results have been obtained.

VI. Probability of Error

A. 1.5-Bit Stage

With the metastability error magnitude known, we can now derive the statistical characteristics of the error if the probability density function (PDF) of the input signal is given. To this end, we make a slight change in our notation and redraw one error

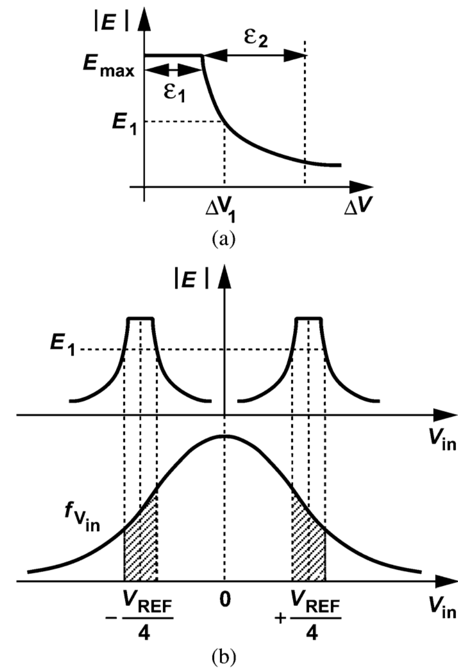


Fig. 11. (a) Error characteristic, and (b) probability of error viewed as the corresponding area under the input PDF.

curve in Fig. 9 as in Fig. 11(a), where ΔV denotes the difference between the input voltage and the decision threshold of interest, e.g., $\Delta V = V_{\rm in} - V_{\rm REF}/4$. We wish to determine the probability that the error magnitude is greater than a certain amount, e.g., E_1. This probability is equal to the probability that the input difference is less than the corresponding ΔV, ΔV_1. That is,

$$P(E > E_1) = \text{prob}\left\{|\Delta V| < \Delta V_1\right\}. \tag{17}$$

We recognize that the right-hand side is in fact equal to the area under the PDF from $\Delta V = -\Delta V_1$ to $\Delta V = \Delta V_1$. As an example, if the input has a Gaussian PDF, $f_{V_{\rm in}}(V_{\rm in})$, with a peak at $V_{\rm in} = 0$, the probability of $E > E_1$ is equal to the shaded areas in Fig. 11(b). Since metastability arises for small input differences, we note that each of the shaded areas can be approx-

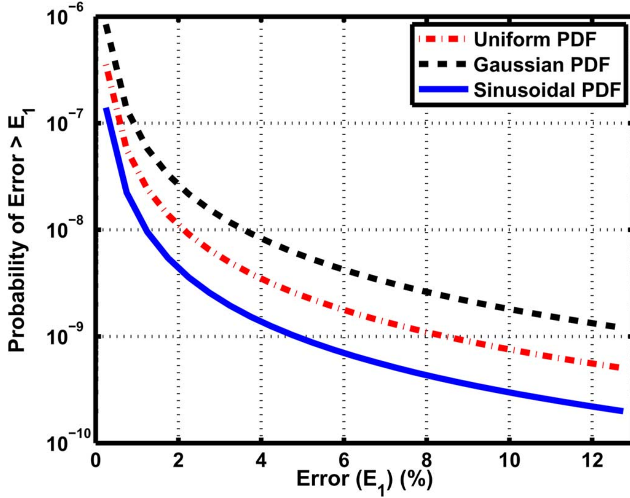


Fig. 12. Probability of error versus magnitude of error for a 1.5-bit stage.

imated as $2\Delta V_1 f_{V_{\rm in}}(V_{\rm in} = V_{\rm REF}/4)$. Thus, $P(E > E_1) \approx 4\Delta V_1 f_{V_{\rm in}}(V_{\rm REF}/4)$. For a general PDF,

$$P(E > E_1) \approx 2\Delta V_1 \left[f_{V_{\rm in}}\left(\frac{-V_{\rm REF}}{4}\right) + f_{V_{\rm in}}\left(\frac{+V_{\rm REF}}{4}\right)\right]. \tag{18}$$

In the last step of our analysis, we wish to express the probability of the error in terms of the error magnitude, and hence ΔV_1 in (18) in terms of E_1. Rewriting (16) as

$$E_1 = \frac{V_{\rm REF}}{4}\left(\frac{V_{\rm on}}{A_{\rm tot}|\Delta V_1|}\right)^{\frac{\tau_{\rm reg}}{\tau_{\rm res}}} \exp\left(\frac{-T_{\rm conv}}{\tau_{\rm res}}\right) \tag{19}$$

we have

$$|\Delta V_1| = \frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{\frac{V_{\rm REF}}{4}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}}. \tag{20}$$

It follows from (18) that

$$P(E > E_1) = 4\frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{V_{\rm REF}/4}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} \times f_{V_{\rm in}}\left(\frac{V_{\rm REF}}{4}\right) \tag{21}$$

if the signal PDF is symmetric with respect to $V_{\rm in} = 0$.

In summary, the probability that the metastability error is greater than E_1 is computed as follows: 1) determine the voltage difference, ΔV_1, with respect to each decision threshold that yields E_1 [e.g., from Fig. 11(a)]; 2) evaluate the input signal PDF at each decision threshold; and 3) multiply the results of the first two steps and sum the products.

Fig. 12 plots this probability for a 1.5-bit stage with three different signal distributions. Different behaviors are expected: a sinusoidal signal spends less time around $V_{\rm in} = \pm V_{\rm REF}/4$ (the decision thresholds) than does a uniformly distributed input, and a uniformly distributed input spends less time around $V_{\rm in} = \pm V_{\rm REF}/4$ than does a Gaussian input.

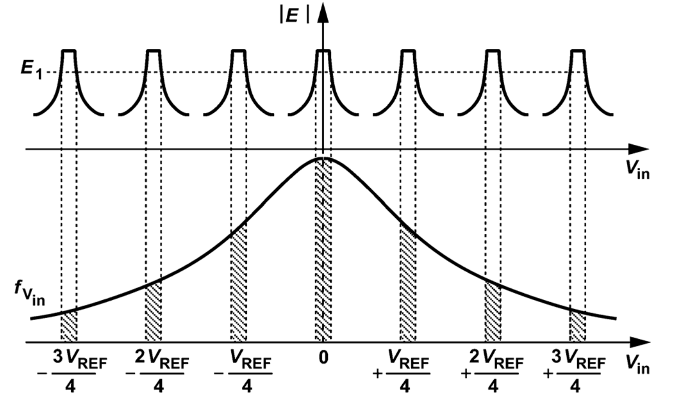


Fig. 13. Error characteristic and probability calculation for a 3-bit stage.

B. Multi-Bit Stage

The foregoing derivations can be readily generalized for an M-bit sub-ADC in the first stage of the pipeline. In this case, there are $2^M - 1$ decision thresholds and for each (14) is rewritten as

$$|E| = \frac{V_{\rm REF}}{2^M}\left|\alpha^{\frac{1}{\tau_{\rm DAC}}} + \alpha^{\frac{1}{\tau_{\rm res}}} - \alpha^{1/\tau_{\rm res}+1/\tau_{\rm DAC}}\right|, \tag{22}$$

revealing that the maximum error is reduced. Now, (21) emerges as

$$P(E > E_1) = 2\frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{V_{\rm REF}/2^M}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} \times \sum_{k=-L}^{+L} f_{V_{\rm in}}\left(k\frac{V_{\rm REF}}{2^{M-1}}\right) \tag{23}$$

where $L = 2^{M-1} - 1$. The factor 2^M inside the square brackets suggests an exponential drop in $P(E > E_1)$. Fig. 13 illustrates a 3-bit example for a Gaussian input. The summation in (23) consists of terms of the form $1/(\sigma\sqrt{2\pi})\exp[(-kV_{\rm REF}/4)^2/(2\sigma^2)]$, where σ denotes the standard deviation of the input PDF. This expression does not simplify further, but if we assume that $\sigma \approx V_{\rm REF}/4$ (so that the signal level rarely exceeds $\pm V_{\rm REF}$), then $P(E > E_1)$ is lower than that of a 1.5-bit stage by a factor of $2 \times 2^{-\tau_{\rm res}/\tau_{\rm reg}}$. Fig. 14 plots $P(E > E_1)$ for $M = 2$, 3, and 4, highlighting the sharp fall as M increases.

If the input has a uniform PDF with a height of $1/(2V_{\rm REF})$, (21) reduces to

$$\begin{aligned} P(E > E_1) &= 2\frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{V_{\rm REF}/2^M}\right]^{-\tau_{\rm res}/\tau_{\rm reg}}\frac{2^M - 1}{2V_{\rm REF}} \\ &\approx \frac{V_{\rm on}}{A_{\rm tot}V_{\rm REF}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{V_{\rm REF}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} 2^{M(1-\tau_{\rm res}/\tau_{\rm reg})}. \end{aligned} \tag{24}$$

It is assumed $2^M \gg 1$. Thus, as M increases, $P(E > E_1)$ falls because $\tau_{\rm res}$ is typically much larger than $\tau_{\rm reg}$.

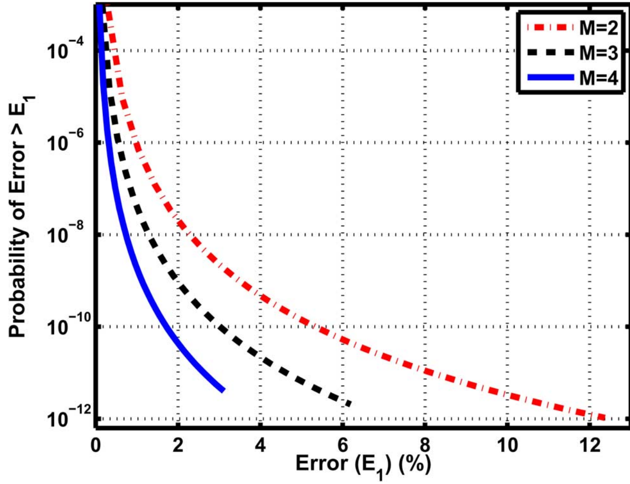


Fig. 14. Probability of error versus magnitude of error for 2-bit, 3-bit, and 4-bit stages.

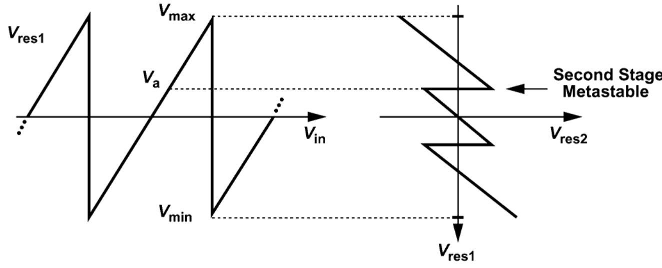


Fig. 15. Effect of first stage metastability on the second stage metastability.

C. Overall Probability in a Pipelined ADC

In order to determine metastability errors due to all stages in a pipelined ADC, we must answer two questions. First, does stage j experience metastability if stage $j-1$ is deeply metastable? Second, how are metastability errors in various stages combined and referred to the input?

Suppose the first stage is deeply metastable and hence its residue, $V_{\rm res1}$, is equal to zero (if offsets are ignored). From Fig. 15, we recognize that, in this case, the second stage is *not* metastable if it has a resolution of 1.5 bits. For the second stage to become metastable, the first residue must reach an appreciable fraction of $V_{\rm REF}$, e.g., $\pm V_{\rm REF}/4$, (V_a in Fig. 15), in which case the first stage is unlikely to be metastable.

To answer the second question, we recall from (10) that the magnitude of metastability errors occurring in the subsequent stages is scaled down when referred to the main input. However, the *number* of decision thresholds increases as the signal travels through the pipeline. In Fig. 15, for example, as $V_{\rm res1}$ varies from $V_{\rm min}$ to $V_{\rm max}$, $V_{\rm res2}$ crosses two decision thresholds.

As an example, let us assume an ADC incorporating three 1.5-bit stages, each with a residue gain of 2. Fig. 16 plots the metastability error magnitude as a function of the input voltage.[4] We observe that the first stage contributes large errors at two decision thresholds, the second stage, smaller errors but at six decision errors, etc. We also note that an error equal to E_a (e.g., 2%) can be created by any of the stages whereas an error equal to E_b (e.g., 9%) can arise from only the first stage.

[4]Here, the comparator response time is chosen unrealistically long so as to obtain the familiar shape for each error curve. In reality, with this horizontal scale, each curve would resemble an impulse.

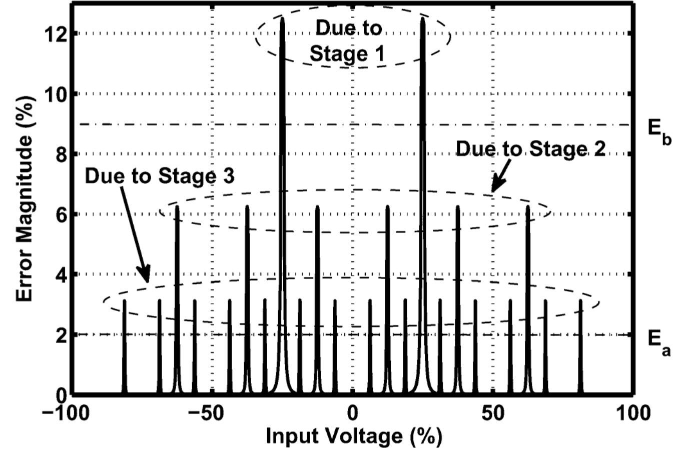


Fig. 16. ADC error due to metastability in the first three 1.5-bit stages.

To formulate the probability that $E > E_1$, we recall from (17) and (18) that the input signal PDF must be evaluated at each decision threshold, $V_{\rm th}$, and multiplied by the input voltage difference that produces $E = E_1$. We generalize (17) as follows:

$$P(E > E_1) = \sum_{k=1}^{F}\sum_{l=1}^{n_k} 2\Delta V_{k,l} f_{V_{\rm in}}(V_{{\rm th},k,l}) \qquad (25)$$

where F is the number of stages, n_k is the total number of decision thresholds resulting from stage k, and $\Delta V_{k,l}$ is that voltage difference which yields E_1. Note that $\Delta V_{k,l}$ is the input-referred value obtained from (20) for a 1.5-bit stage as

$$\Delta V_k = \frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{2^{k-1}E_1}{\frac{V_{\rm REF}}{4}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} \qquad (26)$$

where the factor 2^{k-1} assumes a residue gain of 2 for each preceding stage. It follows from (25) and (26) that

$$P(E > E_1) = 2\frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{\frac{V_{\rm REF}}{4}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} \times \sum_{k=1}^{F} 2^{-(k-1)\tau_{\rm res}/\tau_{\rm reg}} \sum_{l=1}^{n_k} f_{V_{\rm in}}(V_{{\rm th},k,l}). \qquad (27)$$

If the stages are not identical, the terms predicting the summation in (25) must remain within the summation and be calculated for each stage.

Fig. 17 plots the probability of error for three 1.5-bit stages in a cascade along with the total error rate. It is evident that the first stage is the dominant source of error.

D. Design Guidelines

The analysis presented in the previous sections provides several guidelines for the reduction of metastability in pipelined ADCs.

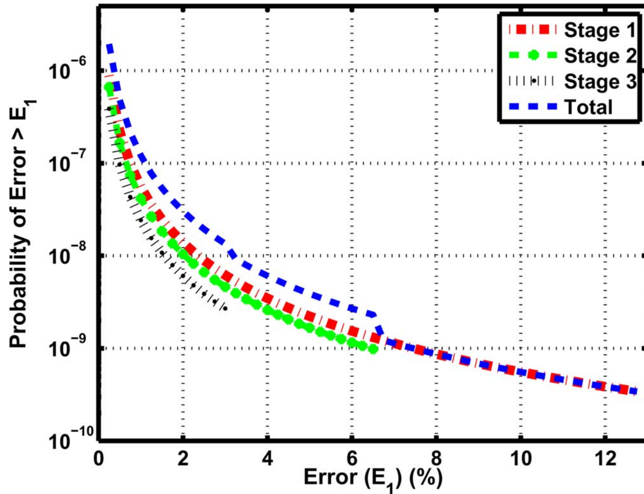


Fig. 17. Probability of error for three 1.5-bit stages in cascade.

1) The resolution of the first stage should be maximized so as to exponentially lower metastability errors. As explained in [9], this effort does face certain limitations in practice, but a more aggressive design targeting, say, 6 bits of resolution greatly reduces the error rate.
2) It is possible to strobe the sub-ADC comparators slightly before the input tracking phase ends, allowing a longer comparison time and hence a lower metastability error rate. The time saved by this operation translates to a voltage discrepancy between the values sampled by the sub-ADC and the MDAC and must be accommodated by the redundancy.
3) Equation (27) and Fig. 17 reveal that the first two or three stages in a pipeline are the dominant contributors to metastability errors, suggesting that an optimum design should allocate more power dissipation (and hence a shorter regeneration time constant) to the comparators in these stages than in the remaining stages.

VII. Experimental Results

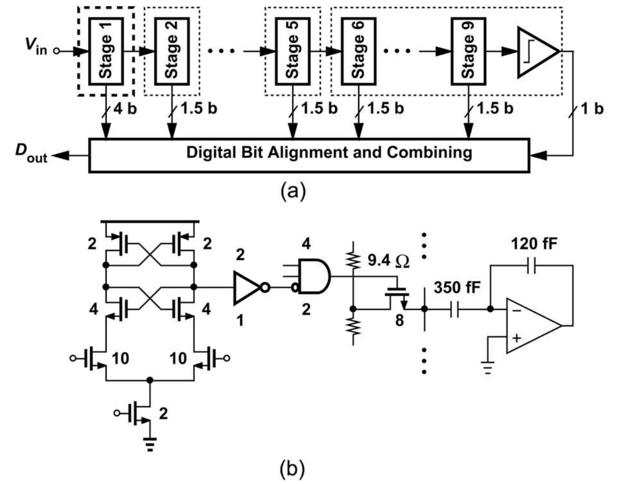
In order to assess the validity of the analyses presented in this paper, we have performed error measurements on an 8-bit 600 MHz ADC based on the design reported in [7]. Fig. 18(a) shows the ADC architecture, highlighting that the front end resolves 4 bits and each subsequent stage, 1.5 bits. This architecture exercises the general results presented in Section VI for an M-bit stage. In a manner similar to that in [7], the gain errors of the stages are calibrated in the digital domain. Fig. 18(b) shows the die photo.

Unlike standard flash ADC metastability measurements, our evaluation seeks both the occurrence of an error and its magnitude, requiring a more complex setup. Let us choose the analog input frequency, $f_{\rm in}$, such that $V_{\rm in}$ changes by no more than 1 LSB between each two successive samples:

$$f_{\rm in} < \frac{f_S}{2^N \pi} \tag{28}$$

where f_S is the sampling rate. Now, we compare each two successive ADC outputs and tag as erroneous those that differ by more than 1 LSB. Fig. 19 illustrates the setup performing these functions, where the ADC output is stored in register A and, after one clock delay, in register B. Once the error magnitude, $|A-B|$, is computed, the corresponding bin in the histogram is incremented by 1.

The above approach measures any error that the ADC incurs each time, including those due to quantization, electronic noise,



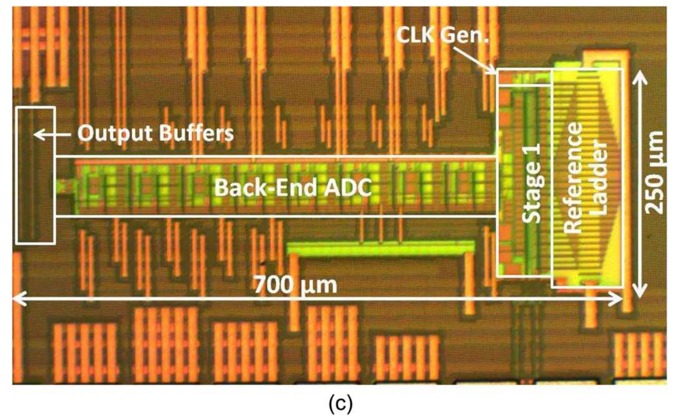


Fig. 18. (a) Prototype ADC architecture, (b) simplified diagram of a critical signal path (device widths are shown in microns; lengths are equal to 60 nm.), and (c) the die photograph.

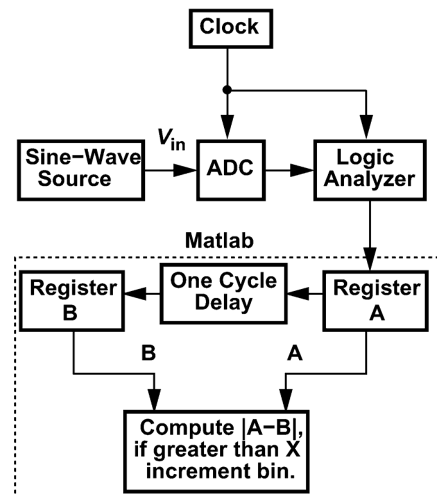


Fig. 19. Setup of the metastability measurement.

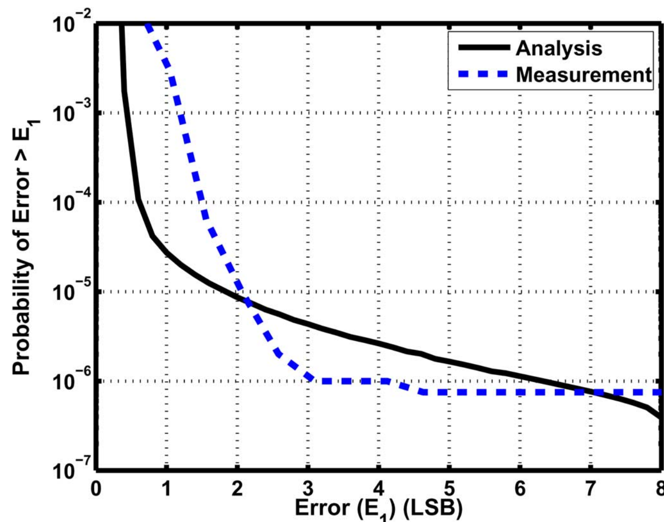


Fig. 20. Error rate versus error magnitude plots obtained by measurements and analysis.

TABLE I
SIMULATED CIRCUIT PARAMETERS OF THE FIRST THREE STAGES

	T_{conv} (ns)	τ_{reg} (ps)	V_{on} (V)	A_{tot} (V / V)	T_{pre} (ps)	τ_{DAC} (ps)	τ_{res} (ps)
Stage 1	1.05	47	0.75	1.5	220	70	75
Stage 2	0.79	22	0.7	3.5	170	200	100
Stage 3	0.79	22	0.7	3.5	170	250	135

and differential nonlinearity. Thus, metastability errors less than a few LSB cannot be distinguished from these other sources.[5]

Fig. 20 plots the measured probability of error along with the theoretical prediction stipulated by (25). The values used in the equation are obtained from transistor-level simulations and shown in Table I.[6]

Due to the physical limitations of the setup, e.g., the down-sampling of the ADC output by a factor of 16, the depth of the logic analyzer's memory, and the slow link between the analyzer and Matlab, it takes an extremely long time to collect statistically significant data for very low error rates. For this reason, the supply voltage of the ADC is lowered to 0.85 V so as to raise the probability of metastable states. The critical signal path along with the comparator topology are shown in Fig. 18(b), highlighting the dependence of both the comparator speed and the DAC settling on the supply. The measured plot in Fig. 20 represents a total of about 10^{10} samples that have been automatically collected over 25 days. Due to the slow link between the setup and Matlab, the data is collected only at regular intervals and discarded otherwise.[7]

[5]Since the setup has no "memory," it cannot average out the effect of random noise.

[6]Average values are used for all the decision levels of a stage. Also, $\tau_{\rm res}$ is not much less than $\tau_{\rm DAC}$ because $V_{\rm DD}$ is quite lower than the nominal value.

[7]As with typical ADC testing, the analog input and clock are not locked. The phases thus slide with a very long periodicity.

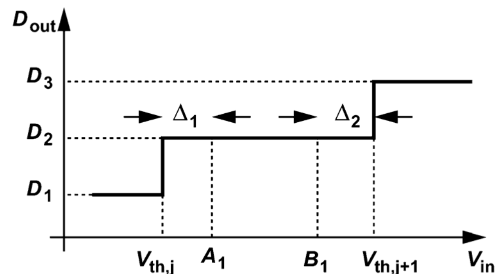


Fig. 21. Resulting error due to threshold ambiguity caused by thermal noise and DNL.

We observe from Fig. 20 that the proposed model predicts the general metastability behavior of the ADC with moderate accuracy for error magnitudes greater than 2 LSB. The discrepancy for errors less than 2 LSB is attributed to the effects mentioned above, namely, quantization and electronic noise and DNL. To clarify this point, we consider the situation depicted in Fig. 21, where two consecutive samples A_1 and B_1 are less than 1 LSB apart and lie away from the decision thresholds, experiencing no metastability. We recognize that the additive electronic noise of the ADC can alter the error measured by our procedure. Suppose the noise voltages added to A_1 and B_1 are denoted by V_{n1} and V_{n2}, respectively, and assumed independent. Also, assume the noise is Gaussian and much less than 1 LSB. The probability that $|A_1 - B_1|$ is interpreted to be less than 1 LSB is given by $P(V_{n1} > -\Delta_1).P(V_{n2} < +\Delta_2)$, a small value. Thus, $|A_1 - B_1|$ is frequently interpreted to be greater than 1 LSB, hence the large discrepancy at $E_1 = 1$ LSB in Fig. 20. On the other hand, for $|A_1 - B_1|$ to be interpreted greater than 2 LSB, we must have $P(V_{n1} < -\Delta_1) \cdot P(V_{n2} > +\Delta_2)$, also a small value. Consequently, few 2-LSB errors arise from only noise, causing much less discrepancy. It should be noted that the first stage is dominant in causing metastable states, producing a maximum error magnitude of 8 LSB. The second and third stages operate on one-fourth of the signal swing and hence, produce maximum error magnitudes of 4 LSB and 2 LSB, respectively.

VIII. CONCLUSION

Pipelined ADCs exhibit interesting metastability mechanisms that corrupt the residue and/or the digital output generated by each stage. Depending on the "depth" of metastability, the residue may be completely incorrect or not have sufficient time to settle. Moreover, the residue and digital outputs of a given stage may be inconsistent. Deriving analytical expressions for the metastability error magnitude and its probability, this paper also recognizes that a multi-bit front end dramatically reduces the error probability. The metastability behavior of an 8-bit 600 MS/s CMOS ADC has been characterized and shown to have a modest agreement with the theoretical results.

APPENDIX I

METASTABILITY IN A FLIP-AROUND STAGE

Shown in Fig. 22(a) is a 1.5-bit flip-around topology that operates as following: during the sampling phase C_S and C_F sample the input voltage and subsequently C_F flips around the amplifier while C_S switches to a DAC voltage. If the sub-ADC

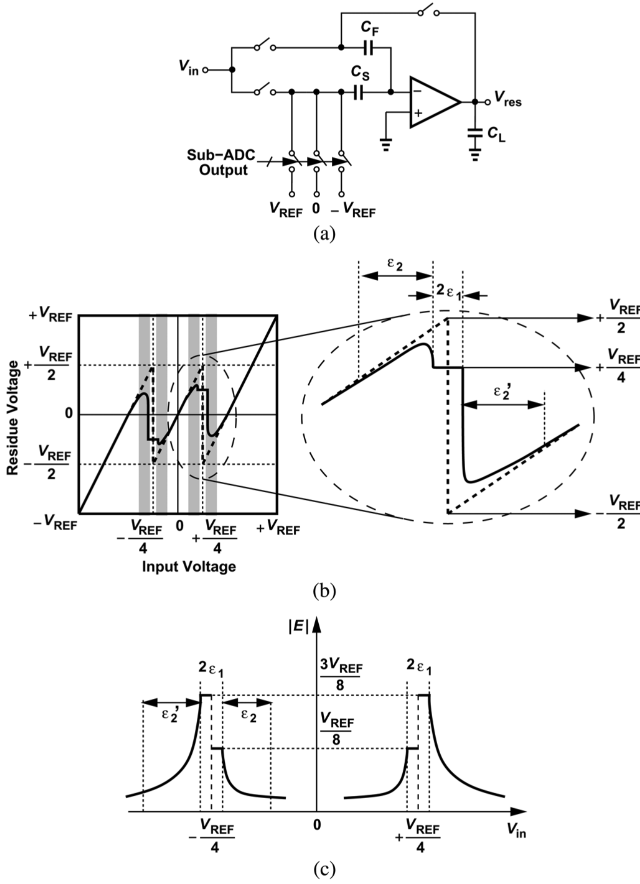


Fig. 22. (a) A 1.5-bit flip-around stage, (b) its residue behavior, and (c) the input-referred residue error.

comparator is metastable, C_F still switches to the output node, but C_S may connect to one of the DAC voltages slowly or not at all. In a similar manner as described for a non-flip-around stage in Section IV-C and assuming a residue gain of 2, we obtain

$$V_{\rm res}(t) \approx V_{\rm in} + \left[V_{\rm in} - V_{\rm in}\exp\frac{-t}{\tau_{\rm DAC}} - D_{\rm sub}V_{\rm REF}\left(1-\exp\frac{-t}{\tau_{\rm DAC}}\right)\right]\left(1-\exp\frac{-t}{\tau_{\rm res}}\right). \quad (29)$$

Substituting $V_{\rm in}$ with $\pm V_{\rm REF}/4$ in (29), it can be shown that the amount of input-referred error for this topology depends on the implied digital output of the stage and is given by

$$|E| = \frac{V_{\rm REF}}{8}\left|\alpha^{\frac{1}{\tau_{\rm DAC}}} + \alpha^{\frac{1}{\tau_{\rm res}}} - \alpha^{1/\tau_{\rm res}+1/\tau_{\rm DAC}}\right| \quad (30)$$

if $D_{\rm sub}$ is 0, and

$$|E| = \frac{3V_{\rm REF}}{8}\left|\alpha^{\frac{1}{\tau_{\rm DAC}}} + \alpha^{\frac{1}{\tau_{\rm res}}} - \alpha^{1/\tau_{\rm res}+1/\tau_{\rm DAC}}\right| \quad (31)$$

if $D_{\rm sub}$ is -1 or $+1$. These results reveal an asymmetric error behavior around decision levels, as depicted in Fig. 22(b) and (c). Due to the asymmetry, the widths of metastability regions denoted by ε_2 and ε_2' are unequal. In addition, (18) must now be rewritten as

$$P(E>E_1) \approx (\Delta V_1 + \Delta V_2)\left[f_{V_{\rm in}}\left(\frac{-V_{\rm REF}}{4}\right) + f_{V_{\rm in}}\left(\frac{+V_{\rm REF}}{4}\right)\right] \quad (32)$$

where,

$$|\Delta V_1| = \frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{\frac{V_{\rm REF}}{8}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}} \quad (33)$$

and

$$|\Delta V_2| = \frac{V_{\rm on}}{A_{\rm tot}}\left[\exp\left(\frac{T_{\rm conv}}{\tau_{\rm res}}\right)\frac{E_1}{\frac{3V_{\rm REF}}{8}}\right]^{-\tau_{\rm res}/\tau_{\rm reg}}. \quad (34)$$

Appendix II

Effect of Noise on Metastability

The effect of latch noise on the metastability of synchronizers has been found negligible [8]. In this appendix, we study this effect in the context of pipelined ADCs.

The comparator input-referred noise, $V_{\rm noise}$, has a Gaussian PDF, $f_{\rm noise}$, and is added to the input signal, $V_{\rm in}$. We assume $V_{\rm noise}$ and $V_{\rm in}$ to be independent and denote their sum by Z. The PDF of Z is given by the convolution of the two PDFs:

$$f_z(Z) = \int_{-\infty}^{+\infty} f_{V_{\rm in}}(Z-u)f_{\rm noise}(u)du. \quad (35)$$

Equation (17) is now rewritten as

$$P(E > E_1) = {\rm prob}\{|\Delta Z| < \Delta V_1\} \quad (36)$$

where ΔZ is the difference between $V_{\rm in}+V_{\rm noise}$ and the decision threshold of interest. Equation (18) then emerges as

$$P(E > E_1) \approx 2\Delta V_1\left[f_z\left(\frac{-V_{\rm REF}}{4}\right) + f_Z\left(\frac{+V_{\rm REF}}{4}\right)\right]. \quad (37)$$

To evaluate $f_z(Z)$ at $Z = \pm V_{\rm REF}/4$, we simplify (35) by noting that, if u is small, then $f_{V_{\rm in}}(Z) \approx f_{V_{\rm in}}(\pm V_{\rm REF}/4)$, and if u is large, then $f_{\rm noise}(u)$ is small. It follows that

$$f_Z\left(\frac{\pm V_{\rm REF}}{4}\right) \approx \int_{-\infty}^{+\infty} f_{V_{\rm in}}\left(\frac{\pm V_{\rm REF}}{4}\right)f_{\rm noise}(u)du \quad (38)$$

$$\approx f_{V_{\rm in}}\left(\frac{\pm V_{\rm REF}}{4}\right)\int_{-\infty}^{+\infty} f_{\rm noise}(u)du \quad (39)$$

$$\approx f_{V_{\rm in}}\left(\frac{\pm V_{\rm REF}}{4}\right). \quad (40)$$

We therefore conclude that (37) is close to (18), revealing that comparator noise has a negligible impact on the metastability of pipelined ADCs.

ACKNOWLEDGMENT

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