An RF Receiver for Intra-Band Carrier Aggregation

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***Abstract*—Carrier aggregation is an attractive approach to increasing the data rate in wireless communication. This paper describes an efficient carrier aggregation receiver architecture that employs one receive path and a single synthesizer. The block-downconversion scalable receiver translates all of the channels to the baseband and utilizes a new digital image rejection technique to reconstruct the signals. A receiver prototype realized in 45 nm CMOS technology along with an FPGA back end provides an image rejection ratio of at least 70 dB with a noise figure of 3.8 dB while consuming 15 mW.**

***Index Terms*—Block downconversion, broadband LNA, carrier aggregation, image rejection, LTE.**

I. Introduction

In ORDER to increase the data rate in wireless communication, two or more adjacent or non-adjacent RF channels can be "joined" together, thus proportionately raising the bandwidth and the capacity. Called "carrier aggregation" [1], this approach has been adopted by the long-term evolution (LTE) standard for cellular systems [2] and poses new RF design challenges. Specifically, the key question is whether for N carriers, one must employ N receivers, transmitters, frequency synthesizers, and baseband chains. It is therefore desirable to develop architectures that can reduce this multiplicity.

This paper proposes a "scalable" receiver architecture based on "block downconversion" and digital image rejection that can support two or more RF carriers using a single receive chain. A CMOS receiver along with an FPGA realization of the background image rejection calibration technique demonstrates a noise figure of 3.8 dB with a gain of 37 dB and an image rejection ratio (IRR) of at least 70 dB.

Section II provides the background for this work, presenting the LTE receiver specifications and the prior art. Section III describes the proposed architecture and Section IV the new image rejection algorithm. Sections V and VI deal with the receiver design and experimental results, respectively.

II. Background

Beyond exploiting bandwidth-efficient modulation schemes, the capacity of wireless links can be raised only by increasing the bandwidth. With the channelization predefined by each standard, this increase can be achieved through decomposing the data that is to be transmitted into two or more streams and impressing them on two or more carriers corresponding to different channels. The RF channels may belong to the same band ("intra-band aggregation") [Fig. 1(a)] or different bands ("inter-band aggregation") [Fig. 1(b)] [2]. In the former case, the channels can be adjacent to one another or not ("contiguous" and "non-contiguous" aggregation, respectively). In this paper, we consider intra-band aggregation and begin with two channels to illustrate various issues.

A. LTE Specifications

The LTE receiver requirements are different in the absence or presence of carrier aggregation. In this section, we describe the latter and, specifically, for intra-band aggregation.

For non-contiguous aggregation, LTE specifies a channel bandwidth of 5, 10, 15, 20 MHz with "reference" sensitivities of -96.5, -93.5, -91.7, -90.5 dBm for QPSK modulation, respectively, and an adjacent channel power 25.5 dB higher than that of the desired channel [Fig. 2(a)].[1] (In the case of contiguous aggregation, the minimum channel bandwidth is 10 MHz.) For other in-band blockers, the signal power is set to 12 dB above the reference sensitivity while the blocker has a power of -56 dBm if it is at 7.5 MHz offset or -44 dBm if at 12.5 MHz offset.[2] Fig. 2(b) and (c) depict examples of contiguous and non-contiguous aggregation for different frequency offsets and different desired channel bandwidths. LTE also stipulates a "narrowband" blocker test wherein an interferer at -55 dBm is applied at an offset of 0.2 MHz, and the desired signal is at a power level of 16 dB + reference sensitivity [Fig. 2(d)]. The maximum separation between the centers of two intra-band channels is 65 MHz.

To maximize spectral usage, LTE allows different bandwidths for the two channels [2] if part of the spectrum is already occupied by another user [Fig. 1(c)]. At the receiver input, that user's signal can be much stronger than the desired channels, thereby acting as a blocker or as an image. In addition, owing to frequency-dependent fading, the two desired channels may arrive with unequal power levels, exhibiting a difference of up to 10 dB for a 65 MHz separation at 2 GHz [3].

B. Prior Art

It is possible to dedicate one receiver and one synthesizer to each channel but with a direct power and area penalty. Moreover, with such a small relative frequency separation, the synthesizers must avoid injection pulling, thus dictating a complex

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[1]These sensitivity levels correspond to band 25 and are specified for intra-band non-contiguous carrier aggregation.

[2]Frequency offsets are with respect to the edge of the desired channel.

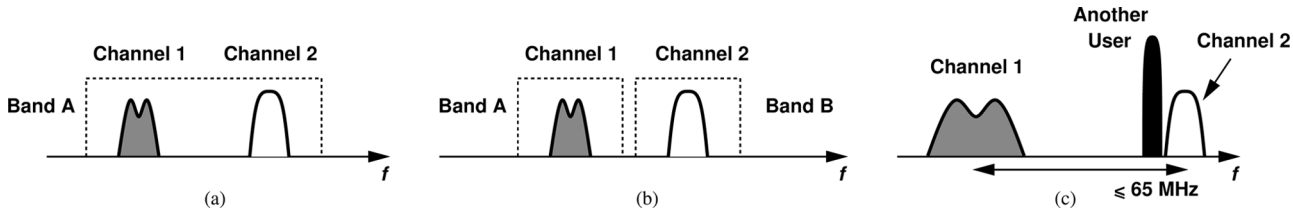


Fig. 1. (a) Intra-band carrier aggregation, (b) inter-band carrier aggregation, and (c) carrier aggregation in the presence of another user.

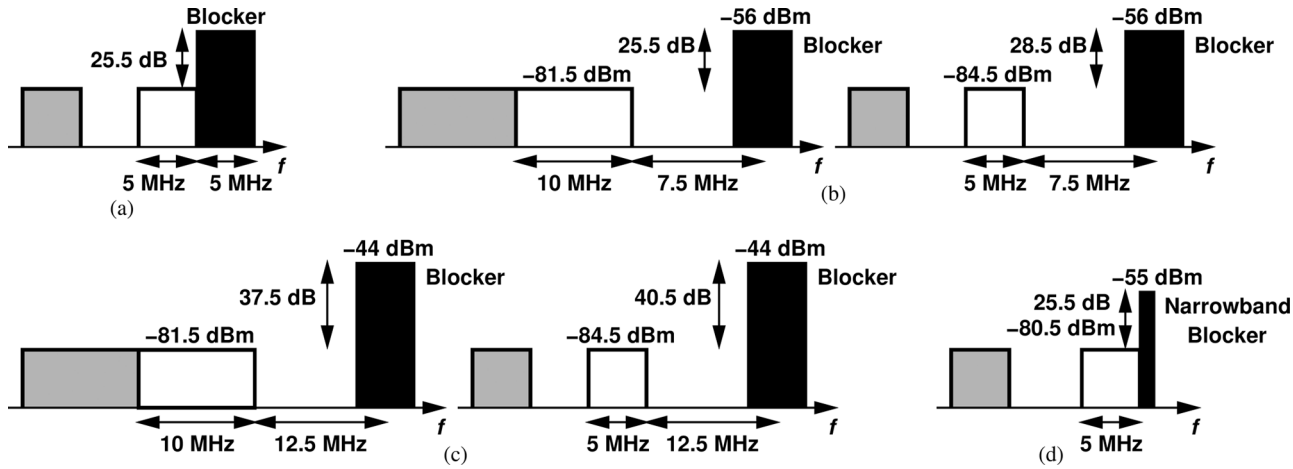


Fig. 2. LTE blocker profiles: (a) adjacent channel, (b) in-band blocking case 1, (c) in-band blocking case 2, and (d) narrowband blocking.

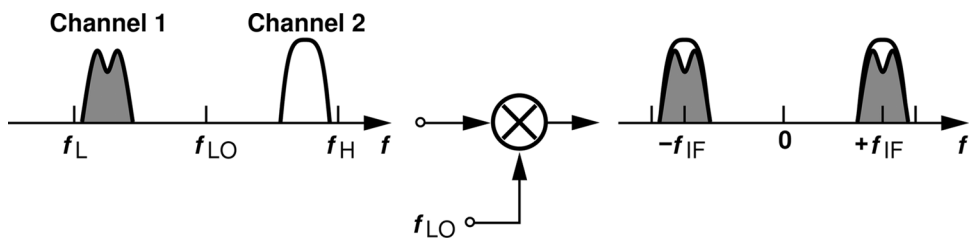


Fig. 3. Block downconversion with two aggregated channels.

frequency plan. For example, to obtain quadrature phases by division, one can operate at twice the channel-1 frequency and the other at four times the channel-2 frequency, but subharmonic or superhamonic injection pulling may still occur.

A more attractive approach is to perform "block downconversion" by a single receiver: the local oscillator (LO) frequency is placed midway between the two channels (Fig. 3), downconverting the entire spectrum from f_L to f_H and, inevitably, making channel 1 and channel 2 images of each other [4]. While avoiding the power and area penalty of dedicated paths, this method must provide a high image-rejection ratio because, as illustrated in Fig. 1(c), another user's strong signal may act as part of the image and fold onto channel 1 or 2 after downconversion. The image problem is addressed in [4]–[7] in the analog domain. Depicted in simplified form in Fig. 4, this (Weaver) architecture requires a second PLL as well as gain and phase adjustments within the harmonic-reject mixers so as to achieve a high IRR. We shall refer to the first and second downconversion mixers as RF and IF mixers, respectively.

The architecture of Fig. 4 entails three drawbacks. First, it cannot readily guarantee a high IRR across the maximum channel bandwidth (20 MHz in LTE). Second, the IF mixers in Fig. 4 must also suppress blockers that may coincide with the *harmonics* of the second LO. The design in [4] employs harmonic-reject IF mixers for this purpose.

The third drawback relates to the "scalability" of the architecture, i.e., the growth in power and area as more channels are aggregated. We observe in Fig. 4 that the image-reject/harmonic-reject mixers, the second LO, and the baseband filters and analog-to-digital converters (ADCs) must be duplicated for each additional channel.[3]

III. Proposed Receiver Architecture

A. Architecture

The block downconversion approach illustrated in Fig. 5 can avoid the foregoing three issues if the image rejection is performed in digital domain. Shown at a high level in Fig. 5, the

[3]Multiple-input multiple-output (MIMO) applications require duplication of the analog baseband circuits.

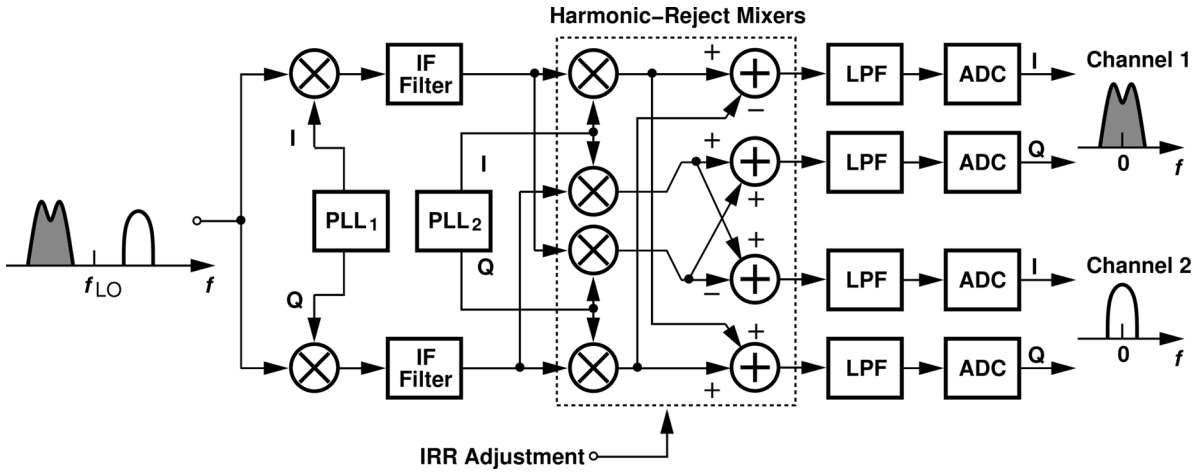


Fig. 4. Receiver in [4] for carrier aggregation.

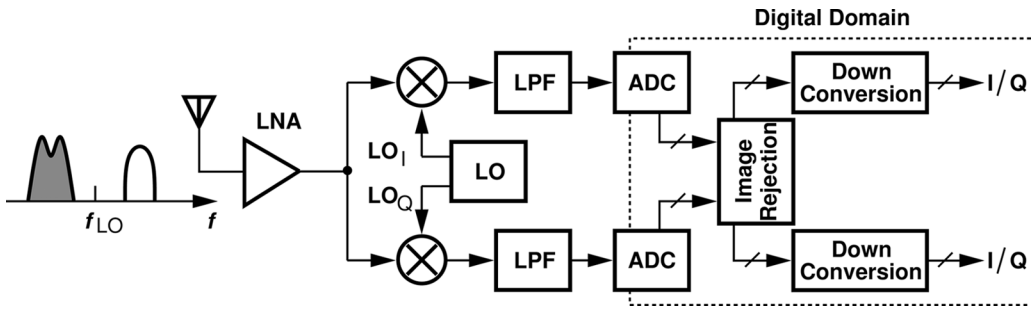


Fig. 5. Proposed block-downconversion receiver for carrier aggregation.

proposed architecture digitizes the quadrature IF signals, removes the image from each channel, and performs downconversion to baseband in the digital domain. The IRR calibration runs in the background (Section IV).

The proposed architecture deals with the three above issues as follows. First, as explained below, the digital image rejection technique inherently accounts for frequency-dependent I/Q mismatches. Second, the downconversions in the digital domain incorporate high-purity numerically controlled oscillators (NCOs), in essence multiplying the IF signals by sinusoids[4] and achieving harmonic-free mixing at much less cost and complexity than analog harmonic-reject mixers. Third, for each channel added to the aggregation, the proposed architecture requires one more digital downconverter and NCO, i.e., an area of about 150 μm $\times$ 150 μm and a power consumption of 0.3 mW in 45 nm technology (Section V).

B. ADC Requirements

The proposed architecture incorporates two ADCs to digitize the 35 MHz block of frequencies in the quadrature IF signals. We must then consider the feasibility and power consumption of these ADCs. Among the scenarios depicted in Fig. 2, that containing a -44 dBm in-band blocker demands the widest ADC dynamic range. (Out-of-band blocking will be discussed later). Let us normalize the voltage gain preceding the ADCs to 1. For a 64-QAM desired signal at a level of -84.5 dBm in a 5 MHz bandwidth, the quantization noise of the ADC must remain about 24 dB below the signal level for a reasonable bit error rate.[5] Denoting the ADCs' least-significant bit (LSB) size by Δ, we obtain this noise power as $[2(\Delta^2/12)/f_s] \times 5$ MHz, where f_s is the sampling rate. It follows that

$$10\log\left(\frac{2\Delta^2}{12f_s}\times 5\ \text{MHz}\right) = -84.5\ \text{dBm} - 24\ \text{dB}. \quad (1)$$

For example, if $f_s = 70$ MHz, then $\Delta = 7.7\ \mu$V.

The upper end of the ADCs' dynamic range is dictated by the -44 dBm blocker level, i.e., a full scale of 4 mV. (Of course, both the LSB size and the full scale should be multiplied by the receiver gain.) In addition, the spurs generated by such a blocker must also fall below -84.5 dBm $-$ 24 dB $\approx$ -109 dBm. We conclude that the ADCs must provide a resolution of 9 bits and a spurious-free dynamic range (SFDR) of -44 dBm $-$ $(-109$ dBm$)$ $=$ 65 dB, i.e., a linearity of about 11 bits. In practice, an additional margin of 10 dB is necessary to account for the RX front-end noise, peak-to-average power ratio of interferers and other imperfections.

Fortunately, recent advances in high-performance ADC design make our proposed solution a plausible one. For example, [9] reports a 14 bit, 80 MHz converter that achieves an SFDR

[4]Harmonic-reject mixers also equivalently multiply by an LO waveform that is free from some harmonics.

[5]In [8], the required error vector magnitude for 64-QAM is at least -22 dB.

of 80 dB at the Nyquist rate while consuming 31 mW. Such an ADC offers both a resolution and a dynamic range for exceeding the above results with a modest power consumption.

Operating in a full-duplex system, an LTE receiver must deal with the transmitter leakage, which can be as high as -20 dBm at 15 MHz below the RX band. This leakage and other out-of-band blockers can be attenuated by low-pass filters having a bandwidth of 35 MHz (not included in this work) after down-conversion to IF to the point that they are less than about 50 dB above the desired signal (e.g., around -30 dBm).

With a moderate attenuation of the out-of-band blockers, the ADC must cope with aliasing. To this end, one can utilize the oversampling ADC in [10], which achieves an SFDR of 77 dB at 37.5 MHz while drawing 39 mW.

IV. Proposed Image Rejection Algorithm

In the case of the LO frequency placed midway between the two aggregated carriers, the worst-case image rejection corresponds to the narrowband blocker scenario shown in Fig. 2(d) and a 64-QAM desired signal. The blocker must be rejected by at least -55 dBm $-(-80.5$ dBm -24 dB$) \approx 50$ dB. Nevertheless, when the number of wanted signals exceeds 2, the required IRR should be obtained from Fig. 2(c), resulting in -44 dBm $-(-84.5$ dBm -24 dB$) \approx 65$ dB.

A number of self-calibrating image rejection techniques have been reported [11]–[15]. Among these, [12] achieves the highest IRR, 62 dB, but it does not calibrate frequency-dependent I/Q mismatches, a critical issue if the signal and the image can appear anywhere in a wide bandwidth (from nearly zero to 35 MHz in our case).

A. Frequency-Dependent I/Q Mismatch

The I and Q signal paths following the first downconversion in Fig. 5 include various filtering sections. To appreciate the effect of frequency-dependent mismatches, let us consider a first-order low-pass RC network as a representative circuit. If the resistor and capacitor mismatches between the I and Q paths produce a small pole frequency mismatch of $\Delta\omega_0$, then the corresponding transfer functions can be written as $H_I(s) = (1 + s/\omega_0)^{-1}$ and $H_Q(s) = [1+s/(\omega_0+\Delta\omega_0)]^{-1}$, yielding a gain mismatch of $\epsilon = |H_Q|/|H_I|-1 \approx (\Delta\omega_0/\omega_0)\omega^2/(\omega^2+\omega_0^2)$ and a phase mismatch of $\theta = \tan^{-1}(\omega/\omega_0) - \tan^{-1}[\omega/(\omega_0+\Delta\omega_0)] \approx \omega\Delta\omega_0/(\omega^2+\omega_0^2)$. It follows that $\text{IRR}^{-1} \approx (\epsilon^2+\theta^2)/4 \approx (1/4)[\omega^2/(\omega^2+\omega_0^2)](\Delta\omega_0/\omega_0)^2$. As an example, Fig. 6 plots $10\log(\text{IRR})$ across the band for $\Delta\omega_0/\omega_0 = 2\%$, displaying considerable deterioration as the frequency exceeds one-tenth of the pole frequency. We therefore observe the extremely tight matching necessary for maintaining an IRR of greater than, say, 60 dB across the band.

It is possible to employ multi-tap adaptive filters to calibrate the mismatches in the background [15], but the analysis in [16] proves the existence of a "phantom" solution and the resulting convergence issues. For this reason, [15] limits the number of taps to two, affording frequency response correction at only two points.

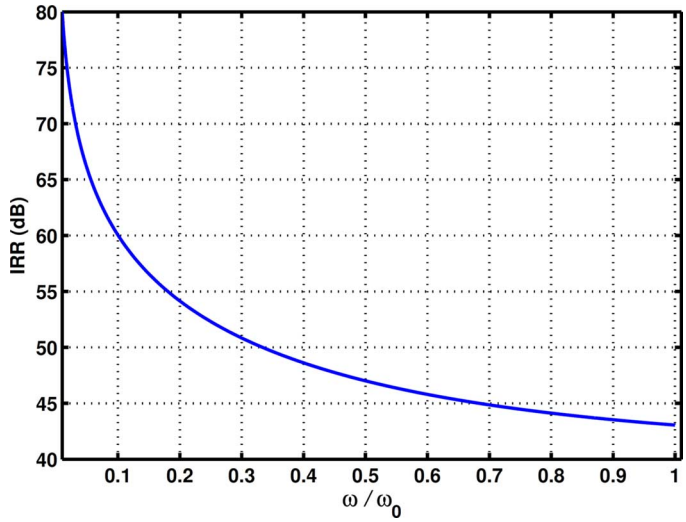


Fig. 6. Frequency-dependent image rejection ratio for $\Delta\omega_0/\omega_0 = 2\%$.

B. Proposed Algorithm

Consider the perfectly balanced downconverter shown in Fig. 7(a), where two channels A and B are received and translated to one IF.[6] In order to visualize the image components, we examine the complex signal, $I(\omega) - jQ(\omega)$, which carries A and B in negative and positive frequencies, respectively. With perfect matching, A and B are free from each other's images. To produce the baseband signals, the I and Q signals can be downconverted again using an LO frequency equal to ω_{IF} and properly combined. For example, the in-phase baseband component of A, $x_{A,I}(t)$, is obtained by forming $I(t)\cos\omega_{\text{IF}}t + Q(t)\sin\omega_{\text{IF}}t$ and low-pass filtering the result.

In the presence of gain and phase mismatches, as modeled in Fig. 7(b) by ϵ and θ, respectively, the composite signal $I(\omega) - jQ(\omega)$ exhibits a finite corruption of A by B and vice versa. This corruption is given by a coefficient equal to $\epsilon\exp(j\theta)$.

Let us now make a key observation: two of the spectral components of $Q(\omega)$ in Fig. 7(b) are multiplied by $\alpha = (1+\epsilon)\exp(j\theta)$. We thus surmise that, if the spectral components of $I(\omega)$ are also subjected to the same scaling factor, then the images may be removed. As illustrated in Fig. 7(c), we multiply $I(\omega)$ by $(1+\epsilon)\exp(j\theta)$ in the frequency domain,[7] obtaining a signal that upon combining with Q, cancels the images.

The proposed method can simplify the problem of image rejection, and, more generally, I/Q calibration. However, we must first develop a means of measuring α in the background. An important point in our proposition is that ϵ and θ need not be measured individually for α to be computed. Let us assume that the digitized I and Q signals are first applied to FFT engines, providing $I(\omega)$ and $Q(\omega)$ as the only observable quantities. We wish to obtain α in terms of $I(\omega)$ and $Q(\omega)$. If P_A and P_B respectively denote the total power of the A and B channels in Fig. 7(c), we recognize that the average power of $|I(\omega)|$ is in fact

[6]We use the notations A and B to refer to both the RF channels and the IF channels.

[7]Frequency-domain multiplication is denoted by a cross in a square to avoid confusion with time-domain multiplication.

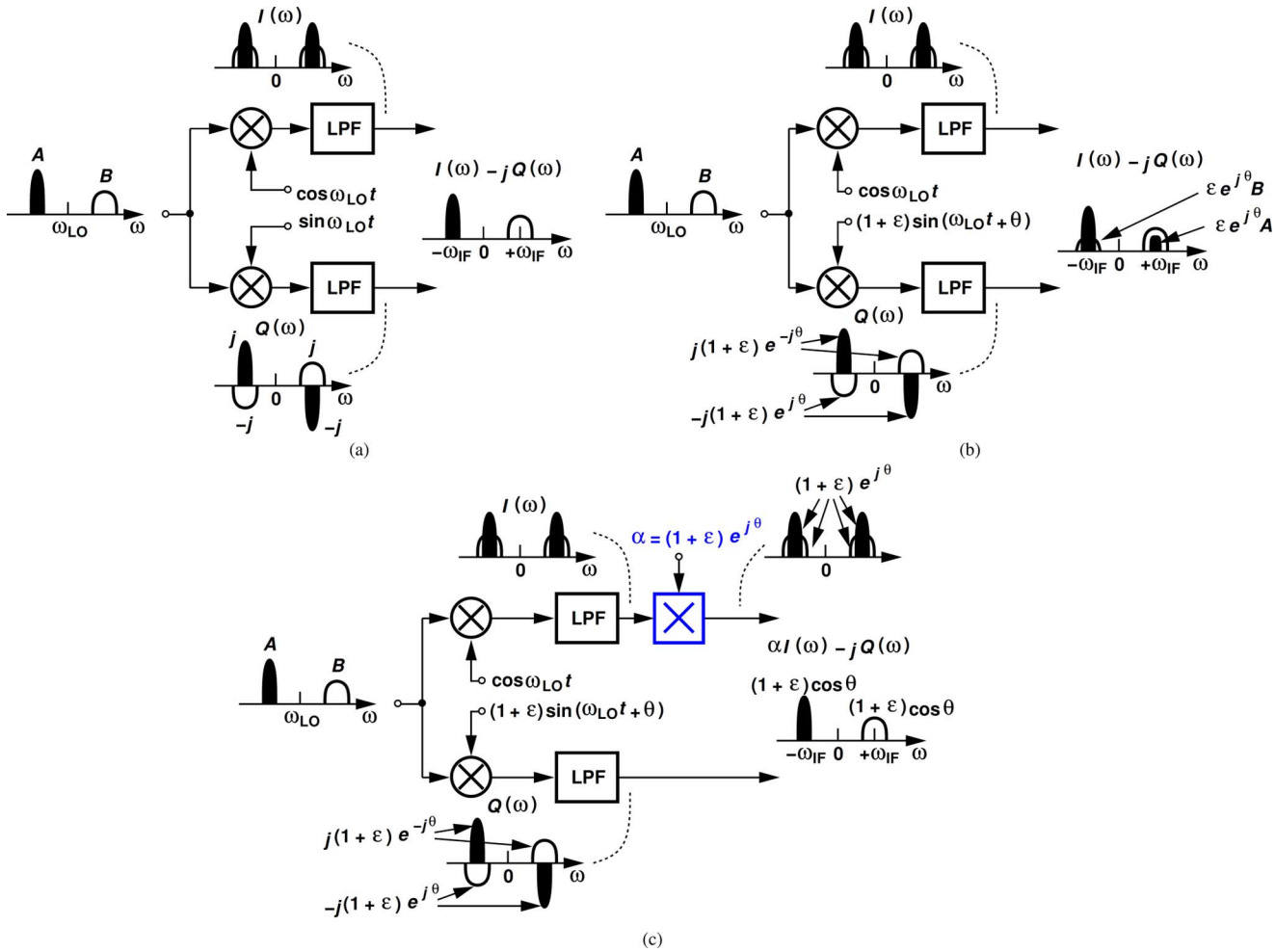


Fig. 7. (a) Ideal image-reject receiver, (b) image problem due to I/Q mismatch, and (c) proposed image rejection technique.

equal to $E\{|I(\omega)|^2\} = P_A + P_B$, where $E\{\cdot\}$ is the expectation value, the gain from the antenna to the ADC output is normalized to unity, and A and B are assumed statistically independent. Similarly, $E\{|Q(\omega)|^2\} = (1+\epsilon)^2(P_A + P_B)$. In addition, it can be shown that the average value of the inner product of $I(\omega)$ and $Q(\omega)$ is given by $E\{I(\omega) \cdot Q(\omega)\} = (1+\epsilon)(P_A + P_B)\sin\theta$. We thus express $\alpha = (1+\epsilon)\cos\theta + j(1+\epsilon)\sin\theta$ as

$$Im\{\alpha\} = \frac{E\{I(\omega) \cdot Q(\omega)\}}{E\{|I(\omega)|^2\}} \tag{2}$$

$$Re\{\alpha\} = \sqrt{\frac{E\{|Q(\omega)|^2\}}{E\{|I(\omega)|^2\}} - \left[\frac{E\{I(\omega) \cdot Q(\omega)\}}{E\{|I(\omega)|^2\}}\right]^2}. \tag{3}$$

While appearing computationally formidable, (2) and (3) allow us to calculate α so long as the I and Q signals are not zero.

Fig. 8 summarizes the necessary digital operations at a high level. In order to reproduce the corrected $I(t)$, an inverse FFT (IFFT) engine follows the complex scaling operation. If the functions prescribed by (2) and (3) can be realized at an acceptable cost, then background image rejection (or I/Q calibration) is achieved entirely in the digital domain. Remarkably, since $Im\{\alpha\}$ and $Re\{\alpha\}$ can be calculated for each FFT bin, the frequency-dependent mismatches are corrected with a fine frequency resolution. We also observe that the complexity in Fig. 8 is independent of the number of aggregated channels.

The accuracy with which α is calculated trades with the time over which $Im\{\alpha\}$ and $Re\{\alpha\}$ are averaged. In this work, the averaging time is about 1 ms to ensure a minimum IRR of 70 dB.

V. Receiver Design

Fig. 9 shows the experimental receiver designed and implemented in this work as a demonstration vehicle. The receiver consists of 1) a CMOS prototype realizing the RF front-end and baseband amplification, 2) off-the-shelf low-pass filters and ADCs, and 3) an FPGA implementation of the image rejection algorithm and IF downconverters. The ADCs have a nominal resolution of 14 bits and a maximum sampling rate of 250 MHz [17] (but run at 50 MHz here due to the setup constraints). The RF front-end receives an external LO signal at twice the desired carrier frequency and generates the 25% LO phases that drive the mixers.

Shown in Fig. 10, the front-end consists of a broadband LNA, passive mixers, and transimpedance amplifiers (TIAs). The sections below describe the analysis and design of the receiver building blocks.

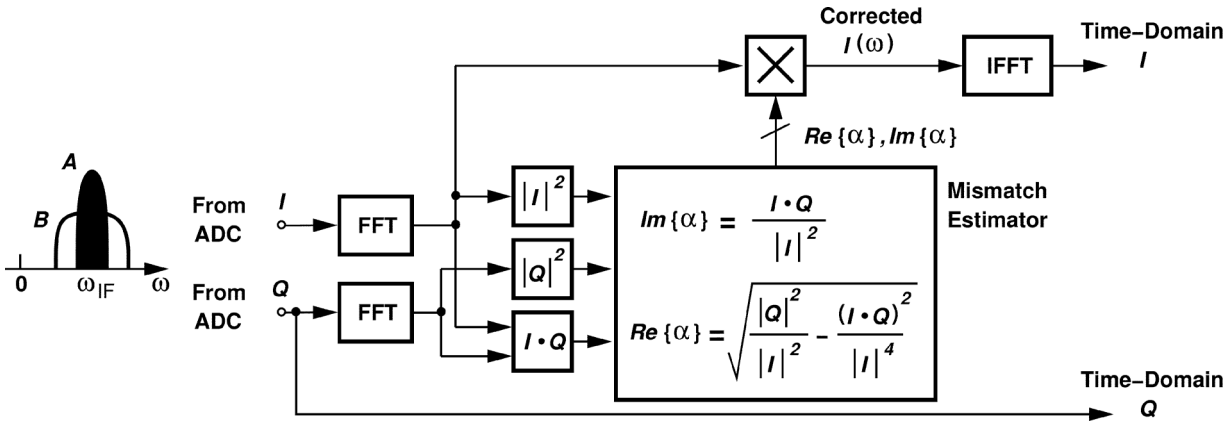


Fig. 8. Proposed image-reject algorithm.

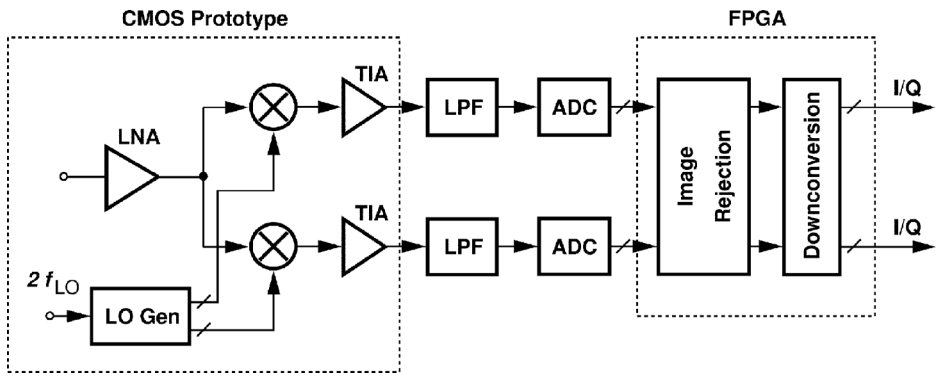


Fig. 9. Experimental receiver implementation.

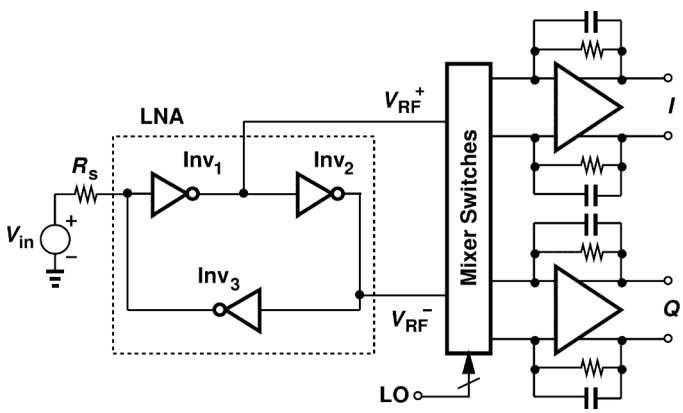


Fig. 10. Proposed RF front-end circuit.

A. Proposed Low-Noise Amplifier

The use of CMOS inverters as LNAs goes back to the early 1990s [18] and has also been practiced in a number of other topologies [19], especially as a G_m stage preceding current-driven mixers. We seek an inductor-less LNA that performs single-ended to differential conversion, provides input matching, and operates with a low supply. It has been suggested that a multi-stage LNA with feedback exhibits input matching with a wide bandwidth [20]. We therefore propose the topology shown in Fig. 11(a), where active feedback by means of Inv_3 affords a low noise figure and broadband matching. In this circuit, R_{mix} denotes the input resistance of the downconversion mixers and is chosen low ($\approx 50\ \Omega$) so as to minimize the LNA internal voltage swings, thereby improving its linearity in a manner similar to other topologies [19]. The RF signals at nodes X and Y are approximately differential.

With the low value of R_{mix}, the boundary between the LNA and the mixers begins to diminish as most of the RF currents produced by Inv_1 and Inv_2 are absorbed by the mixers. Nonetheless, we first analyze the stand-alone LNA and then explore the properties of the LNA/mixer cascade. The analysis and design of the circuit begin with enforcing input matching and the hope that the resulting voltage gain and noise figure will be acceptable.

For the input resistance to be equal to R_S, we arrive at the following condition $G_{m1}R_{\mathrm{mix}}G_{m2}R_{\mathrm{mix}}G_{m3}R_S = 1$, where channel-length modulation is neglected. We then obtain the closed-loop voltage gains to nodes X and Y as $|V_X/V_{\mathrm{in}}| = G_{m1}R_{\mathrm{mix}}/2$ and $|V_Y/V_{\mathrm{in}}| = G_{m1}R_{\mathrm{mix}}G_{m2}R_{\mathrm{mix}}/2$. It follows that the currents delivered to the mixers at X and Y are equal to $(G_{m1}/2)V_{\mathrm{in}}$ and $(G_{m1}G_{m2}R_{\mathrm{mix}}/2)V_{\mathrm{in}}$, respectively. For V_X and V_Y to be differential, $G_{m2}R_{\mathrm{mix}} = 1$.

B. LNA Biasing

While offering flexibility in the design, the LNA's three inverters experience considerable PVT-induced variation in their bias current. It is possible to define the bias current by placing

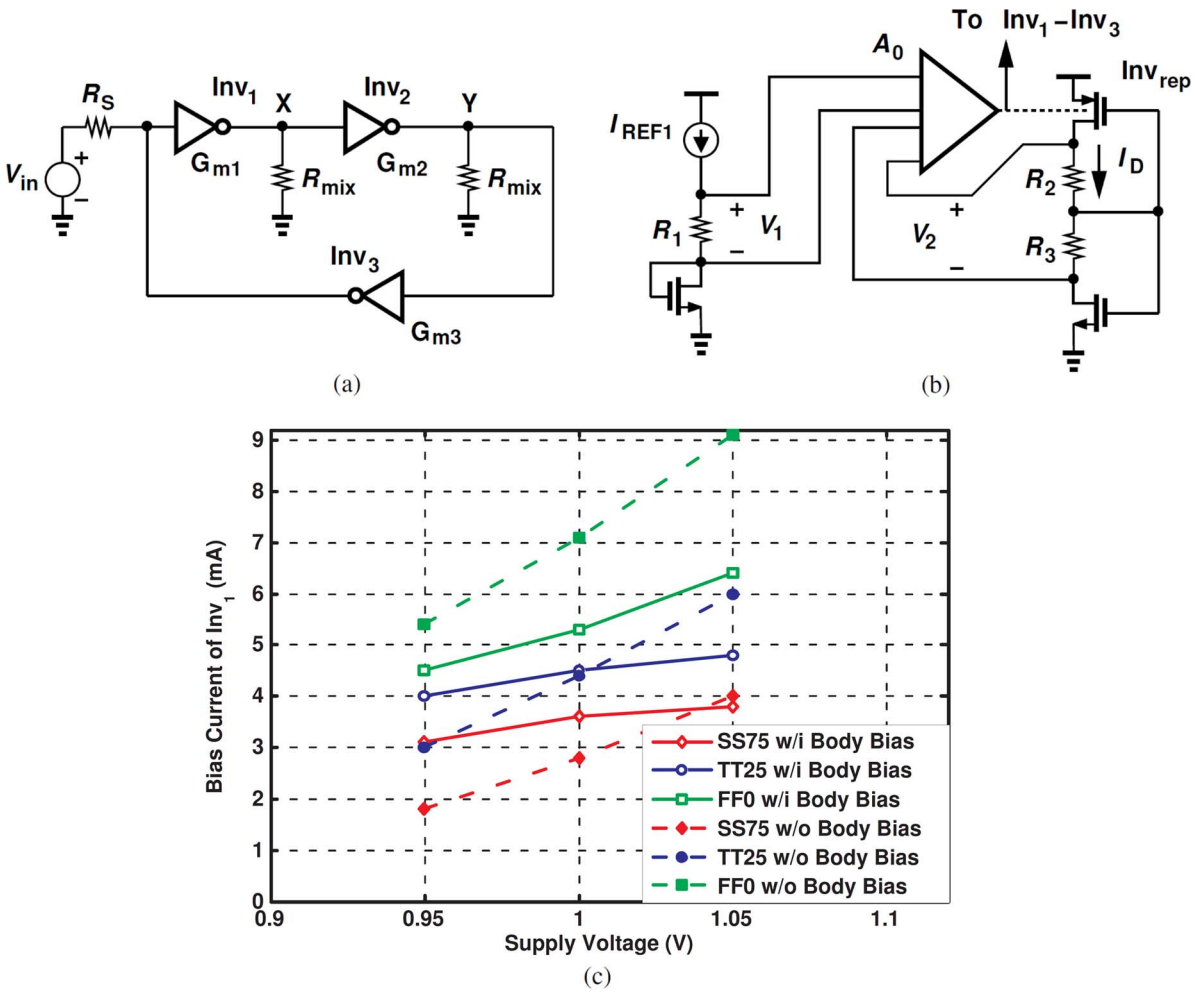


Fig. 11. (a) Proposed LNA topology, (b) PMOS body bias circuit, and (c) bias current of $\mathrm{Inv_1}$ with and without PMOS body bias.

a current source in series with the PMOS or NMOS devices [21] but at the cost of voltage headroom and hence linearity. We propose a method of controlling the bias that does not sacrifice headroom.

Illustrated in Fig. 11(b), the idea is to adjust the bias current of a replica inverter, $\mathrm{Inv_{rep}}$, through the PMOS body voltage. To achieve a well-defined value for I_D, a servo loop consisting of A_0 forces the voltage $V_2 = (R_2 + R_3)I_D$ to be equal to $V_1 = R_1 I_{\mathrm{REF1}}$ and hence $I_D = [R_1/(R_2 + R_3)]I_{\mathrm{REF1}}$. The output voltage of A_0 drives the PMOS bodies of $\mathrm{Inv_1 - Inv_3}$, faithfully copying I_D onto the three stages if mismatches are acceptably small.

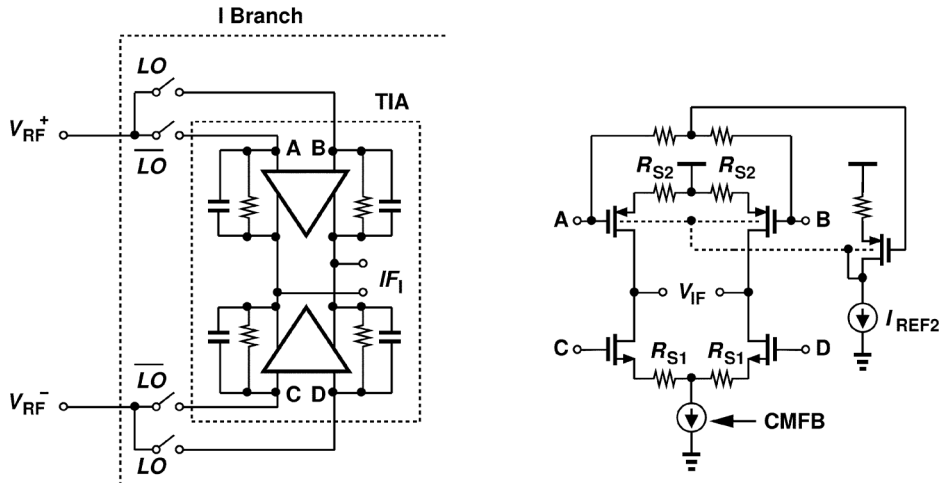
Due to channel-length modulation, V_2 must be small enough to avoid a large mismatch between $\mathrm{Inv_{rep}}$ and $\mathrm{Inv_1}$-$\mathrm{Inv_3}$. On the other hand, V_2 must be sufficiently larger than the input offset of A_0. In this work, $V_2 = 150$ mV as a compromise and $A_0 = 16.5$. Fig. 11(c) plots the simulated bias current of $\mathrm{Inv_1}$ as a function of V_{DD} for several process and temperature corners with and without the servo loop, revealing a fourfold reduction provided by the proposed technique. Although the bias current still varies considerably, the input matching, voltage gain, and noise figure are relatively constant because the input impedance of the mixers also varies but in a favorable direction.

C. TIA Design

The design of the TIA is influenced by the LNA and mixers. Since random mismatches in Fig. 10 may create a difference between the dc levels of V_{RF}^{+} and V_{RF}^{-}, the mixer switches carry a dc current, thereby producing substantial flicker noise. With the low impedance seen at the input of the mixers, capacitive coupling proves difficult, especially at the lower edge of the LTE band (700 MHz). This issue is resolved through the use of two TIAs as shown in Fig. 12(a) so as to isolate V_{RF}^{+} and V_{RF}^{-}. In this case, the mismatch between the TIAs' common-mode level and the dc level of V_{RF}^{+} or V_{RF}^{-} does produce a dc current through the switches, but this current is limited by the TIA's feedback resistor. For example, a 50 mV dc difference generates 10 μA and hence negligible flicker noise.

To avoid doubling the bias current as a result of decomposing the TIA into two, we implement the two using different MOSFET types and share their bias current, as shown in Fig. 12(b). Due to limited voltage headroom, the PMOS pair's bias is defined through its body rather than by a tail current source.

The required third-order intercept point $(\mathrm{IIP_3})$ can be derived from Fig. 13. According to [2], the desired signal at -84.5 dBm



(a) (b)

Fig. 12. (a) Separate TIAs to avoid DC current and (b) amplifier implementation.

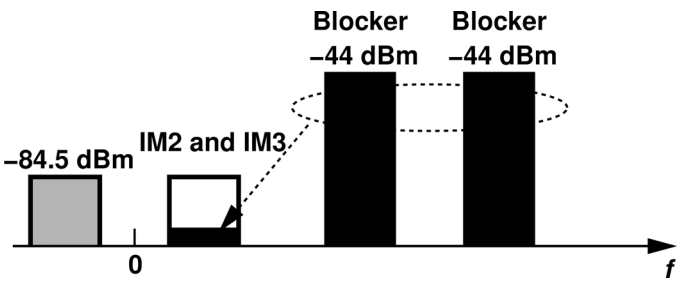


Fig. 13. Intermodulation in the baseband.

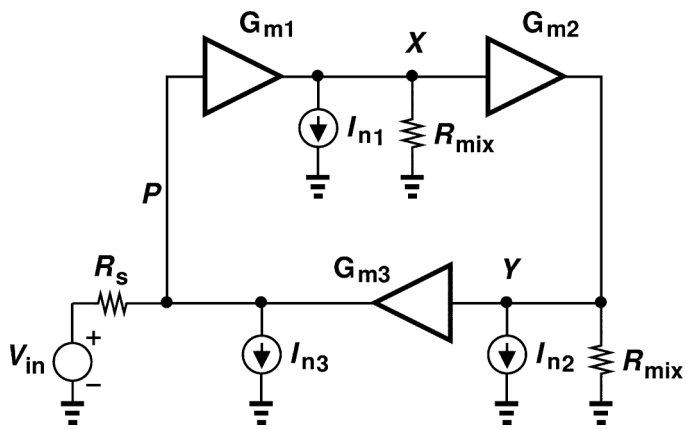


Fig. 14. LNA noise model.

could be accompanied by a -44 dBm in-band blocker. The intermodulation term should be below the desired signal by about 24 dB for 64-QAM modulation. We conclude that the required receiver IIP_3 should exceed -12 dBm. The degeneration resistors, $R_{S1} = 30\ \Omega$ and $R_{S2} = 60\ \Omega$, in Fig. 12(b) and a bias current of 2 mA establish the requisite linearity.

D. Single-Ended Noise Analysis

In this and the next sections, we analyze the noise performance of the receiver and demonstrate an important property of the LNA. The analysis proceeds in three steps: (1) downconvert the broadband LNA noise to the IF, (2) add the TIA noise to the result, and (3) refer the overall RX output noise to the LNA input and determine the NF. While the method in [24] is also applicable here, our approach more easily allows the inclusion of the baseband stages following the TIA. As explained in the previous section, we assume $G_{m2}R_{\mathrm{mix}} = 1$ and $G_{m1}G_{m2}G_{m3}R_{\mathrm{mix}}^2R_S = 1$, i.e., $G_{m3}R_S = (G_{m1}R_{\mathrm{mix}})^{-1}$.

Fig. 14 shows the LNA circuit and the noise components, $I_{n1} - I_{n3}$, contributed by $\mathrm{Inv}_1 - \mathrm{Inv}_3$, respectively. We assume the TIA is single-ended and connected to X. Since the impedance seen at X is equal to $R_{\mathrm{mix}}/(1 + G_{m1}G_{m2}G_{m3}R_{\mathrm{mix}}^2R_S) = R_{\mathrm{mix}}/2$, the noise voltage at this node due to I_{n1} is equal to $I_{n1}R_{\mathrm{mix}}/2$. We also multiply the noise voltage at P, $I_{n3}R_S/2$, by $G_{m1}R_{\mathrm{mix}}$ and that at Y, by $G_{m3}R_SR_{m1}R_{\mathrm{mix}}$, obtaining the noise voltage at X due to I_{n3} and I_{n2}. The total noise at this node thus equals

$$\overline{V_{n,X}^2} = \frac{R_{\mathrm{mix}}^2}{4}\left[\overline{I_{n1}^2} + \overline{I_{n2}^2} + (G_{m1}R_S)^2\overline{I_{n3}^2}\right]. \quad (4)$$

To downconvert the above RF noise to IF, we construct the model shown in Fig. 15(a), where R_{LNA} denotes the LNA output impedance and R_{SW} the switch on-resistance. The IF devices R_{TIA} and C_1 represent the single-ended input impedance of the TIA. Since $R_{\mathrm{LNA}} \approx R_{\mathrm{mix}}$, the noise voltage source is modeled as $2V_{n,X}$, yielding $V_{n,X}$ at node M (which would be the same as node X in Fig. 14). In this design, $R_{\mathrm{TIA}}C_1$ ($= 25$ ns) is much greater than the LO period, T_{LO}, so as to maximize the receiver voltage gain.

The principal difficulty facing our noise analysis is that the broadband LNA produces noise at the harmonics of the LO, and the input impedance of the downconversion mixers *varies* substantially at these harmonics. In this design, both $R_{\mathrm{TIA}}C_1 \gg T_{\mathrm{LO}}$ and $(R_{\mathrm{LNA}} + R_{\mathrm{SW}})C_1 \gg T_{\mathrm{LO}}$, leading to current-driven

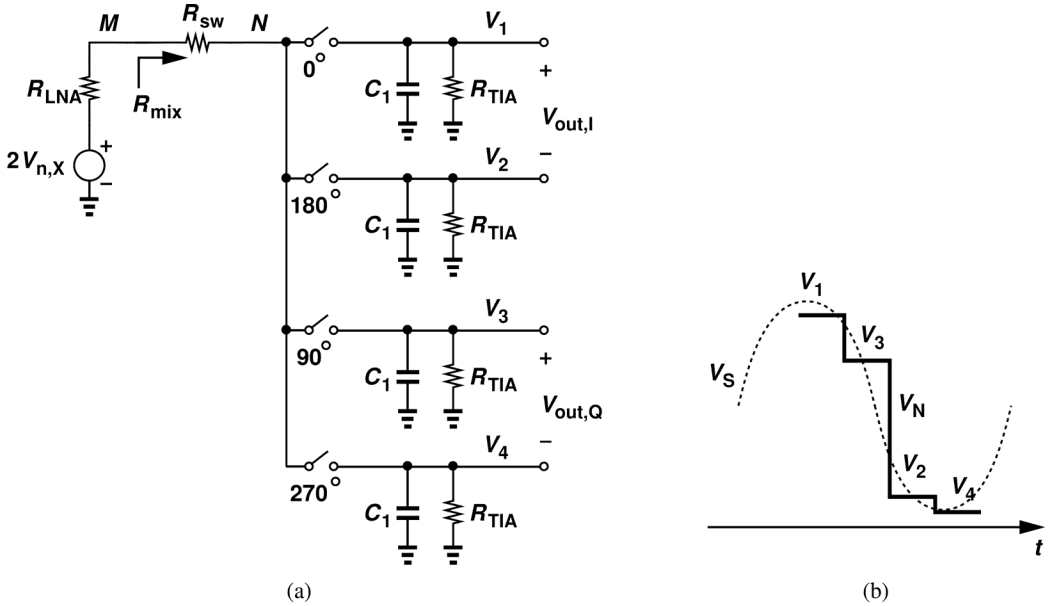


Fig. 15. Downconversion noise model.

mixing. To determine the conversion gain at different harmonic frequencies, let us replace the noise source in Fig. 15(a) with $V_S = V_0 \cos(N\omega_{\rm LO}t)$ and examine the waveform at node N. Due to the condition $(R_{\rm LNA} + R_{\rm SW})C_1 \gg T_{\rm LO}$, the output voltages vary by a small amount when each switch turns on. We equate the charge lost by C_1 through $R_{\rm TIA}$ in the hold mode to the charge delivered by V_S to C_1 in the tracking mode [24]:

$$\frac{V_k T_{\rm LO}}{R_{\rm TIA}} = \int_{t_1}^{t_2} \frac{V_S - V_k}{R_{\rm LNA} + R_{\rm SW}} dt \ (k = 1, \ldots, 4), \quad (5)$$

where $t_2 - t_1 = T_{\rm LO}/4$. It can be proved that the amplitude of the differential IF outputs in Fig. 15(a) is given by

$$\begin{aligned} |V_1 - V_2| &= |V_3 - V_4| \\ &= \frac{1}{N}\frac{4\sqrt{2}}{\pi}\frac{R_{\rm TIA}V_0}{R_{\rm TIA} + 4R_{\rm LNA} + 4R_{\rm SW}} \text{ odd } N, \\ &= 0 \text{ even } N. \end{aligned} \quad (6)$$

This result suggests that the downconversion to differential outputs has the same $1/N$ gain dependence as simple return-to-zero passive 50%-duty-cycle mixers but with a different coefficient. The broadband noise power at odd LO harmonics can therefore be multiplied by $1 + 1/3^2 + 1/5^2 + \cdots = \pi^2/8$ and the square of $(4\sqrt{2}/\pi)R_{\rm TIA}/(R_{\rm TIA} + 4R_{\rm LNA} + 4R_{\rm SW})$.

From the foregoing observations and noting that $R_{\rm LNA}$ in Fig. 15 is equal to $R_{\rm mix}$, we can express the downconverted LNA noise appearing in $V_{\rm out,I} = V_1 - V_2$ as

$$\overline{V_{n,I}^2} = \frac{4\pi^2}{8}\left(\frac{4\sqrt{2}}{\pi}\frac{R_{\rm TIA}}{R_{\rm TIA} + 4R_{\rm LNA} + 4R_{\rm SW}}\right)^2 \overline{V_{n,X}^2}, \quad (7)$$

which, from (4), reduces to

$$\overline{V_{n,I}^2} = 4\left(\frac{R_{\rm TIA}}{R_{\rm TIA} + 4R_{\rm LNA} + 4R_{\rm SW}}\right)^2 R_{\rm mix}^2\left[\overline{I_{n1}^2} + \overline{I_{n2}^2} + (G_{m1}R_S)^2\overline{I_{n3}^2}\right]. \quad (8)$$

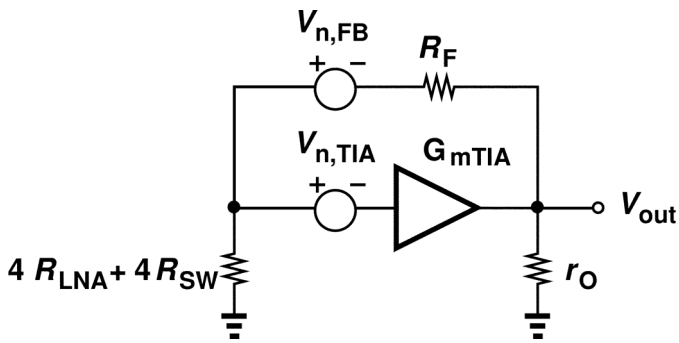


Fig. 16. Model for TIA noise calculation.

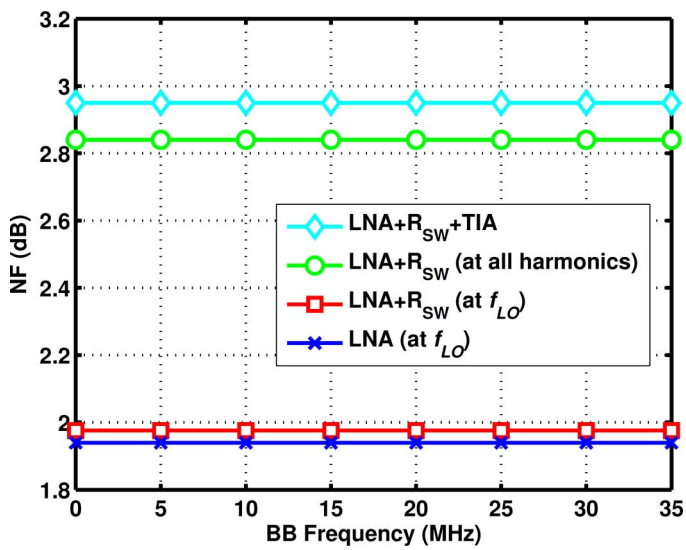


Fig. 17. Noise figure simulation results.

The baseband noise of $R_{\rm SW}$ is downconverted in the same manner:

$$\overline{V_{n,out,SW}^2} = 4\overline{V_{n,SW}^2}\left(\frac{R_{\rm TIA}}{R_{\rm TIA} + 4R_{\rm LNA} + 4R_{\rm SW}}\right)^2, \quad (9)$$

where $\overline{V_{n,SW}^2} = 4kTR_{\rm SW}$.

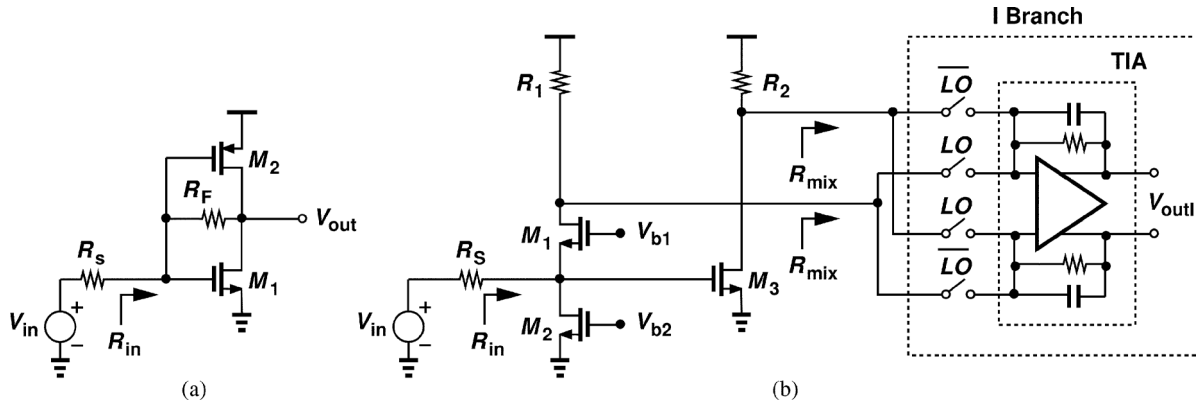


Fig. 18. (a) Resistive-feedback LNA and (b) noise-cancelling LNA.

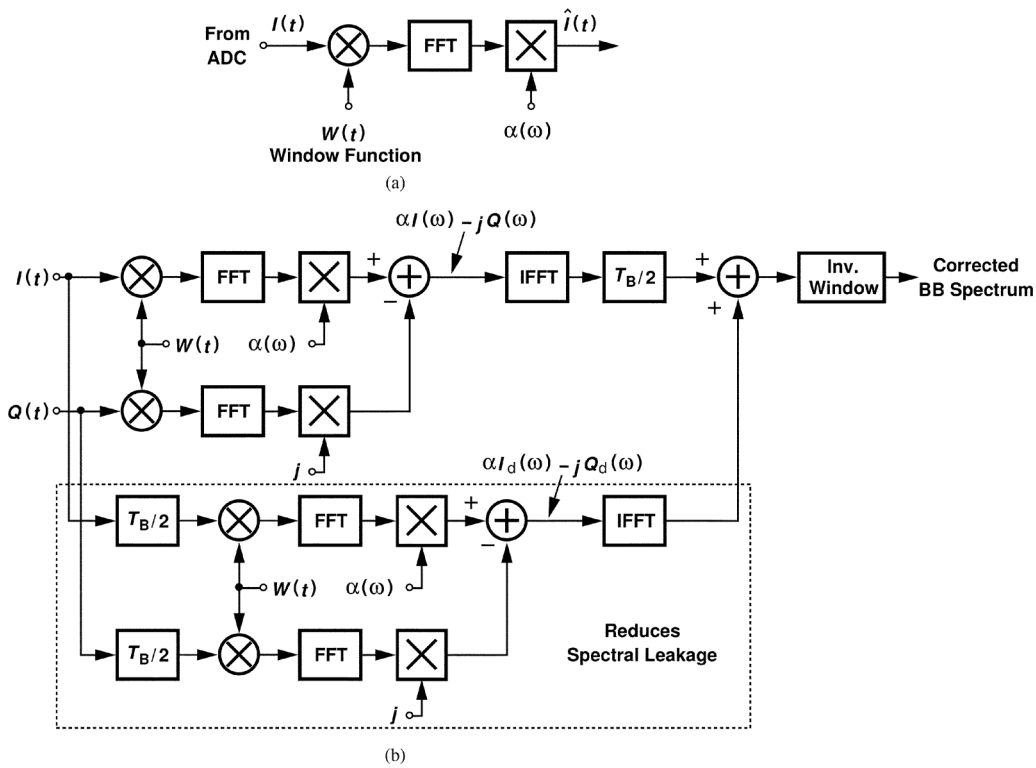


Fig. 19. (a) Window function multiplication, and (b) shifting path to suppress spectral leakage.

We must now calculate the noise contributed by the TIA. As shown in Fig. 16, with a 25% duty cycle, each single-ended input of the TIA sees an equivalent driving impedance of $4R_{\rm LNA} + 4R_{\rm SW}$. The output noise arising from R_F and the core amplifier can be expressed as

$$\overline{V_{n,out}^2}|_{\rm res+amp} = \frac{[1 + G_{m\rm TIA}(4R_{\rm LNA} + 4R_{\rm SW})]^2}{D^2}\overline{V_{n,FB}^2} + \frac{G_{m\rm TIA}^2(R_F + 4R_{\rm LNA} + 4R_{\rm SW})^2}{D^2}\overline{V_{n,\rm TIA}^2}, \quad (10)$$

where $D = 1 + G_{m\rm TIA}(4R_{\rm LNA} + 4R_{\rm SW}) + (R_F + 4R_{\rm LNA} + 4R_{\rm SW})/r_O$. The total output noise is equal to the components given by (8) and (9) times A_0^2 plus that given by (10), where A_0 is the voltage gain from the input of the core amplifier to its output. The voltage gain from the antenna to the TIA output is given by

$$A_{\rm tot} = G_{m1}R_{\rm mix}\left(\frac{4\sqrt{2}}{\pi}\frac{R_{\rm TIA}}{R_{\rm TIA} + 4R_{\rm mix} + 4R_{\rm SW}}\right)A_{\rm TIA}. \quad (11)$$

We must now divide the output noise by $4kTR_SA_{\rm tot}^2$ and substitute for $\overline{I_{n1,2,3}^2}$ to find the noise figure. We have in Fig. 14: $\overline{I_{n1}^2} = 4kT\gamma G_{m1}$ with no contribution from $R_{\rm mix}$ because

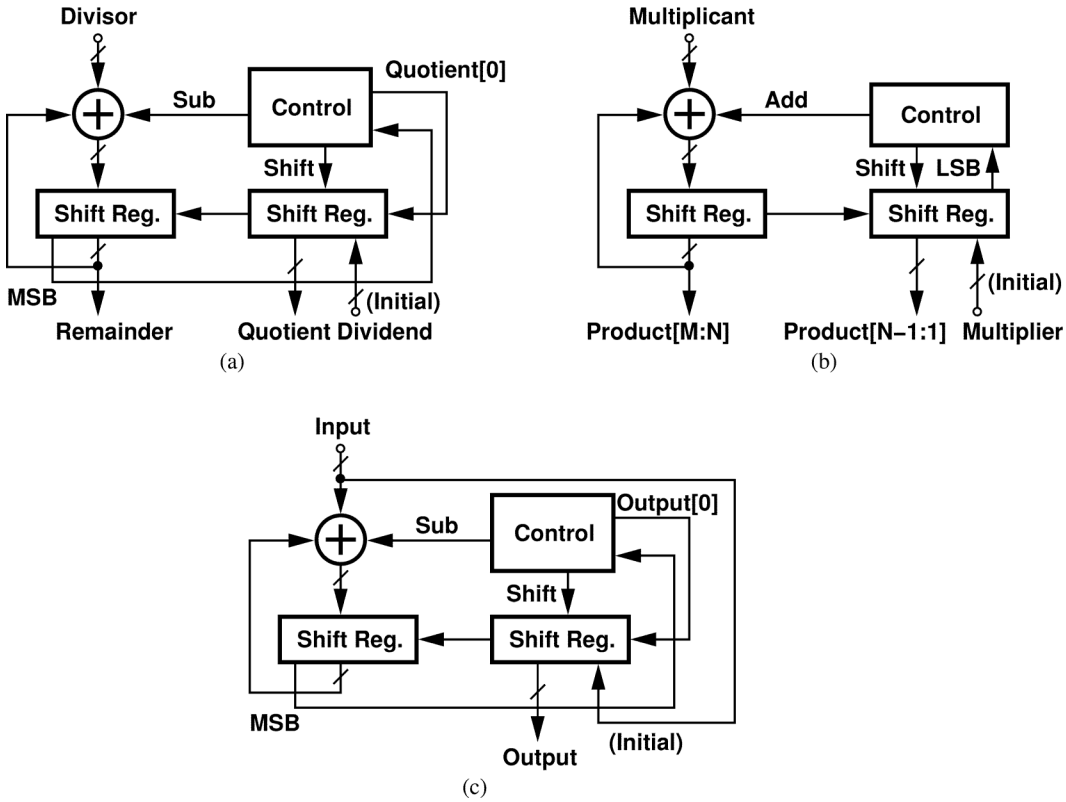


Fig. 20. Bit-serial arithmetic implementations of (a) division, (b) multiplication, and (c) square root functions.

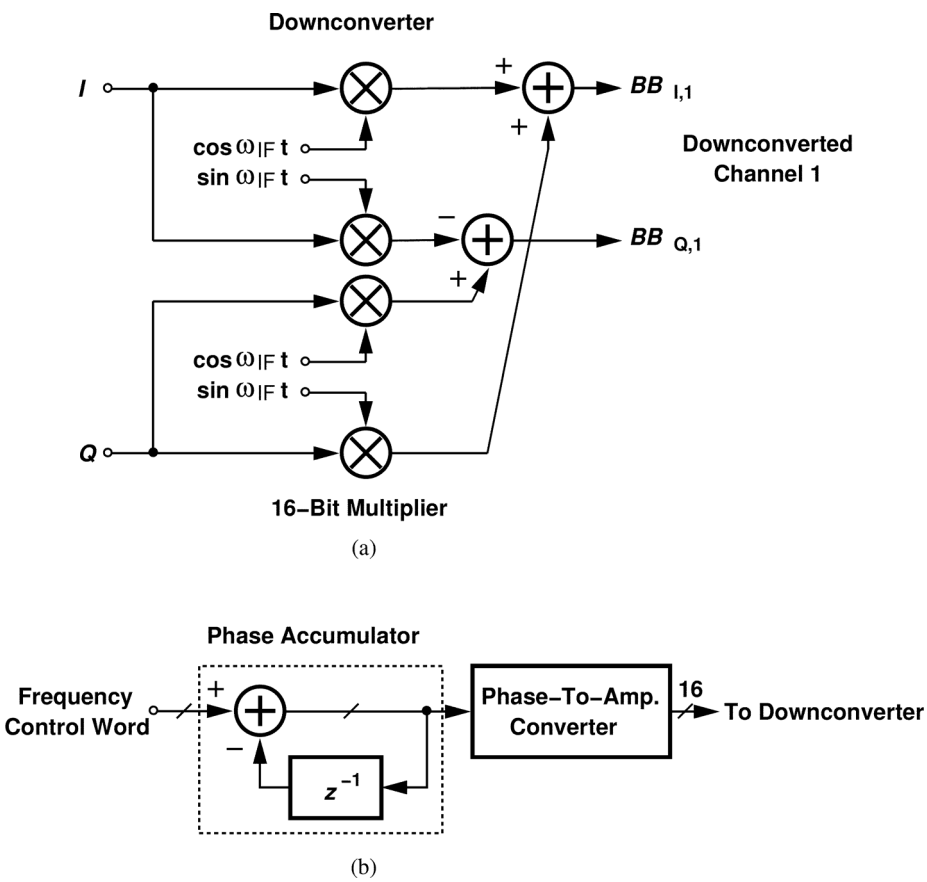


Fig. 21. (a) Digital downconverter, and (b) numerically-controlled oscillator.

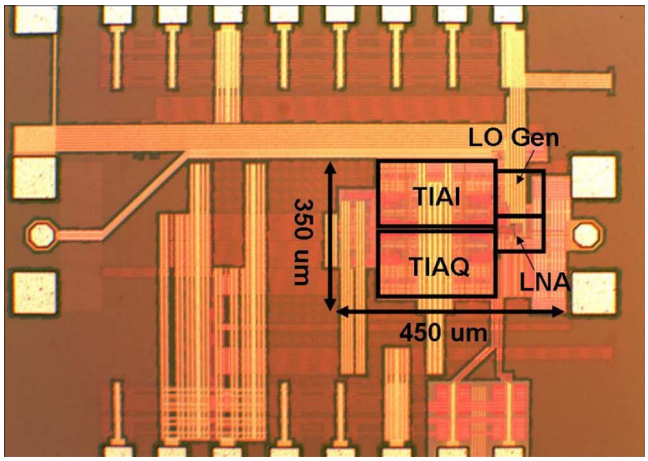


Fig. 22. Front-end die photograph.

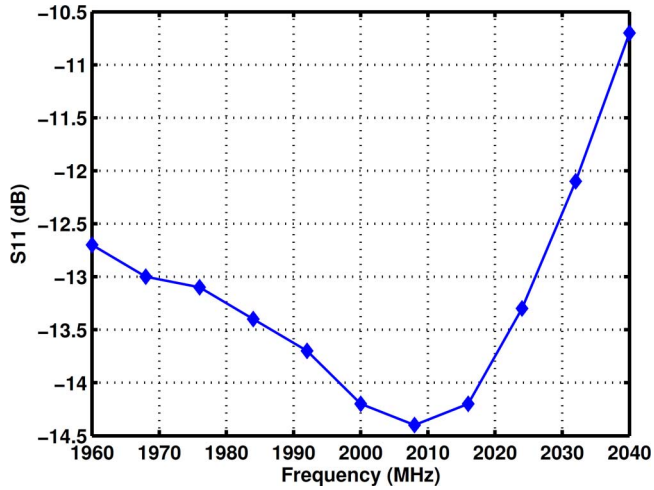


Fig. 24. Measured input matching.

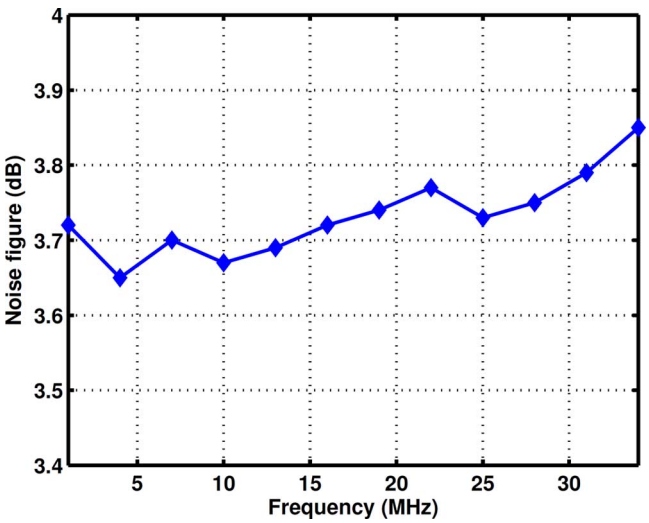


Fig. 23. Measured noise figure.

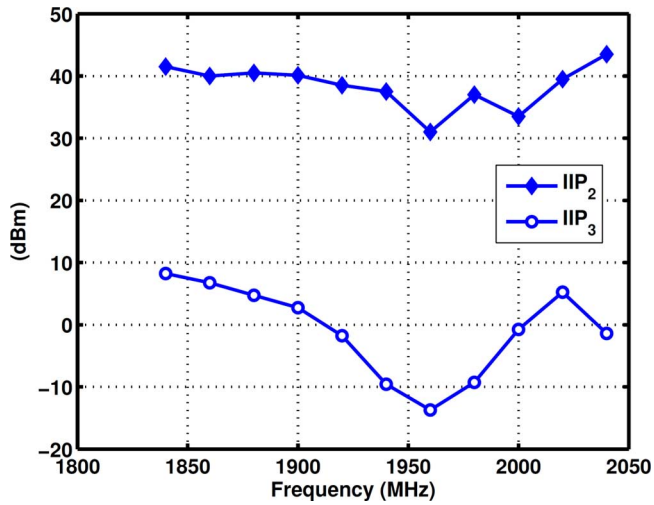


Fig. 25. Measured IIP_2 and IIP_3.

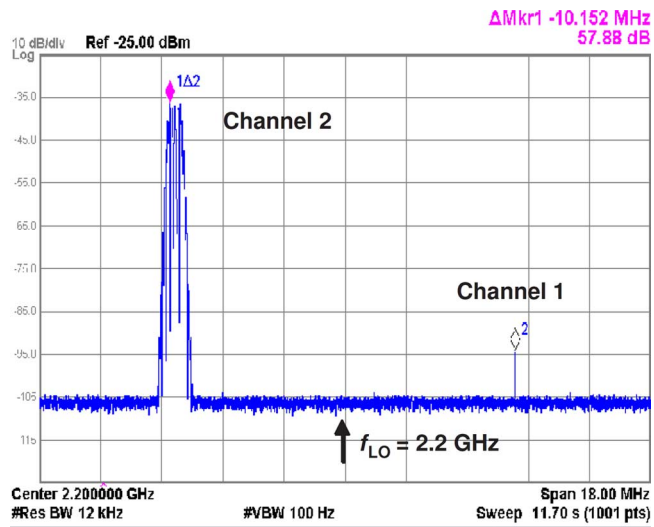


Fig. 26. Measured RF spectrum with two carriers.

the switch resistance noise is included above. For $\overline{I_{n2}^2}$, on the other hand, we write $\overline{I_{n2}^2} \approx 4kT\gamma(G_{m2} + 1/R_{\rm mix})$, because the switch resistance comprises 80% of $R_{\rm mix}$. Finally, we have $\overline{I_{n3}^2} = 4kT\gamma(G_{m3} + 1/R_S)$. It follows that

$$NF = \frac{\pi^2}{8}\left[1+\frac{\gamma}{G_{m1}R_S}+\frac{\gamma+1}{G_{m1}^2R_SR_{\rm mix}}+\frac{\gamma}{G_{m1}R_{\rm mix}}+\frac{R_{\rm SW}}{R_S(G_{m1}R_{\rm mix})^2}\right] + \frac{2R_F}{R_S}\frac{\left[1+G_{m\rm TIA}(4R_{\rm LNA}+4R_{\rm SW})\right]^2}{A_{\rm tot}^2D^2} + 2\frac{G_{m\rm TIA}^2(R_F+4R_{\rm LNA}+4R_{\rm SW})^2}{D^2}\frac{\overline{V_{n,\rm TIA}^2}}{4kTR_SA_{\rm tot}^2}. \quad (12)$$

In order to show the relative contributions of the receiver's devices, Fig. 17 plots the NF for four cases: 1) only the LNA has noise, 2) the LNA and switch resistance have noise at $f_{\rm LO}$, 3) the LNA and switch resistance have noise at all LO harmonics, and 4) the entire receiver. It is worth noting that the inclusion of noise at harmonics raises the NF by 0.9 dB.

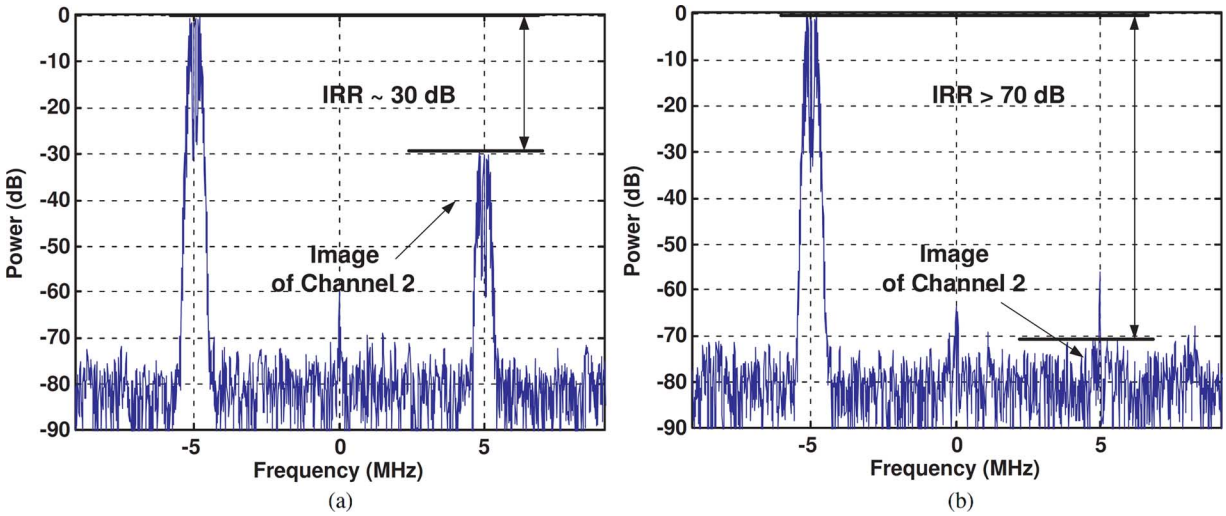


Fig. 27. Measured baseband spectrum with two carriers (a) before image rejection, and (b) after image rejection.

E. Differential Noise Analysis

Since the LNA drives the mixers and the TIAs differentially, the correlation between its output noise currents must be taken into account. Simulations reveal that, if *both* inputs of each TIA are driven by the LNA, then the overall noise figure *falls* by 0.25 dB. This is because I_{n2} in Fig. 14 appears with the same gain and opposite phase at X and Y but is mixed with the 0° and 180° phases of the LO, thus acting as a *common-mode* baseband component. To account for this effect, the term $(\gamma+1)/G_{m1}^2 R_S R_{\rm mix}$ in (12) must be omitted.

The noise of the TIA plays a critical role in the receiver's performance. From (12), the TIA core amplifier's input noise voltage must be limited to about $1.92\ {\rm nV}/\sqrt{\rm Hz}$ if an overall NF of 3 dB is targeted. An important advantage of the complementary TIA implementation shown in Fig. 12 over one with constant current-source loads is that it exhibits less input-referred noise for a given bias current. A tail current of 2 mA allows $V_{n,{\rm in,comp}}$ to be less than $1.63\ {\rm nV}/\sqrt{\rm Hz}$.

F. Noise Figure Comparison

The proposed broadband LNA is capable of achieving a noise figure less than $1+\gamma$. To appreciate this point, we compare the circuit with the resistive-feedback and noise-cancelling topologies shown in Fig. 18.

In Fig. 18(a), the NF is approximately equal to $1+\gamma+4R_S/R_F$, exceeding 3 dB. In Fig. 18(b), one can choose a higher transconductance for M_3 than for M_1 and a proportionally smaller R_2 than R_1, achieving [25] an NF equal to $1+\gamma R_2/R_1+R_S/R_1+R_S R_2/R_1^2+\gamma g_{m2}R_S$. Unfortunately, the unequal values of R_1 and R_2 prohibit cancellation of the noise of M_1 if the circuit is followed by a balanced passive mixer and baseband TIA. If we consider only the LNA noise at $f_{\rm LO}$ for simplicity, the NF rises to $1+\gamma+R_S/R_1+R_S R_2/R_1^2+\gamma g_{m2}R_S$.

The proposed LNA, on the other hand, exhibits a noise figure of $1+\gamma/(G_{m1}R_S)+\gamma/(G_{m1}R_{\rm mix})$. With $R_{\rm mix}\approx R_S=50\ \Omega$ and bias currents of 4 mA, 1.5 mA, and 0.3 mA in ${\rm Inv}_1$, ${\rm Inv}_2$, and ${\rm Inv}_3$, respectively, we have $G_{m1}=80$ mS and $NF=1.76$ dB.

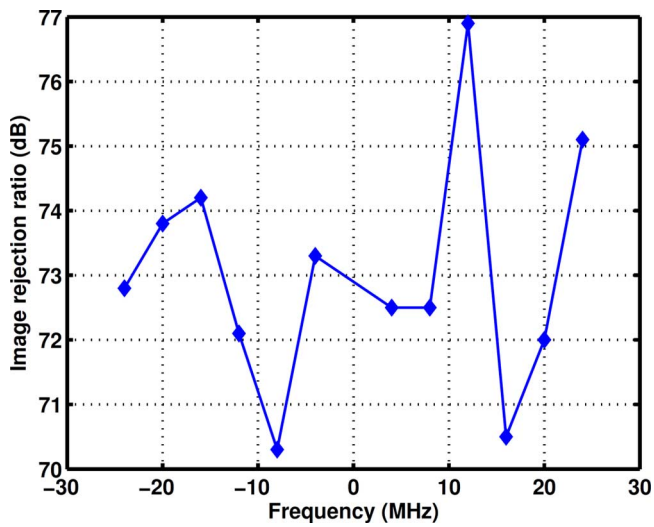


Fig. 28. Measured image-rejection ratio across baseband.

VI. FPGA Implementation

From the scenario depicted in Fig. 2, we note that a narrowband blocker can appear as part of the image in the first down-conversion. With a blocker power substantially higher than the desired signal power, care must be taken to minimize spectral leakage in FFT and IFFT operations of Fig. 8. In order to examine this phenomenon, we look more closely at the functions performed on the signals. As shown in Fig. 19(a), each ADC output is first multiplied by a window function, $W(t)$, then applied to an FFT engine and finally multiplied by a correction factor, $\alpha(\omega)$, in the frequency domain. In order to obtain the time-domain data, the inverse FFT of each corrected FFT frame must be taken and divided by the window function. The resulting real and imaginary parts represent the balanced I and Q data streams, respectively. For example, in our work we employ a 64-point FFT and hence choose a Blackman

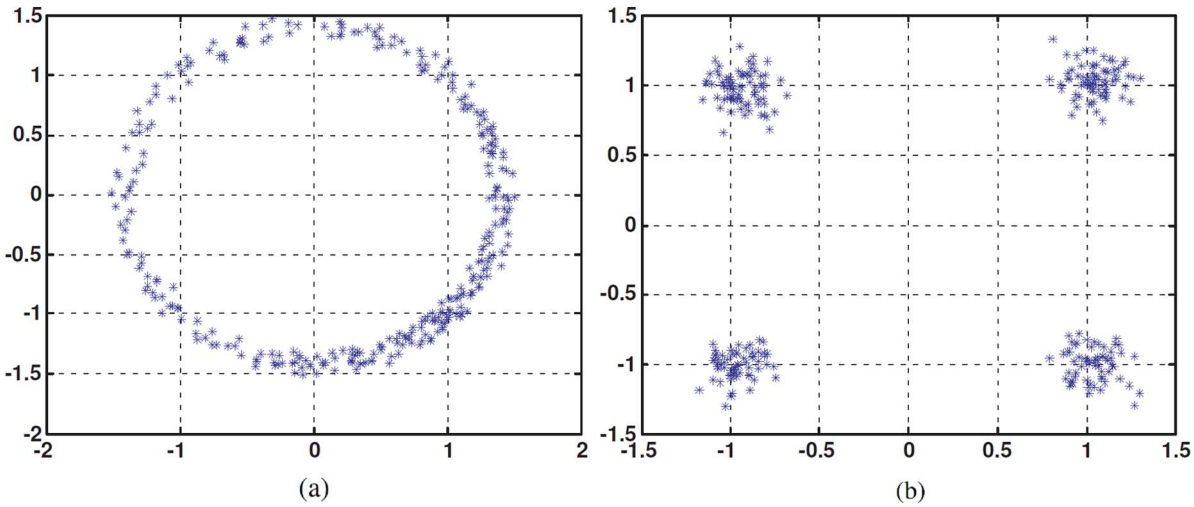


Fig. 29. Measured QPSK constellation (a) before, and (b) after calibration.

window to avoid aliasing. Since the windowed I signal is multiplied by α in the frequency domain, we equivalently write in the time domain $\hat{I}(t) = [I(t)W(t)] * \alpha(t)$, where $\alpha(t)$ denotes the inverse Fourier transform of $\alpha(\omega)$. For proper signal constellation formation, the windowing must eventually be undone, but the convolution with $\alpha(t)$ prohibits simple division because $\hat{I}(t)/W(t) \neq I(t) * \alpha(t)$. In fact, $\hat{I}(t)/W(t)$ suffers from enormous spectral leakage.

To resolve this issue, the I and Q processing and combining are carried out as depicted in Fig. 19(b). Here, in addition to the main I and Q paths, which generate $\alpha I(\omega)$-$jQ(\omega)$, a "shifting" path delays the data by half an FFT block ($T_B/2 = 32$ points) before windowing, FFT, and combining operations, producing $\alpha I_d(\omega)$-$jQ_d(\omega)$. The two composite signals are subsequently applied to IFFTs, the top path signal is delayed by $T_B/2$ to match the delay of the bottom path, and the results are summed before the final inverse window.

The complexity and power consumption of the digital processing described above are of interest. The complexity is estimated conservatively from the FPGA implementation. A 64-point FFT consists of 6 stages of radix-2 butterfly structures [26]. The FFT and IFFT blocks thus require a total gate count of 84,000, which for a gate density of 400 k/mm^2 in 45 nm technology, translates to an area of roughly 0.21 mm^2.

The operations required in the α estimator may appear rather complex. Fortunately, however, they can all be performed by bit-serial arithmetic using only adders and registers [27] because the computation of α can be as slow as temperature- and supply-induced drifts in ϵ and θ. Fig. 20 depicts examples for division, multiplication, and square root functions. (The word length is 20 in the implementation.) The α estimator consumes 3,600 gates and hence 0.01 mm^2. The digital downconverter and NCO are shown in Fig. 21, requiring a total of 2,700 gates and 64 k of memory, i.e., an area of about 0.023 mm^2.

The power consumption of the digital back end arises from (a) the full-rate multipliers necessary for windowing, (b) the full-rate multipliers and accumulators used in the computation of $|I|^2$, $|Q|^2$, and $I \cdot Q$, (c) the downconverters and NCOs, and (d) the FFT and IFFT blocks. At a clock frequency of 70 MHz in 45 nm technology, the first three add up to 1 mW. From the values reported in [28] for FFT blocks in silicon, the fourth component is estimated to be 8 mW.

VII. Experimental Results

This section presents the measured results for the experimental receiver system shown in Fig. 9. The CMOS prototype has been characterized both by itself and along with the receiver chain.

The CMOS prototype has been fabricated in TSMC's 45 nm CMOS technology and characterized with a 1 V supply. Shown in Fig. 22 is the die, whose core area measures 450 μm $\times$ 350 μm. Tested around 2 GHz on a printed-circuit board, the receiver draws 15 mW: 7 mW in the LNA, 5 mW in the TIAs, and 3 mW in the 25%-duty-cycle LO generation circuit.

Fig. 23 plots the measured noise figure for a baseband frequency from 0 to 35 MHz and an LO frequency of 2 GHz. The NF ranges from 3.6 dB to 3.8 dB. Fig. 24 shows the measured S_{11} for $f_{\rm LO} = 2$ GHz, displaying a return loss of better than -11 dB for ± 35 MHz around $f_{\rm LO}$.

The measured $\rm IIP_2$ and $\rm IIP_3$ are plotted in Fig. 25 for two tones that are 3 MHz apart as a function of one-tone frequency. The worst case values are $+30$ dBm and -13 dBm for $\rm IIP_2$ and $\rm IIP_3$, respectively.[8]

The complete receiver of Fig. 9 has been characterized with various types of RF inputs to evaluate the proposed image rejection algorithm. Fig. 26 shows an example with two RF channels, one containing a weak tone and another, a strong modulated signal. Fig. 27(a) depicts the downconverted (complex) spectrum before image rejection calibration, indicating an IRR of about 30 dB. Fig. 27(b) repeats the result after calibration, showing that the image of Channel 2 is buried under

[8]The low value of the duplex IIP2 is attributed to imbalances between V_X and V_Y in Fig. 11(a).

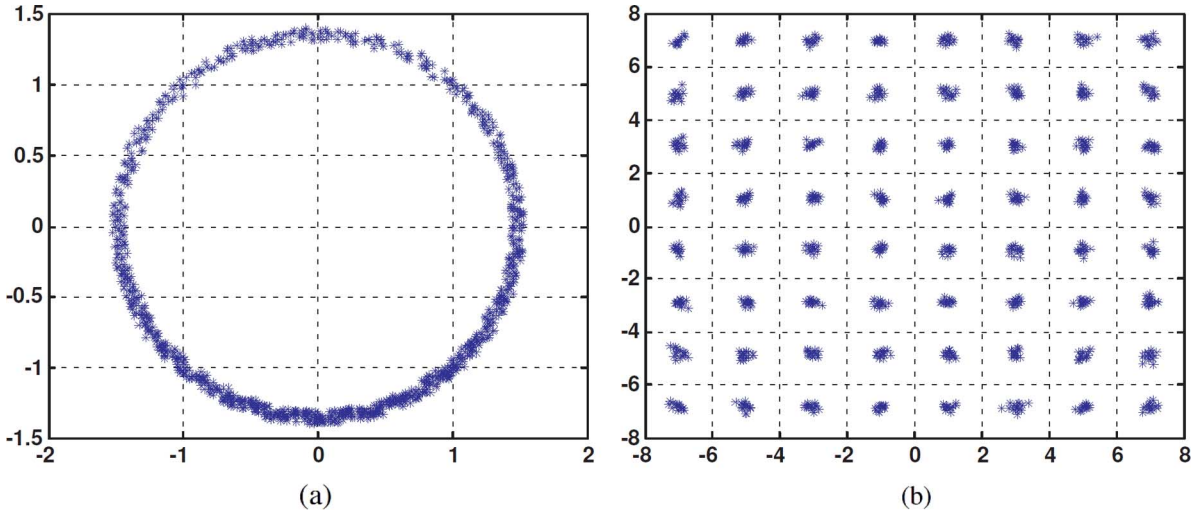


Fig. 30. Measured 64-QAM constellation (a) before, and (b) after calibration.

TABLE I
PERFORMANCE SUMMARY

	This work	Sundstrom [4] ISSCC2013	Din [29] TCASII2013	Xie [30] TMIT 2012
Standard	LTE	LTE	LTE/GSM	LTE/WCDMA
Architecture	Block Down.	Double Conv.	Direct Conv.	Direct Conv.
No. of Intra-Band Carriers	> 2	2	1	1
Tech. / Supply	45 nm / 1 V	65 nm / 1.45V	65 nm / NA	90 nm / NA
Power	15 mW(1)	68 mW(2)	80 mW(3)	NA
IIP2 (duplex)	> 40 dBm	> 58 dBm	57.8 dBm(4)	> 60 dBm
IIP3 (half-duplex)	2.75 dBm	2.4 dBm	-6.9 dBm(4)	2 dBm
IIP2 (in-band)	31 dBm	27 dBm	44 dBm(4)	NA
IIP3 (in-band)	-13.7 dBm	-15 dBm	-18.2 dBm(4)	-8 dBm
DSB NF	3.9 dB	4.5 dB	3.9 dB(4)	3 dB
Voltage Gain	37 dB	45 dB	38 dB(4)	60 dB
IRR	> 70 dB	> 55 dB	NA	NA

(1) LNA + Mixers + TIAs + LO gen.
(2) Estimated from ISSCC Visual Supplement for LNA + RF mixers + IF mixers, excluding the power of all IF and baseband filters.
(3) LNA + Mixers + TIAs + LO gen.
(4) Measured at 1800 MHz.

the noise floor. (In both cases, the output spectrum is computed by the FPGA.) Fig. 28 extends these results for an IF range of -25 MHz to $+25$ MHz.

The performance of the receiver chain has also been assessed by examining signal constellations. A QPSK signal in Channel 1 and 40 dB below another modulated signal in Channel 2 yields the constellations shown in Fig. 29(a) and (b) before and after calibration, respectively. Fig. 30 repeats the experiment with a 64-QAM signal, yielding an error vector magnitude of -30.1 dB after calibration for a Channel 1 input power of -76 dBm.

Table I summarizes the performance of our receiver and compares it with that of the prior art.[9]

[9]The comparison with [4] considers only relevant blocks, but, of course, the work in [4] is an integrated receive chain while our prototype consists of an integrated front-end and off-the-shelf components. The IRR in [4] is greater than 60 dB as averaged over one channel after calibration.

VIII. CONCLUSION

This paper proposes a receiver architecture that can accommodate intra-band channel aggregation for the LTE standard. The use of a new image rejection algorithm in the digital back end greatly simplifies the RF and analog sections of the design and allows calibration of frequency-dependent mismatches. A new broadband LNA topology is also presented that achieves a noise figure less than $1 + \gamma$. With improvements in the performance of ADCs, it is expected that the proposed architecture can also be applied to concurrent reception in WiFi applications.

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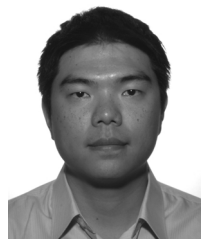

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