A 10-Bit 500-MS/s 55-mW CMOS ADC

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***Abstract*—A pipelined ADC incorporates a digital foreground calibration technique that corrects errors due to capacitor mismatch, gain error, and op amp nonlinearity. Employing a high-speed, low-power op amp topology and an accurate on-chip resistor ladder and designed in 90-nm CMOS technology, the ADC achieves a DNL of 0.4 LSB and an INL of 1 LSB. The prototype digitizes a 233-MHz input with 53-dB SNDR while consuming 55 mW from a 1.2-V supply.**

***Index Terms*—Calibration by inverse function, foreground digital calibration, low gain op amp, nonlinearity correction, pipelined analog-to-digital converter, resistor-ladder DAC.**

I. Introduction

RECENT work on analog-to-digital converters (ADCs) has made significant progress toward sampling rates of hundreds of megahertz and resolutions in the range of 10 to 11 bits [1], [2]. Among the reported designs, those employing a single channel face a limited speed [3], [4], while those incorporating interleaving suffer from a high power dissipation [2] or a low signal-to-(noise+distortion) ratio (SNDR) [5]. The need therefore exists for ADC architectures that combine high resolution, high speed, and low power dissipation in a single channel. Of course, interleaving can further increase the speed of such designs.

This paper proposes a pipelined ADC calibration technique that allows the use of high-speed, low-power, and yet inaccurate op amps. Designed in 90-nm CMOS technology, a 10-bit prototype digitizes a 233-MHz input with an SNDR of 53 dB, for a power consumption of 55 mW [6]. The ADC derives its performance from a high-speed op amp and a highly-linear resistor ladder topology.

Section II of the paper describes the ADC architecture and Section III the calibration algorithm. Section IV presents the implementation of the prototype ADC and its building blocks. Section V summarizes the experimental results.

II. ADC Architecture

Pipelined ADCs, even with 1.5-bit stages, must deal with four critical issues: $\mathrm{kT/C}$ noise, capacitor mismatch, finite op amp gain, and op amp nonlinearity. An efficient architecture selects capacitor values according to $\mathrm{kT/C}$ noise requirements but not necessarily capacitor matching requirements, handling the latter by calibration. The two op-amp-related issues begin to manifest themselves as it becomes increasingly more difficult to design high-gain, high-swing op amps using deep-submicron devices. Table I summarizes recent work on the correction of these errors and the limitations of each technique [7]–[16]. It is observed that only [16], [12], and [15] address the amplifier nonlinearity issue, but the first sacrifices the input dynamic range, the second does not correct for capacitor mismatch, and the third operates with an op amp gain of several hundred (for 12 bits).

An ADC suffering from various errors can be viewed as a system having a general input-output characteristic given by $D_{\mathrm{raw}} = g(x)$. As shown in Fig. 1(a), an inverse operator in the digital domain can correct for all errors, producing a faithful replica of the input, D_{corr}. However, it is difficult to realize this inverse function with reasonable complexity. For example, if the ADC characteristic is nonmonotonic, then $g^{-1}(x)$ must entail hysteresis.

Now consider one stage of a pipelined ADC. We surmise that if, as depicted in Fig. 1(b), the residue is digitized by an ideal digitizer (i.e., an "ideal back end"), then it can be corrected more easily because its errors are not as complex as those in a general ADC. Nonetheless, since the digital output of this stage, D_j, may bear gain error with respect to the analog residue value (as explained in Section III), an additional gain correction step is necessary [Fig. 1(c)]. We also recognize that the ideal back end is simply formed if the calibration begins with the last stage of the pipeline and progresses backward. That is, calibration of stage j can assume that stages $j+1$ and higher are ideal.

The arrangement shown in Fig. 1(c) is the basis of the proposed ADC architecture and calibration technique. The architecture is shown in Fig. 2. It consists of 13 1.5-bit stages and one 1-bit stage. The first two stages are calibrated for residue gain error, digital-to-analog-converter (DAC) gain error, and op amp nonlinearity; the next four stages for residue gain and DAC gain error; and the next seven stages for residue gain error.

The digital calibration back end consists of programmable gain coefficients, w_j [ideally equal to $(1/2)^j$], and two programmable third-order polynomials of the form $g_j^{-1}(x) = \alpha_1 x + \alpha_3 x^3$, which approximates the inverse function of the input/output characteristic of each multiplying digital-to-analog converter (MDAC). With the aid of a highly-accurate on-chip reference DAC, the system applies a number of analog levels at the input (at start-up) and uses a least-mean-square (LMS) engine to adjust w_j and α_j so as to drive a certain error function to zero.

The sub-ADC and the MDAC in the first stage sample V_{in} simultaneously, thereby obviating the need for an explicit front-end sample-and-hold amplifier (SHA) [17]–[19]. Such

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TABLE I
SUMMARY OF PRIOR ART

Reference	Gain Error Correction	Capacitor Mismatch Correction	Nonlinearity Correction	Notes
[7]		√		Requires an extra averaging amplifier.
[8]		√		Trim capacitors and switches.
[9]	√	√		Requires a calibrated backend.
[11]	√			Reduced input dynamic range, slow-but-accurate ADC and 7-bit reference DAC.
[12]	√		√	Does not correct capacitor mismatch, requires additional bit for stage under calibration, corrects nonlinearity of only one stage, and assumes a calibrated back end.
[13]	√	√		Requires a slow-but-accurate ADC.
[14]	√			Addition of random input reduces dynamic range.
[15]	√	√	√	Requires one clock for ADC (f_C), and one clock for SHA (f_S). Also, for background calibration $f_C > f_S$.
[16]	√	√	√	Addition of random input reduces dynamic range.

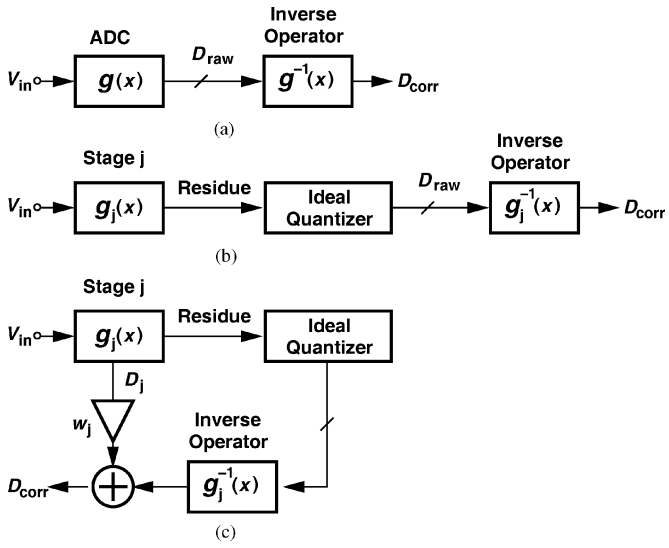

Fig. 1. Calibration concept.

a SHA would consume substantial power while contributing significant noise and nonlinearity. Nevertheless, the sampling networks at the input of the sub-ADC and the MDAC must sustain minimal mismatches such that the resulting discrepancy can be corrected by the 0.5-bit redundancy. Also, the sub-ADC conversion time now limits the time allocated to the settling of the MDAC. These issues are discussed in Section IV.

III. CALIBRATION TECHNIQUE

Consider the 1.5-bit pipelined stage shown in Fig. 3, where the sub-ADC consisting of two comparators determines whether $-V_{\rm REF}/4 < V_{\rm in} < +V_{\rm REF}/4$ or not, and the MDAC consisting of C_1, C_2, and the op amp generates the residue. In the ideal case, the residue is expressed as $V_{\rm out} = 2V_{\rm in} - D_{\rm out}V_{\rm REF}$, where $D_{\rm out}$ denotes the digital output of the sub-ADC. That is, the sampled analog input can be estimated as

$$V_{\rm in} = \frac{1}{2}V_{\rm out} + \frac{1}{2}D_{\rm out}V_{\rm REF}. \quad (1)$$

Capacitor mismatch and finite op amp gain give rise to a gain error while op amp nonlinearity introduces a nonlinear component. If $C_1 = C(1+\epsilon)$, $C_2 = C(1-\epsilon)$, and the open-loop input/output characteristic of the op amp is represented by $y = f(x)$, then V_N in Fig. 3 is equal to $-f^{-1}(V_{\rm out})$ and hence

$$V_{\rm in} = \frac{1}{2}(1+\epsilon)V_{\rm out} + f^{-1}(V_{\rm out}) + \frac{1}{2}(1-\epsilon)D_{\rm out}V_{\rm REF}. \quad (2)$$

Incorporating the effect of the finite input capacitance of the op amp C_p, we have

$$V_{\rm in} = \frac{1}{2}(1+\epsilon)V_{\rm out} + \left(1+\frac{C_p}{2C}\right)f^{-1}(V_{\rm out}) + \frac{1}{2}(1-\epsilon)D_{\rm out}V_{\rm REF}. \quad (3)$$

Note that capacitor mismatch, ϵ, appears in the first term, leading to a residue gain error, and in the last term, translating to a DAC gain error. In accordance with our notation in Fig. 1(c), we observe that the first two terms in (3) constitute $g_j^{-1}(x)$ and the coefficient of $D_{\rm out}$ is the same as w_j. In the architecture of Fig. 2, $g_j^{-1}(x)$ is approximated by a third-order polynomial for the first two stages.

The op amp used in this work (Section IV) achieves a high speed and large output swings but suffers from a low gain (≈ 25). We therefore expect a relatively high closed-loop nonlinearity. On the other hand, the architecture of Fig. 2 assumes that

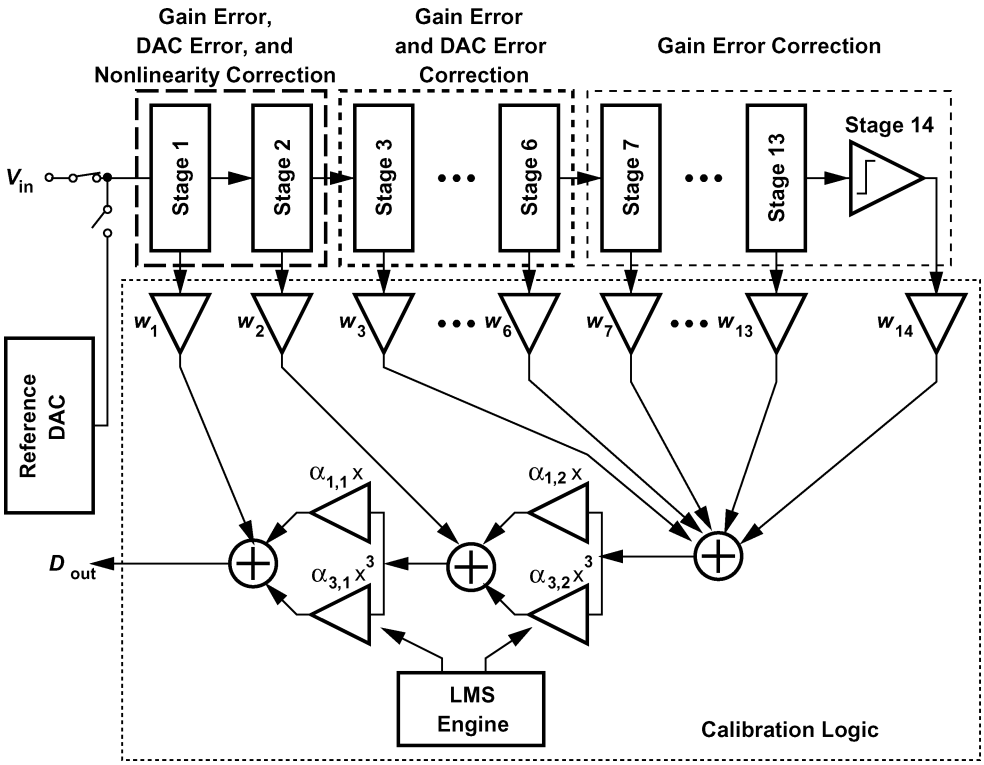

Fig. 2. Pipelined ADC architecture.

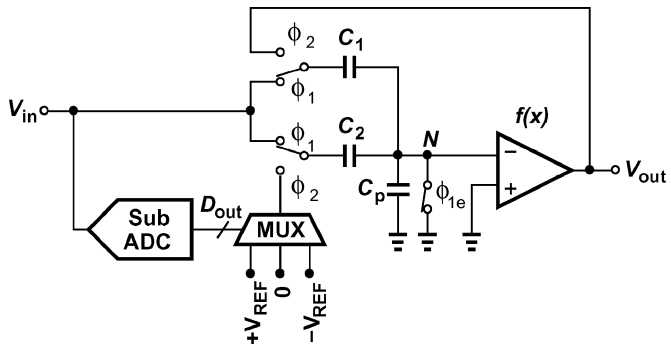

Fig. 3. Switched capacitor implementation of 1.5-bit stage.

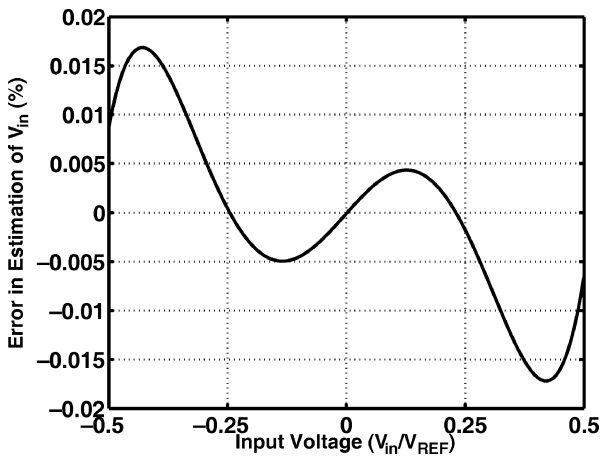

Fig. 4. Error in $V_{\rm in}$ with third-order polynomial fitting.

the inverse transfer characteristic of each stage can be approximated by no more than third-order terms. To verify the validity of this assumption, we first rewrite (3) as

$$V_{\rm in,approx} = \alpha_1 V_{\rm out} + \alpha_3 V_{\rm out}^3 + \frac{1}{2}(1-\epsilon) D_{\rm out} V_{\rm REF}. \quad (4)$$

Next, we perform a transistor-level transient simulation on Fig. 3 (e.g., with $\epsilon = 0$ and forcing the multiplexer output to 0) whereby $V_{\rm in}$ is slowly varied from $-0.5V_{\rm REF}$ to $+0.5V_{\rm REF}$ (in differential implementation) and $V_{\rm out}$ is measured. Last, we estimate the values of α_1 and α_3 so as to obtain a good fit (e.g., with minimum mean-square error between $V_{\rm in}$ and $V_{\rm in,approx}$). If the residual error between the actual $V_{\rm in}$ and the value predicted by (4) ($V_{\rm in,approx}$) remains well below 1 LSB, then the third-order approximation is justified. Fig. 4 plots this error across the input range (with $\alpha_1 = 0.554$, and $\alpha_3 = 0.004\ \mathrm{V}^{-2}$), revealing a maximum of about 0.15 LSB and implying that the approximation is reasonable.

A. Calibration Procedure

The calibration begins with the last stage and proceeds toward the front end. As a result, calibration of stage j can assume that the subsequent stages constitute an "ideal" back end. Fig. 5 illustrates the calibration arrangement. The reference DAC applies dc inputs to stage j such that the sub-ADC of this stage produces $D_{{\rm out},j}$ and the back end generates $D_{\rm BK}$. Note that $D_{\rm BK}$ accurately represents the residue output of stage j. Next, $D_{\rm BK}$ is subjected to $f^{-1}(\cdot)$ so as to "undo" the nonlinearity created by stage j, and is combined with $w_j D_{{\rm out},j}$ to arrive at the overall

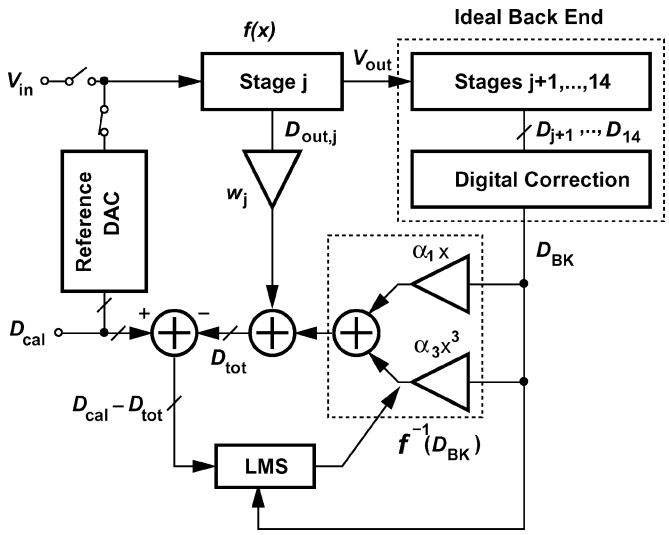

Fig. 5. Digital calibration.

output, $D_{\rm tot}$. In the ideal case, $D_{\rm tot}$ must be equal to the digital input of the reference DAC, $D_{\rm cal}$. Thus, $D_{\rm cal} - D_{\rm tot}$ serves as the error function that must be minimized by the LMS algorithm.

The calibration procedure consists of two steps: estimation of α_1 and α_3 without interaction with w_j, and estimation of w_j with α_1 and α_3 set properly.[1] These steps are described below.

B. Estimation of α_1 and α_3

In the first step of calibration, dc inputs equal to $\pm V_{\rm REF}/2$, $\pm V_{\rm REF}/4$, and 0 are produced by the reference DAC in Fig. 5 and applied to stage j. Stage j is configured as a multiply-by-two circuit such that $D_{{\rm out},j} = 0$. Thus, in Fig. 5

$$D_{\rm tot} = \alpha_1 D_{\rm BK} + \alpha_3 D_{\rm BK}^3. \tag{5}$$

The LMS algorithm adjusts α_1 and α_3 so as to drive the mean square error of $D_{\rm tot} - D_{\rm cal}$ to zero. Specifically, α_1 and α_3 are updated according to the following equations:

$$\alpha_1(k+1) = \alpha_1(k) + \mu_1(D_{\rm cal} - D_{\rm tot})D_{\rm BK} \tag{6}$$

$$\alpha_3(k+1) = \alpha_3(k) + \mu_3(D_{\rm cal} - D_{\rm tot})D_{\rm BK}^3. \tag{7}$$

Fig. 6(a)–(c) depict the convergence of α_1, α_3, and $D_{\rm cal} - D_{\rm tot}$ in a system-level simulation of the first stage.[2]

C. Estimation of w_j

The coefficients w_j correct for the effect of capacitor mismatch on D/A conversion [the last term in (4)]. In this case, the MDAC operates in the regular mode (sampling, D/A conversion, multiplication by 2). The reference applies a voltage equal to $+V_{\rm REF}/2$ such that the digital equivalent of (4) plus $w_j D_{{\rm out},j}$ can be written as

$$D_{\rm tot} = \alpha_1 D_{\rm BK} + \alpha_3 D_{\rm BK}^3 + w_j D_{{\rm out},j}. \tag{8}$$

[1]Note that the gain error of the op amp is captured within α_1.

[2]In [6], coefficient α_1 is estimated first, and then α_3. It is later determined that the simultaneous calibration of α_1 and α_3 is a better technique and is explained here.

The value of w_j is therefore adjusted to minimize the difference between $D_{\rm tot}$ and $D_{\rm cal}$. The proposed calibration operates in the foreground, potentially suffering from drifts with temperature. This issue is addressed in Section IV-B.

D. Back-End Stages

The low open-loop gain of the op amp yields a closed-loop residue gain of only 1.7. Owing to this large departure from the ideal value of 2.00, a cascade of n pipelined stages provides an overall gain substantially less than 2^n, failing to generate digital codes for the lower and upper ends of the range. For this reason, the architecture of Fig. 2 employs eight back-end stages to achieve five bits of resolution. (The digital outputs are eventually truncated to five bits after calibration logic.)

As indicated in Fig. 2, the last eight stages are calibrated for only residue gain error. Since capacitor mismatch is negligible here, only the finite gain of the op amp produces gain error. Moreover, since the mismatches among the gains of the op amps used in these stages are negligible at this resolution level, we assume that the stages exhibit *equal* gain errors and hence can be calibrated by a single variable.

To calibrate the back end, its first stage (stage number 7 in Fig. 2) is configured as a multiply-by-two circuit while sensing an input equal to $\pm V_{\rm REF}/4$ provided by the calibration DAC. Coefficients w_j are then adjusted so as to minimize the difference between the digital output of this back end and $D_{\rm cal}$.

A flow chart of the steps described above is shown in Fig. 7.

IV. ADC Design

The architecture of Fig. 2 has been realized in 90-nm CMOS technology. This section presents the implementation details.

A. Input Sampling Network

As mentioned in Section II, the first flash stage and MDAC sample the analog input simultaneously, facing potential timing mismatches and hence inconsistencies between the digital and residue outputs. Half a bit of redundancy alleviates this issue considerably, but reasonable path matching must be ensured to leave margin for other errors (e.g., comparator offset).

Fig. 8 shows the front-end input sampling network in the acquisition mode. To keep the two paths nominally identical, the input to the op amp or the comparator is disconnected in this mode. Switches S_1, S_2 and S_3 turn off before others, thus performing bottom-plate sampling.

Another critical issue in the front end is that the flash ADC conversion time must be minimized to allow sufficient settling time for the MDAC. The tight timing budget requires careful partitioning of the clock period, $T_{\rm CK}$, among three operations: sampling, flash conversion, and residue generation (in the first stage). Since bootstrapped switches can provide a relatively short acquisition time while achieving high linearity, this design allocates 25% of $T_{\rm CK}$ to sampling, and the other 75% to flash conversion and residue generation (in the first stage). These waveforms are derived from an input clock frequency of 1 GHz, which is divided by 2 so as to generate quadrature phases. Two of the phases are then ANDed, producing the necessary 25% duty cycle.

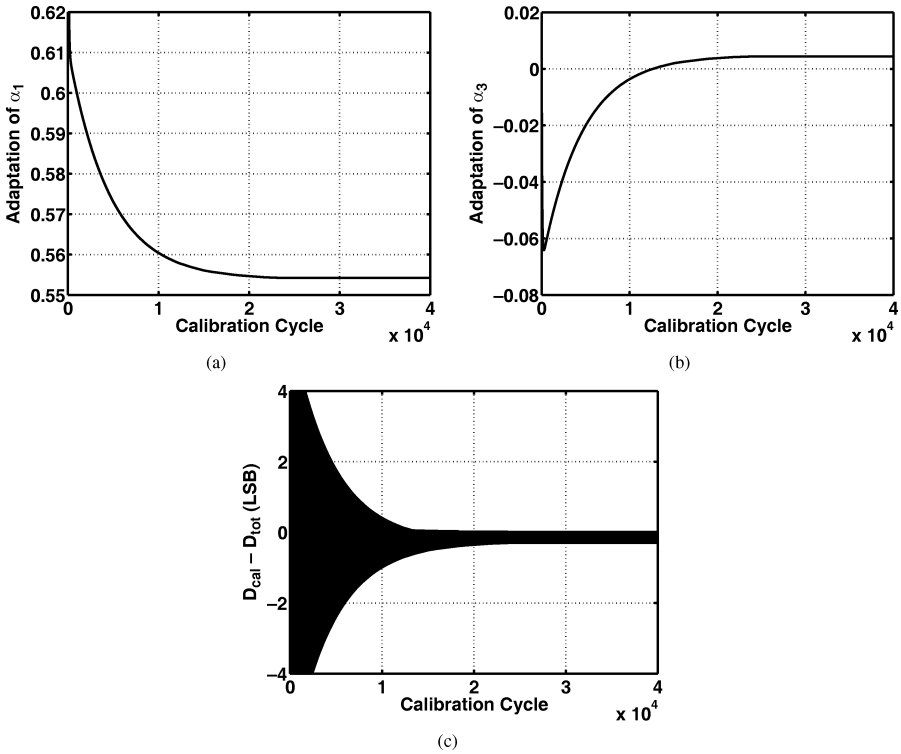

Fig. 6. Simulated convergence of (a) α_1, (b) α_3, and (c) $D_{\rm cal} - D_{\rm tot}$.

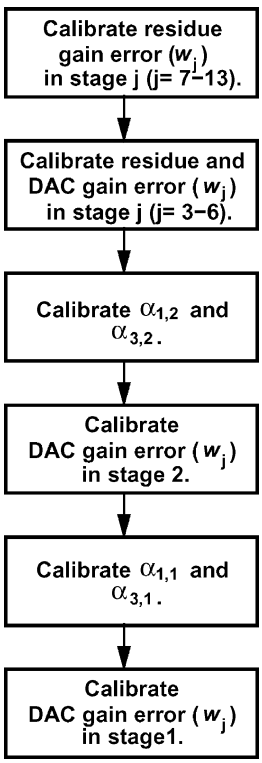

Fig. 7. Calibration flow chart.

The following stages in the pipeline operate with a 50% duty cycle. The switching of the second-stage sampling capacitors to the output of the first MDAC generates a glitch, which subsides over the remaining half cycle. This glitch is, however, relatively small because of the smaller capacitors used in the second stage.

The absence of the op amp from the sampling network in Fig. 8 means that its offset is not removed. While benign in general ADCs, such a front end offset does create discrepancy in the calibration mode as the correcting third-order polynomial assumes that there is no offset present in the system. To cancel this offset, a zero dc input is applied and the resulting digital output $D_{\rm os}$ is stored in the memory. This digital output $D_{\rm os}$ is then subtracted from the overall output when the calibration coefficients are computed.

B. Op Amp

The speed and power consumption of the ADC are determined primarily by those of the op amp. This work views the op amp as an amplifier having large output swings and maximum speed with little attention to its open-loop gain. The large output swings relax kT/C noise requirements, directly leading to a lower power consumption.

The need for a high-swing op amp naturally points to a two-stage topology, and the desire for maximum speed, to the smallest number of poles, namely, two. From these observations emerges the op amp shown in Fig. 9. To maintain a true two-pole (uncompensated) behavior, the circuit avoids cascode devices. Moreover, to achieve fast common-mode (CM) settling, each stage employs a simple resistive feedback network. Note that the bias current of the output stage is defined as a multiple of $I_{\rm SS}$ through the current mirror action of the pMOS devices. Also, the output CM level is raised to $0.5I_1R_{C1,2} + V_{GS7,8}$ so that it reaches approximately $V_{\rm DD}/2$.

In order to maximize the uncompensated pole frequencies, the circuit of Fig. 9 incorporates minimum-length transistors in the signal path, thus exhibiting an open-loop gain of only

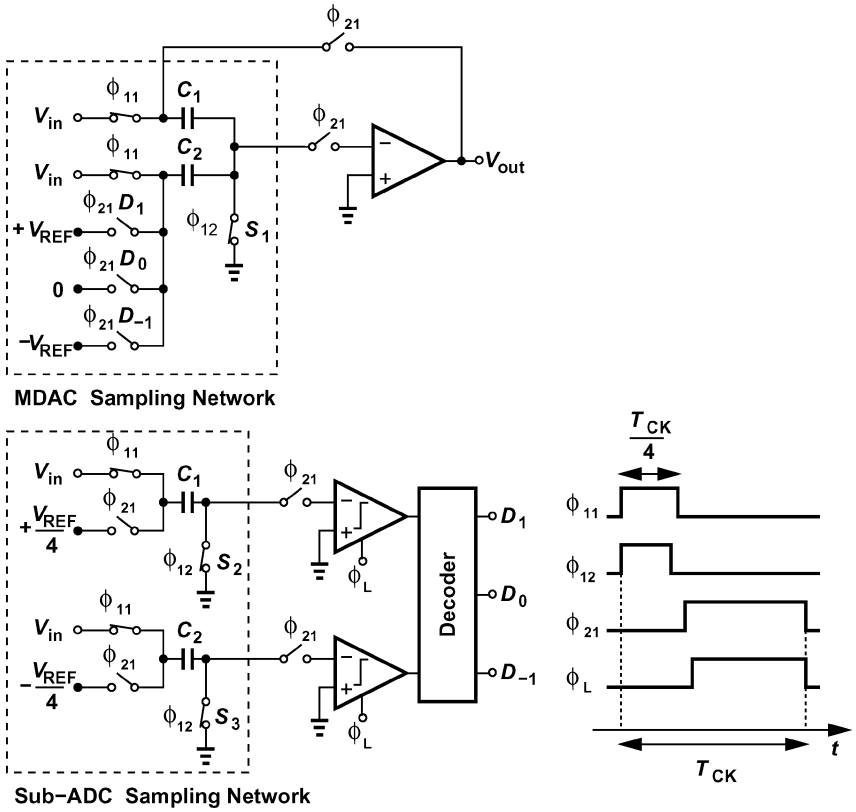

Fig. 8. Input sampling networks and timing diagram.

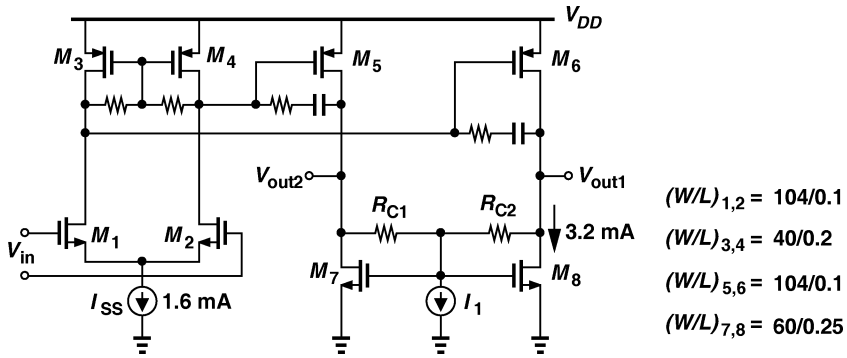

Fig. 9. Two-stage op amp schematic.

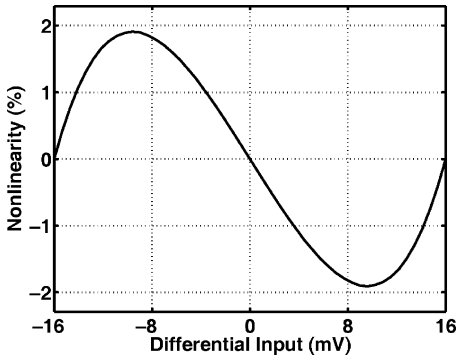

Fig. 10. Simulated nonlinearity of the op amp.

25. As explained in Section II, the low gain yields substantial closed-loop nonlinearity, necessitating calibration. Fig. 10 plots the simulated open-loop nonlinearity of the op amp for a peak-to-peak differential output swing of 1.2 V.

In order to study the behavior of the op amp in the MDAC environment, we construct the equivalent circuit shown in Fig. 11 (without the compensation network). Here, A_j and $R_{\text{out},j}$ denote the voltage gain and output resistance of stage j, respectively, and C_{p1} models the total capacitance at the output of the first stage. Capacitors C_1, C_2, and C_L represent those required for MDAC operation.

The loop transmission, $T(s)$, can be obtained by setting V_{in} to zero, breaking the loop at V_X and computing the transfer function around the loop. It follows that

$$T(s) = \frac{\beta A_1 A_2}{\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} \tag{9}$$

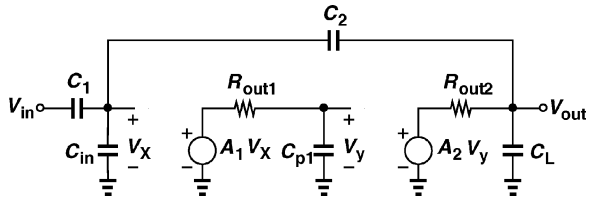

Fig. 11. Small-signal model of MDAC before compensation.

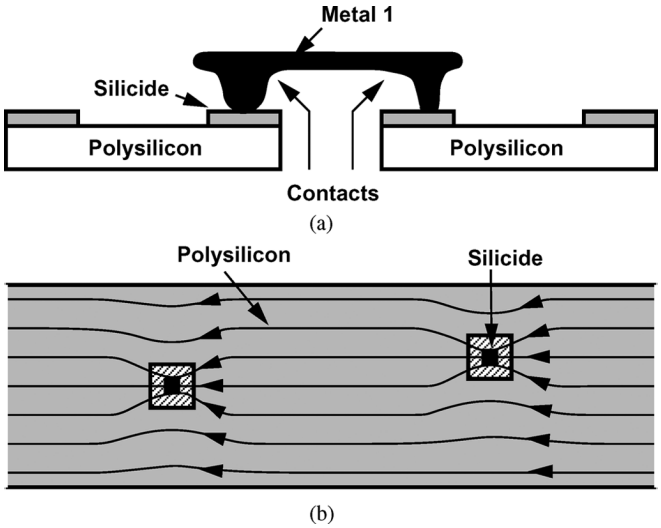

Fig. 12. (a) Series poly resistors with current-carrying contacts. (b) Continuous polysilicon ladder (top view).

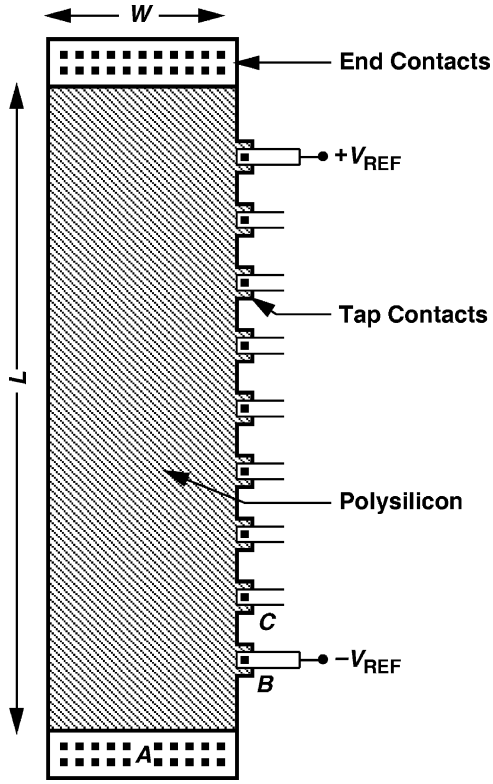

Fig. 13. Reference DAC.

where $\beta = C_2/(C_1 + C_2 + C_{\rm in})$ and

$$\omega_{p1} = \frac{1}{R_{\rm out1} C_{p1}} \tag{10}$$

$$\omega_{p2} = \frac{1}{R_{\rm out2}\left[C_L + \dfrac{(C_1 + C_{\rm in})C_2}{C_1 + C_2 + C_{\rm in}}\right]}. \tag{11}$$

The magnitude of $T(s)$ falls to unity at a frequency given by

$$\omega_u^2 = \frac{-(\omega_{p1}^2+\omega_{p2}^2)+\sqrt{(\omega_{p1}^2+\omega_{p1}^2)^2-4\omega_{p1}^2\omega_{p2}^2[1-(\beta A_1 A_2)^2]}}{2}. \tag{12}$$

In this design, $\omega_{p1} \approx 2\pi(1.28\ \text{GHz})$, $\omega_{p2} \approx 2\pi(3.16\ \text{GHz}) \approx 2.47\omega_{p1}$, $\beta \approx 0.303$, and $A_1 A_2 = 30$. Thus, $\omega_u \approx 4.36\omega_{p1}$. The phase shift at ω_u is thus given by

$$\angle T(s = j\omega_u) = -\left(\tan^{-1}\frac{\omega_u}{\omega_{p1}} + \tan^{-1}\frac{\omega_u}{\omega_{p2}}\right) \tag{13}$$

$$= -138^\circ. \tag{14}$$

The key observation here is that the phase margin is about 42° before compensation, thereby requiring only a moderate reduction of ω_{p1} so as to reach an adequate amount, e.g., 60°. This stands in contrast to the behavior of typical two-stage op amps, especially if loaded with a significant capacitance, which exhibit a negative or near-zero uncompensated phase margin. Compensated for a phase margin of 60°, the op amp of Fig. 9 provides a unity-gain bandwidth of 10 GHz.

The device dimensions and bias currents shown in Fig. 9 correspond to those in the first MDAC. The MDAC is scaled down by a factor of two in the second stage and four in the third stage. Stages 4 to 13 remain unscaled due to the small size of the capacitors (25 fF) and negligible power consumption.

The foreground calibration technique proposed herein assumes negligible drift of the MDAC characteristics with temperature. Since the op amp operates in a closed-loop configuration, variation of its characteristics is suppressed by the loop gain. Nonetheless, for a constant bias current, the op amp small-signal gain varies markedly with temperature, degrading the performance.[3] On the other hand, it was found from simulations that if the overdrive voltage of the input transistors is kept constant, so is the small signal gain. Using the bias circuit in [21] for this purpose, simulations suggest an SNDR degradation of about 2 dB if the circuit is calibrated at 27 °C and the temperature rises to 75°.

C. Reference DAC

The calibration algorithm proposed here relies on a highly-accurate on-chip DAC. The reference fractions used in the calibration process (Section III) must be generated with a precision higher than approximately 11 bits. The choice of the DAC is governed by the following considerations [20]: 1) capacitor DACs require large units to achieve high accuracy, thus

[3]The nonlinear terms vary negligibly.

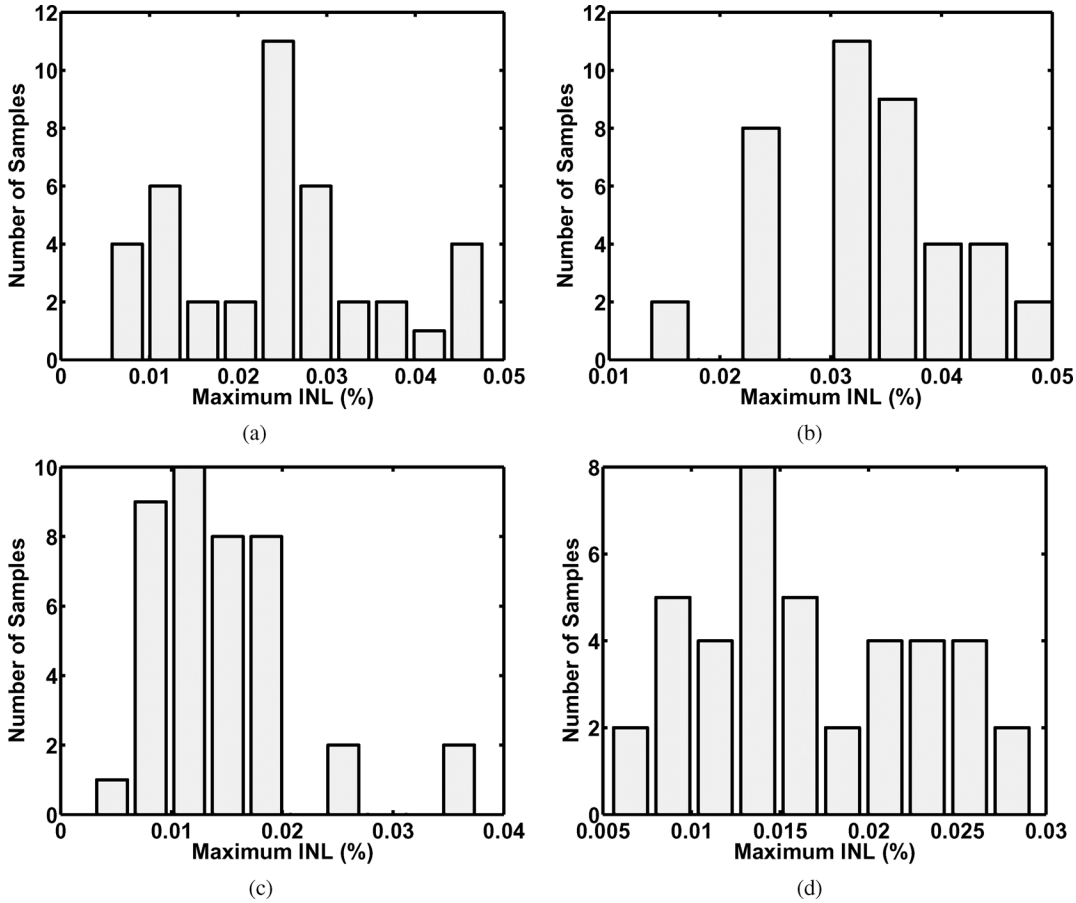

Fig. 14. INL distributions for ladders of different dimensions, (a) L = 32 μm, W = 10 μm, (b) L = 32 μm, W = 20 μm, (c) L = 64 μm, W = 10 μm, and (d) L = 64 μm, W = 20 μm.

slowing down the MDAC if they are tied to the virtual ground; 2) current-steering DACs suffer from both gain error and a limited output swing; 3) resistor ladders can provide a zero-offset rail-to-rail output but with a long settling time. Since this work employs foreground calibration, the third choice proves most suitable.

In order to design a resistor ladder having a reproducibly accurate set of outputs, a number of error sources must be considered. First, the very thin layer of silicide deposited on polysilicon can experience large thickness variations from one end of the ladder to the other. Thus, non-silicided poly is preferable. Second, the relatively large contact resistance and the poor definition of its value (depending on how much and how deeply the metal fills each contact window) [Fig. 12(a)] suggest that current-carrying contacts can potentially introduce large errors in voltage division. It is therefore desirable to avoid such contacts along the ladder. Third, even contacts that carry no current and simply sense a voltage must create minimal disturbance in the flow of the current. This concern arises because the silicided area under each contact disturbs the current flow, and misalignment in its position leads to random disturbance [Fig. 12(b)].

Based on these observations, we propose the ladder structure shown in Fig. 13. The voltage-sensing contacts are placed on the edge, introducing negligible disturbance in the current flow. Also, since the poly segment between the end A and the tap B is not identical to that between taps B and C (due to the large number of contacts and their underlying silicided area at A), the full-scale references used for the ADC, $\pm V_{\mathrm{REF}}$, are taken from the first and last taps rather than from the ends.

The ladder structure of Fig. 13 has been fabricated separately with different dimensions and its integral nonlinearity (INL) profile has been measured for differential outputs on 40 samples. Fig. 14 plots the distributions of the maximum measured INL for four sets of dimensions: $W = 10$ μm and 20 μm, and $L = 32$ μm and 64 μm.

It is observed that the peak INL falls to a value of 0.027% for $L = 64$ μm and $W = 20$ μm. These dimensions are chosen for the reference ladder used in this work. The high linearity of the resistor ladder makes it also attractive for use as an interstage multi-bit DAC in the main signal path (in pipelined or subranging architectures). However, the high resistance of the ladder gives rise to long settling times.[4]

V. Experimental Results

The prototype ADC has been fabricated in 90-nm digital CMOS technology. Shown in Fig. 15 is the die, whose active area measures 700 μm$\times$ 700 μm. The resistor-ladder DAC is

[4]The DAC has 3 bits of resolution and a total resistance of 1.3 kΩ. It occupies an area of 64 μm$\times$ 20 μm, consumes 0.3 mW, and can run at a speed of 100 MHz.

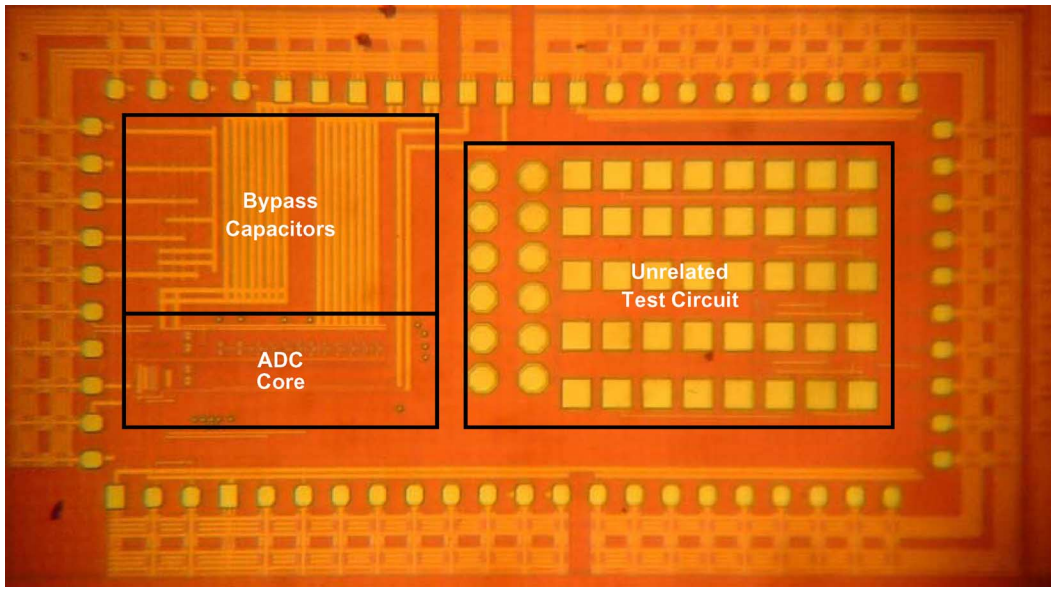

Fig. 15. Die photograph.

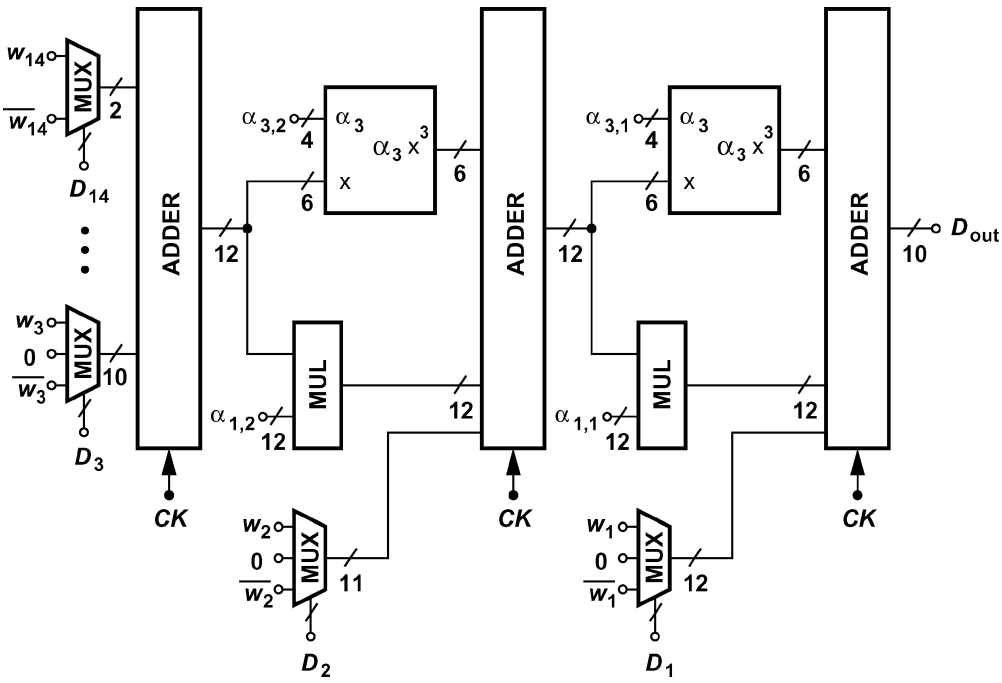

Fig. 16. Block diagram of synthesized calibration logic.

included on the chip. The digital outputs are downsampled by a factor of 16 to simplify testing. The die has been mounted directly onto a printed-circuit board. Operating with a 1.2-V supply, the ADC draws 55 mW, of which 40 mW is consumed by the op amps and 15 mW by the comparators and the clock buffer.

The calibration is run off-chip, but a detailed gate-level synthesis of the calibration logic is performed to estimate the associated power dissipation. Fig. 16 shows a block diagram of the synthesized system. The complexity is about 20,000 gates. The nonlinearity correction requires the function $y = \alpha_3 x^3$, which, if implemented directly, incurs a considerable area and power penalty. However, the logic can be greatly simplified by observing that the correction term ($\alpha_3 x^3$) is only a few LSBs wide. The adder output (shown as input x) is also truncated to 6 bits and the coefficient α_3 is represented by only 4 bits. The output of this block is truncated to 6 bits. With a clock frequency of 500 MHz in 90-nm CMOS technology, the total power dissipation of the logic is about 8 mW with $V_{\rm DD} = 1.2$ V and 5.6 mW with $V_{\rm DD} = 1$ V.

Fig. 17 shows the measured DNL and INL at a sampling rate of 500 MHz before and after gain error, DAC error, and nonlinearity calibration. The uncalibrated prototype suffers from a large number of missing codes and an INL of 40 LSB. After full calibration, the DNL and INL fall below 0.4 LSB and 1 LSB, respectively.

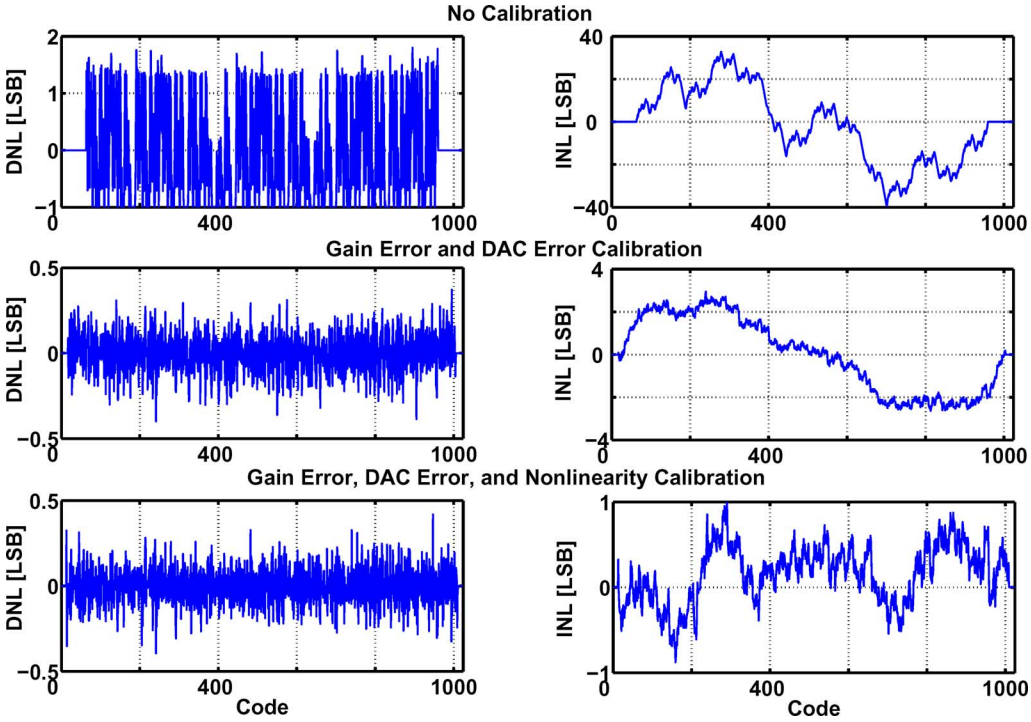

Fig. 17. Measured differential and integral nonlinearity at a sampling rate of 500 MHz.

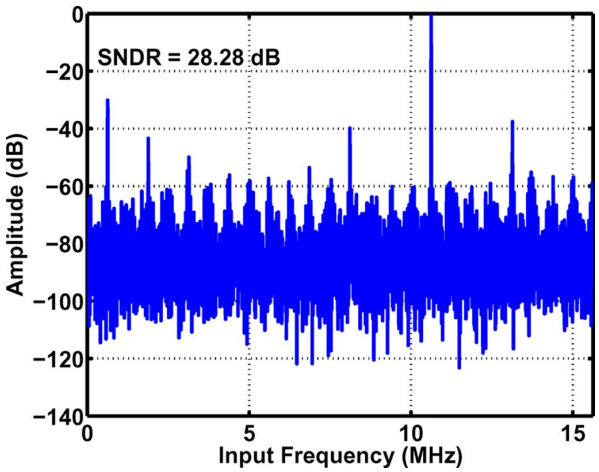

Fig. 18. Output spectrum for 10.7 MHz input frequency at a sampling rate of 500 MHz before calibration.

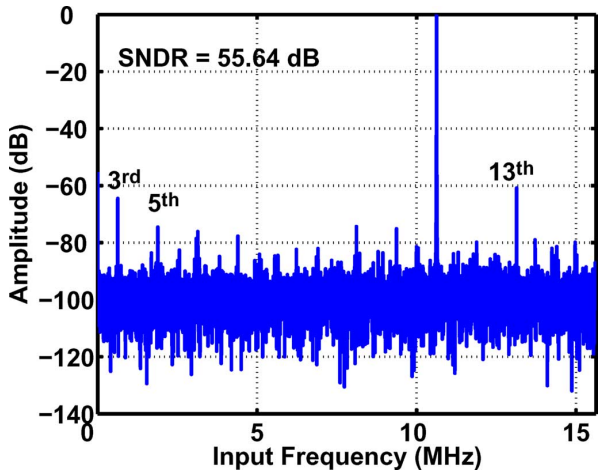

Fig. 19. Output spectrum for 10.7 MHz input frequency at a sampling rate of 500 MHz after calibration.

Figs. 18 and 19 show the measured output spectrum for an input frequency of 10.7 MHz before and after calibration, respectively. The sampling rate is 500 MHz. (Due to the downsampling factor of 16, the spectrum is shown up to half of 500 MHz/16 = 31.25 MHz.) Before calibration, the SNDR is only 28.28 dB. After full calibration, the SNDR improves to 55.64 dB. Since the background calibration is performed at a sampling rate of 100 MHz, operation at 500 MHz suffers slightly from uncorrected gain error and nonlinearity. Also, the fifth-order harmonic remains uncorrected and relatively significant.

Fig. 20 shows the output spectrum for an input frequency of 233 MHz.

The SNDR is equal to 52.8 dB, yielding a figure-of-merit (FOM) of 0.3 pJ/conversion. The degradation is partially attributed to the ringing on the external reference lines that feed the sampling capacitors of all of the MDAC stages. Even though a bypass MOS capacitor of 500 pF is tied on-chip between $+V_{\mathrm{REF}}$ and $-V_{\mathrm{REF}}$, the total capacitance that MDACs switch to these reference reaches 500 fF, creating considerable ringing for a bond wire inductance of greater than 2 nH. It is expected that an on-chip reference buffer improves the dynamic performance.

Fig. 21 plots the measured SNDR as a function of the analog input frequency at a sampling rate of 500 MHz. Table II compares the performance of this ADC with that of prior art.

TABLE II
COMPARISON OF THE PERFORMANCE OF THIS ADC WITH THAT OF PRIOR ART

	This Work	Lee07	Hsu07	Louwsma07	Anthony08
Resolution	10 bits	10 bits	11 bits	10 bits	13 bits
Conversion Rate	500 MHz	205 MHz	800 MHz	1.35 GHz	250 MHz
Supply Voltage	1.2 V	1.0 V	1.3/1.5 V	1.2/1.6 V	1.8 V
Input Voltage	1.2 Vpp	1 Vpp	-	-	1.45 Vpp
Power (mW)	55	61	350	175	140
SNDR (dB)	52.8	53.9	54	48.1	65.9
INL (LSB)	1	0.5	1.6	-	0.7
DNL (LSB)	0.4	0.5	0.5	-	1.5
FOM (pJ/Conv)	0.31	0.65	1.07	0.6	0.28
Technology	90 nm CMOS	90 nm CMOS	90 nm CMOS	0.13 μm CMOS	0.18 μm CMOS
Active Area	0.5 mm^2	1 mm^2	1.4 mm^2	1.6 mm^2	0.89 mm^2

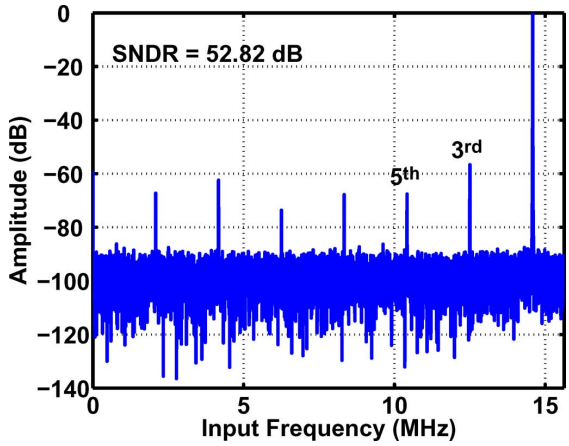

Fig. 20. Output spectrum for 233 MHz input frequency at a sampling rate of 500 MHz.

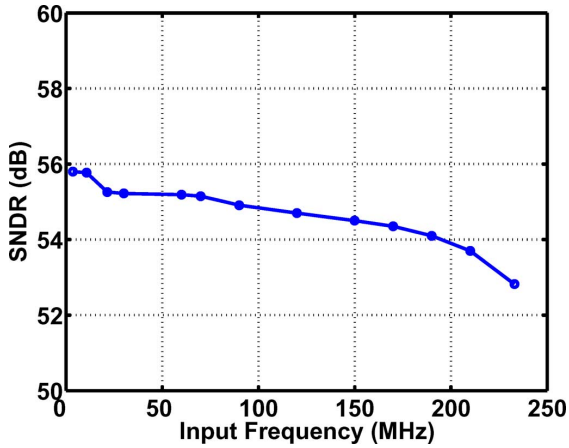

Fig. 21. Measured SNDR as a function of input frequency at a sampling rate of 500 MHz.

VI. CONCLUSION

As each generation of CMOS technology continues to further limit the performance of op amps, calibration techniques that deal with not only gain error but nonlinearity become essential. This paper has introduced a pipelined ADC calibration method and an accurate resistor ladder topology that can remove residue gain error, DAC error, and op amp nonlinearity. Owing to a high-speed low-power op amp design, the ADC achieves 53 dB SNDR reported for a power consumption of 55 mW.

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