EE 215C-Home Work #3, Feb 2nd, 2009 Amir Hadji-Abdolhamid, Email:amirh@ieee.org

The schematic with the component parameters is shown in Fig.1.

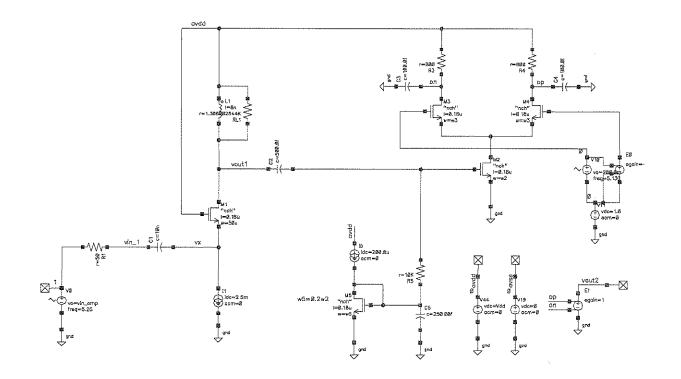


Figure 1: Schematic Diagram

Summary of results:

w1 =

w3=w4=

Conversion Gain: LO(given):

13µm (See Figure 2)

35um (see Figure(3))

(29.67 dB

800mV diff-pk-pk or ~2dBm

LO Leakage at 5.13 GHz: -173dB (The absolute voltage value: -171dbm) LO Leakage at 10.26 GHz: -72.8dB (The absolute voltage value: -70.8dbm)

Output DC offset: 9.45mV (see Fig.9)

IIP3 for vin/2 or input PORT1 power:

IIP3 Total= -18.77 dBm (Šee Figure 12-14)

IIP3 of first stage= -6.27 dBm

IIP3 of 2nd stage(mixer)= 0.01 dBm

(a) Determine the width of M2 for resonance at 5.2GHz:

By looking at ac response at vout1 (Drain of M1) and sweeping of M2 width, the resonance occurs at 5.2GHz when:

w1=13um (See Figure 2),

The gain at vout1 at 5.2 GHz is 8.15 or 18.22dB (relative to vin source) Gain is 24.22dB relative to vin/2 or 22.22 dB relative to node vin_1. Gain from vin to vin 1 is -4dB.

(b)M3/M4 width for maximum conversion gain:

Using transient or pss analysis we look the FFT of differential output of mixer e.g. vout2 in Fig.1. Sweeping w2 and optimizing for maximum IF component at IF=RF-LO=5.2GHz-5.13GHz=70MHz, The input level was set about -40dbm. (after 50 Ohm Rs, well below nonlinearity limits). Result is:

w3=w4=35um (see Figure(3))

Conversion Gain (The Magnitude of differential 70Mhz output to half of 5.2GHz vin input before Rs): 29.67 dB

Note that after part (b) we needed a slight *iteration* of redoing part (a) and (b) to keep both desired resonance frequency and maximum conversion gain. The input level was set about -40dbm. (after 50 Ohm Rs).

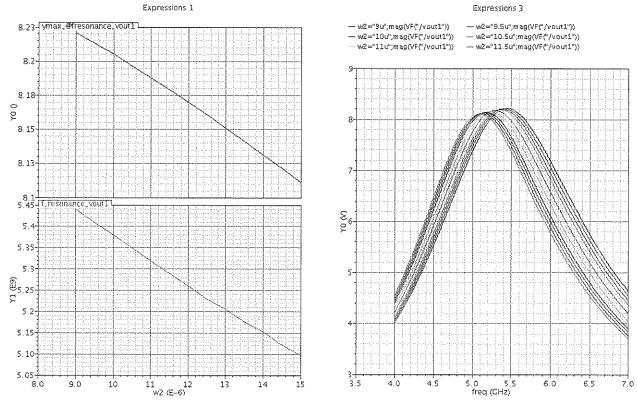


Figure 2: AC output at vout1 for swept w2, w2=13u gives resonance at 5.2GHz

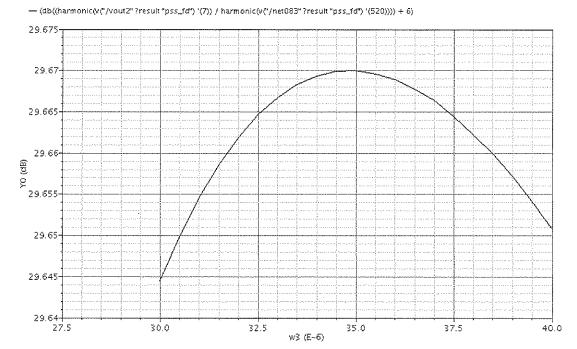


Figure 3: Conversion gain versus swept w3 values, w3=35um gives maximum Conversion gain of 29.67 dB

(c) Determine the LO leakage

This part we used transient analysis or pss to find both time and frequency domain of the LO leakage at the input as the circuit is nonlinear and can't use ac analysis. Also for simplicity of figures input is turned off first but the results are the same even if the input is on. (See Fig 6 and Fig 7 for this)

As shown in Fig. 4 when no mismatch applied to the mixer stage, LO has a very small leakage at LO frequency (and all odd harmonics of it) but there is a considerable second harmonic leakage due to non-linear operation of the mixer.

LO leak over the 50 Ohm Rs or at Vin_1 in Fig.1 relative to differential LO input which is ~2dBm is:

At 5.13 GHz: -173dB (The absolute voltage value: -171dbm) At 10.26 GHz: -72.8dB (The absolute voltage value: -70.8dbm)

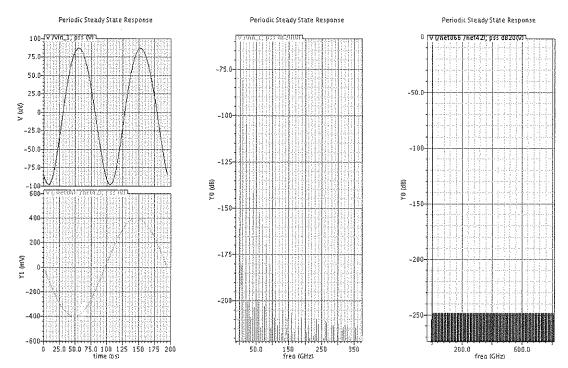


Figure 4:Differential LO versus differential L in time and frequency domain

The LO first (and Odd) harmonics leakage to input are considerably increased in the presence of the mismatch in mixer switches, as an example see below results:

LO leakage after adding 10mV offset for mixer diff-pair of M3-M4 (see Fig. 5):

At 5.13 GHz: -86.6dB (The absolute voltage value: -84.6dbm) At 10.26 GHz: -72.8dB (The absolute voltage value: -70.8dbm)

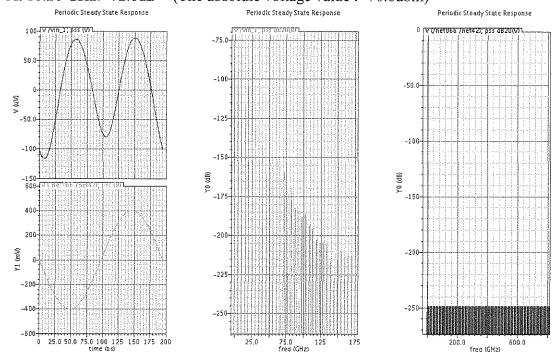


Figure 5: Differential LO versus differential L in time and frequency domain when M4 M5 Vth have 10mV offset

Input ON or OFF effect on the leakage value is negligible

The leakage values are the same when the input is ON or OFF as the input has very small effect on the nonlinear path of the leakage. This was checked because the superposition is valid in linear circuits. Please see Fig 6, and Fig.7.

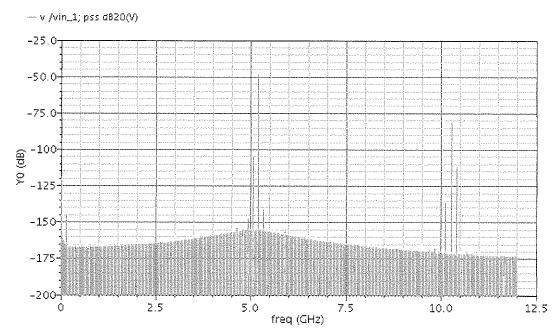


Figure 6 This figure shows the spectrum at the input Vin_1 (after RS) showing LO leakage, High 2nd harmonic LO leakage and negligible first harmonic leakage when the input is On.

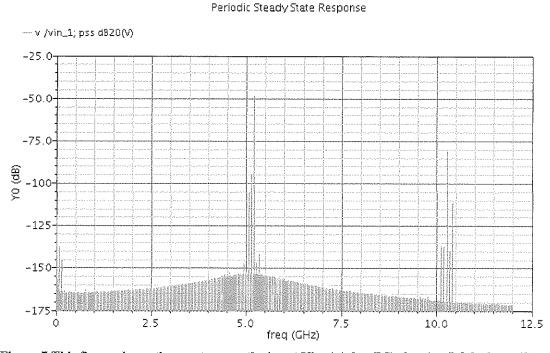


Figure 7 This figure shows the spectrum at the input Vin_1 (after RS) showing LO leakage, High 2nd harmonic LO leakage and NON-negligible first harmonic leakage when the input is On and there exists a 10mV offset in mixer switches.

(c) continued: The LO leakage path

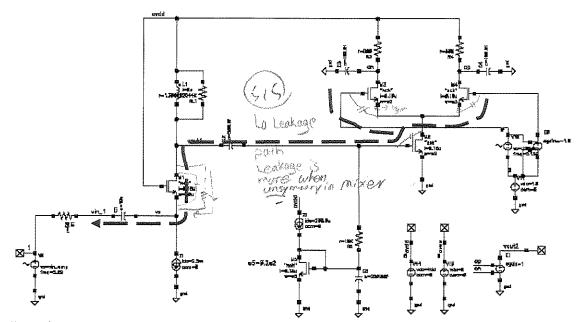


Figure 8: The LO leakage path is shown.

(d) Find output DC offset when M3-M4 Vth have 10mV dc offset and LO has a 8% second harmonic (Non differential as the course instructor has guided)

The schematic test bench for this part is shown in Fig.9.

The time domain signal at the differential IF output (vout2) can be averaged over time or simply we can look at the DC term in FFT response. From either the methods the Output offset is obtained as:

Output DC offset: 9.45mV (see Fig.10)

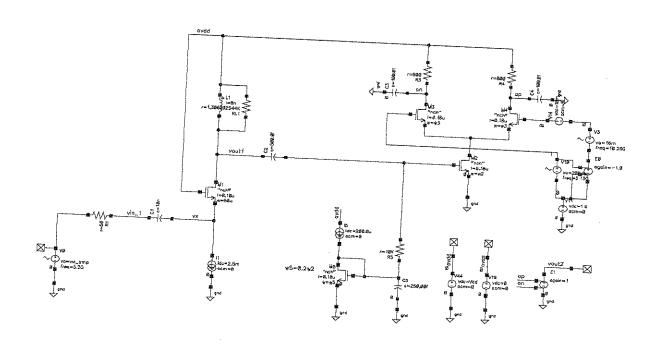


Figure 9as a DC voltage and: Schematic for part (d), Vth offset modeled as DC votage source and alsp non differential second harmonic is added as an another votage source

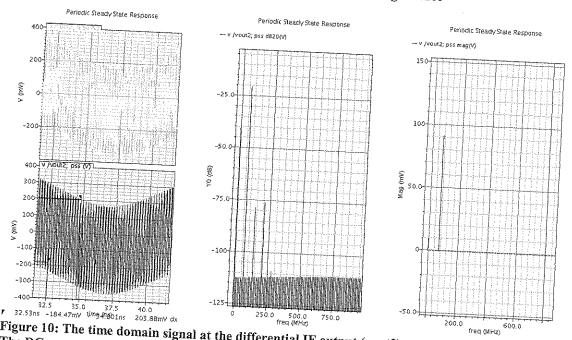


Figure 10: The time domain signal at the differential IF output (vout2) and its frequency response. The DC component is shown and is 9.45mV. This is same as the average of time domain signal. We see pss and transient analysis have same time domain results.

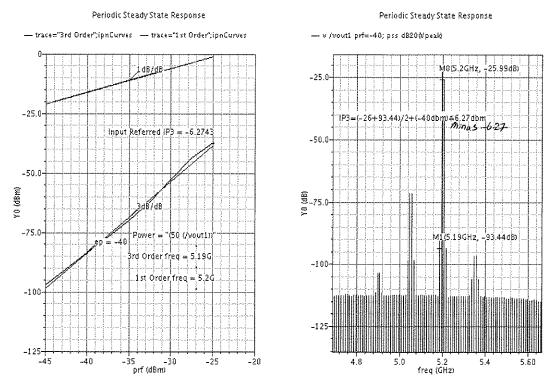


Figure 13: IIP3 calculation for the first stage at pin=-40dbm

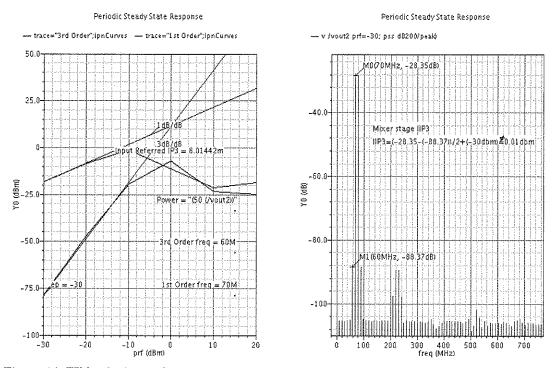


Figure 14: IIP3 calculation for the second stage at pin=-30db