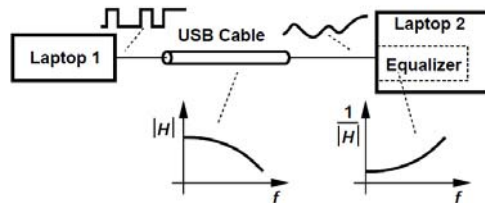


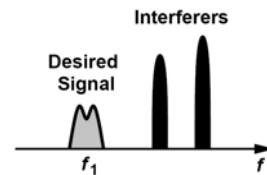
Why Analog?

- Naturally-occurring signals, e.g., voice and video, are analog.
- System and medium non-idealities often make it necessary to treat digital signals as analog:

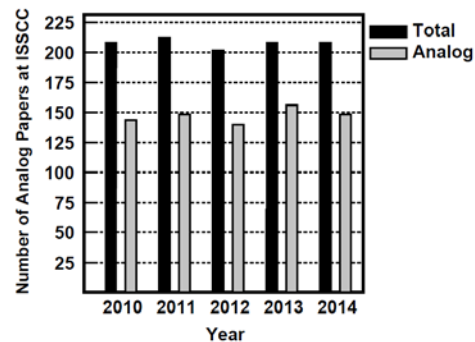
o Data on a USB Cable



o Digital Wireless Communications



Analog Design Is Far From Dead



Why is analog design such a big deal?

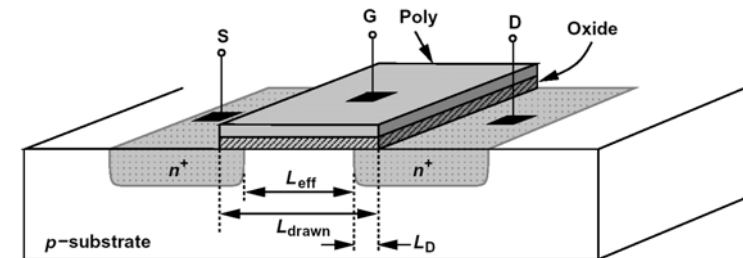
- Entails more trade-offs than digital design:



- More sensitive to noise and cross-talk.
- More sensitive to second-order effects in devices.
- More difficult to automate.
- More difficult to model and simulate.
- More sensitive to process, supply voltage, temperature (PVT)

REVIEW OF MOS DEVICES

MOS Structure (NMOS)

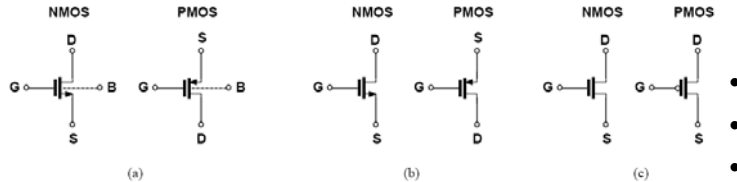


- A piece of polysilicon with a width of W and length of L on top of a thin layer of oxide defines the gate area.
- Source and drain areas are heavily doped.
- Substrate usually tied to the most negative voltage.
- $L_{eff} = L - 2L_D$, where L_D is the side diffusion of source and drain.

MOS Symbols (Enhancement Type)

PMOS

NMOS

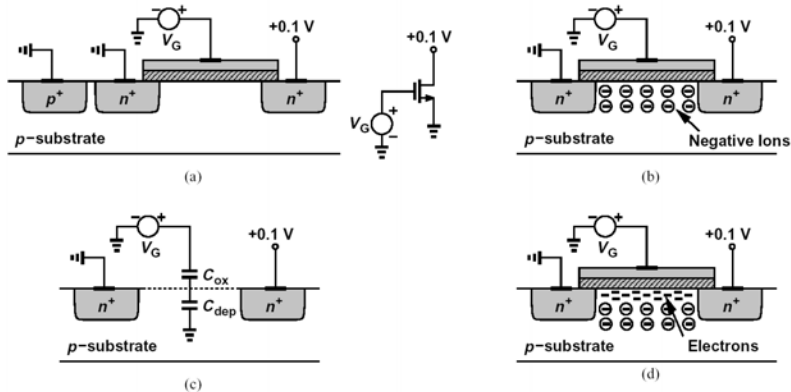


- MOS structure is symmetric.
- MOS devices have a very high input impedance.

MOS characteristics

- o How does the device turn on and off?
- o What is the drain-source current when the device is on?

Threshold Voltage



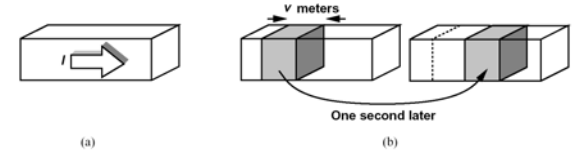
- For $V_{GS} < V_{TH}$, holes in substrate are repelled from gate area, leaving negative ions behind. (No current flows because no carriers are available.)
→ A depletion region forms under the gate.

- For $V_{GS} \approx V_{TH}$, electrons are attracted to the interface under gate, establishing a “channel” for conduction. The channel is also called the “inversion layer.”

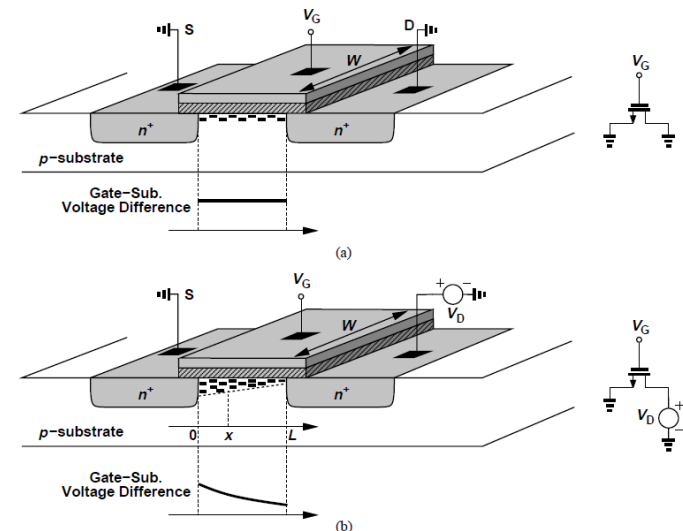
- For $V_{GS} \approx V_{TH}$, depletion region under channel remains relatively constant, but the charge in inversion layer increases.
- Turn-on process not really abrupt, i.e., for $V_{GS} \approx V_{TH}$, $I_D > 0$. → Sub-threshold conduction (considered later).

- A helpful approximation: For $V_{GS} \approx V_{TH}$, there is only depletion region in the gate area; for $V_{GS} \approx V_{TH}$, the depletion region is constant and the inversion layer charge increases.

- A useful Lemma: If a conductor carries a constant current I and it has a charge density (charge per unit length) of Q_d and the charge moves with a velocity v :
 $I = Q_d v$



MOS I – V Characteristics



- For $V_{DS} > 0$, the inversion layer charge is non-uniform:

$$Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}]$$

Note that as we approach the end of the channel, the charge density falls.

- To find the current, multiply charge density by charge velocity. For a semiconductor:

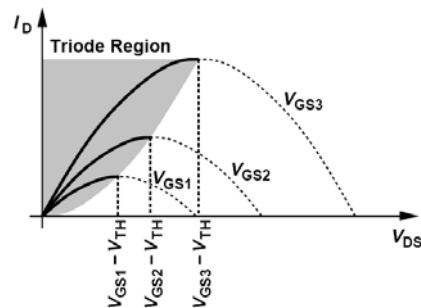
The drain current is therefore given by

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

subject to boundary conditions at the two ends of the channel. Thus,

$$\int_{x=0}^L I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dx$$

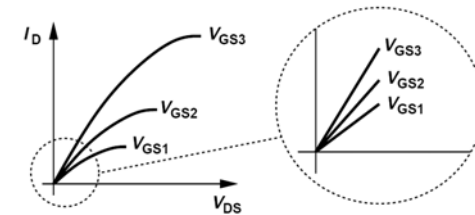
and hence,



- Assumptions made:
 - One-dimensional structure
 - Constant mobility
 - Constant depletion layer charge

- For small V_{DS} ,

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$



Each line represents an ohmic resistor of

$$R_{on} =$$

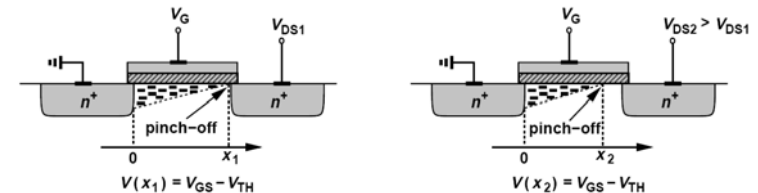
Thus, a MOS device can operate as a resistor whose value is controlled by V_{GS} (so long as $V_{DS} \ll 2(V_{GS} - V_{TH})$):



- Note that the device can be on but have zero current, which occurs only if $V_{DS} = 0$.

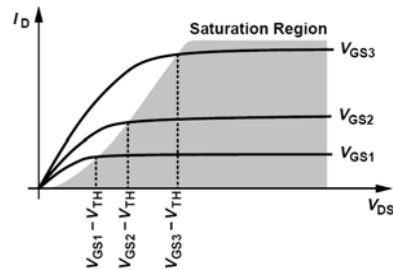
Pinch-Off

- What happens if $V_{DS} > V_{GS} - V_{TH}$?

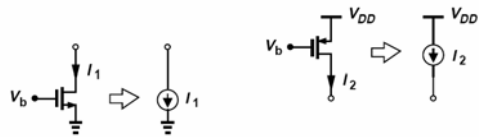


- Electrons reach a high velocity near the end of inversion layer and shoot into depletion region around the drain.

- Device has entered the “saturation region.”

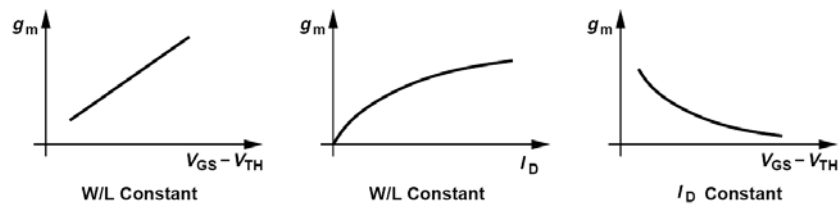


- In saturation region, I_D is independent of V_{DS} $\Rightarrow$ device acts as a current source:

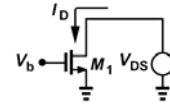


Concept of Transconductance

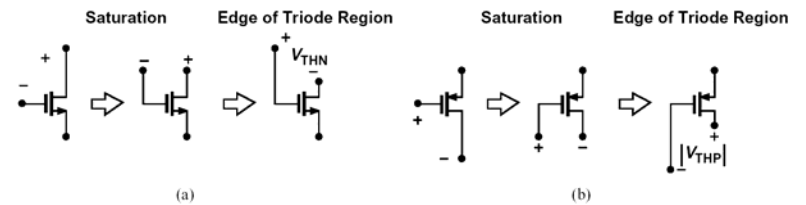
$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$



Example

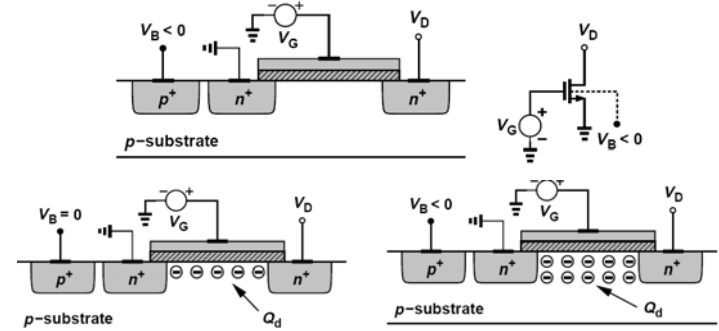


Conceptual Visualization



Other Phenomena

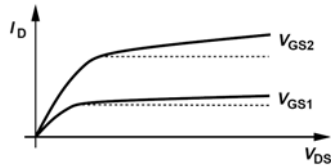
1. Body Effect:



- As V_B becomes more negative, more holes can break loose from atoms under the gate area, leaving negative ions behind $\Rightarrow$ depletion region can contribute more charge $\Rightarrow$ inversion layer forms for larger V_G $\Rightarrow$ threshold voltage $\uparrow$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}) \quad \gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$

2. Channel Length Modulation



- As $V_{DS} \uparrow$, the width of depletion region between inversion layer and drain $\uparrow \Rightarrow$ Effective channel length $\downarrow = I_D \uparrow$

$$I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

3. Mobility Degradation with Vertical Field

- As $V_{GS} \uparrow$, vertical field $\uparrow \Rightarrow$ carriers travel closer to interface and experience more scattering $\Rightarrow$ mobility falls:

4. Mobility Degradation with Lateral Field

- At high electrical fields, electrons experience substantial scattering from lattice and eventually travel at a constant velocity: $I = Q_d v$

Consequences of Velocity Saturation:

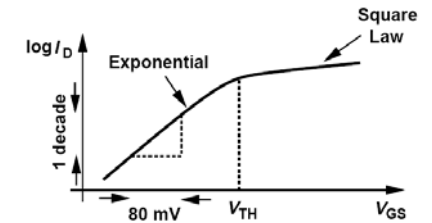
- Drain current saturates before pinch-off $\Rightarrow$ it's lower than predicted by square law.
- Transconductance is relatively independent of current and channel length. Why?

5. Subthreshold Conduction

For V_{GS} near V_{TH} , I_D has an exponential dependence on V_{GS} :

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T}$$

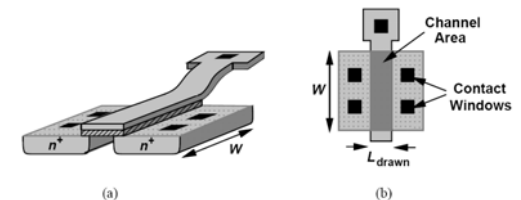
if V_{DS} is greater than roughly 200 mV. This conduction is important in very large circuits, e.g., memories, because it results in finite stand-by current.



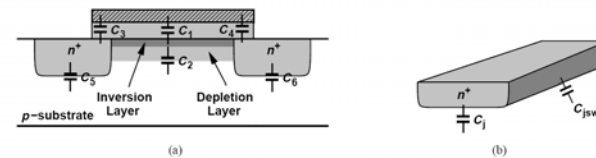
6. Temperature Effects

The mobility and threshold voltage vary with temperature:

Device Layout



MOS Capacitances

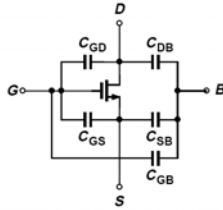


Gate – Channel Cap. $C1 =$
 Gate - S/D Overlap Cap. $C2 = C3 =$
 Gate – Bulk Cap. $C4 =$

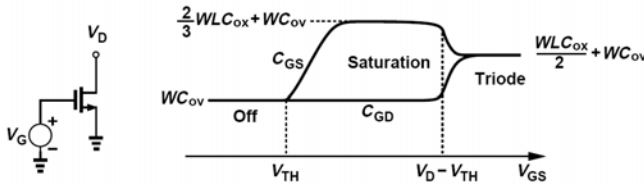
Source and drain junction caps consist of two components: sidewall and bottom plate. Each component can be expressed as:

$$C_j = C_{j0} / [1 + V_R / (2\Phi_F)]^m$$

where m is typically between 0.3 and 0.5. The device thus looks like this:

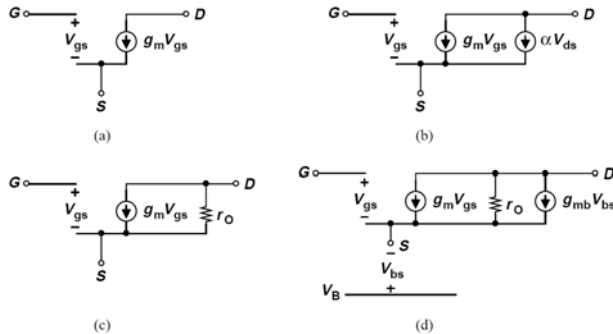


NOTE: Depending on the region of operation (off, triode, sat.), the equivalent capacitances between terminals assume different values.



Small-Signal Model

The model can be developed by perturbing the voltage difference between each two terminals and measuring each resulting current change.



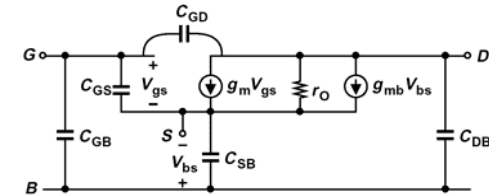
For body effect:

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \left(-\frac{\partial V_{TH}}{\partial V_{BS}} \right)$$

and hence:

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m,$$

Complete Model:



SPICE MOS Model

The following parameters are the bare minimum SPICE needs to simulate circuits.

VTO: threshold voltage with zero V_{SB}

GAMMA: body effect coefficient

PHI: $2\Phi_F$

TOX: gate oxide thickness

NSUB: substrate doping

LD: source/drain side diffusion

UO: channel mobility

LAMBDA: channel-length modulation coefficient

CJ: source/drain bottom-plate junction capacitance per unit area

CJSW: source/drain sidewall junction capacitance per unit length

PB: source/drain junction built-in potential

MJ: exponent in CJ equation

MJSW: exponent in CJSW equation

CGDO: gate-drain overlap capacitance per unit width

CGSO: gate-source overlap capacitance per unit width

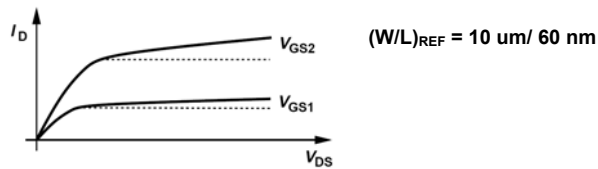
JS: source/drain leakage current per unit area

Modern MOS models have several hundred parameters.

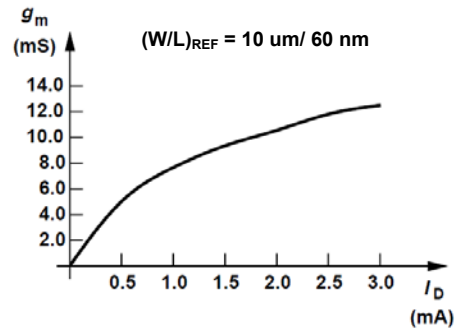
Design in Deep-Submicron CMOS

It is difficult to represent deep-submicron devices by a square-law model. In actual design, we take a pragmatic approach:

(1) Construct I/V characteristics for a given W/L using simulations:



(3) Using simulations for $(W/L)_{REF}$, plot g_m as a function of I_D :



(3) Based on the require current and tolerable V_{ds} , scale the transistor width $\rightarrow g_m$ also scales.

The Return of the Quadratic Monster

For nodes below 20 nm, FinFETs are replacing the planar MOS structure. These devices have nearly square-law characteristics!

