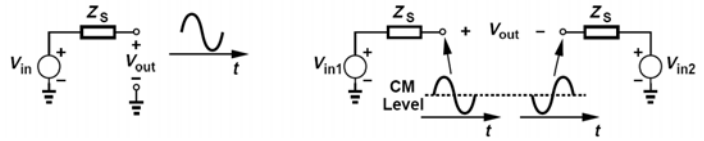
Differential Amplifiers

- **Differential & Single-Ended Operation**

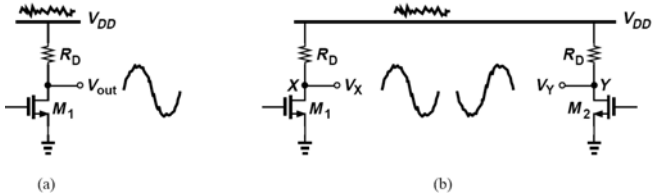
- A single-ended signal is taken with respect to a fixed potential (usually ground).

- A differential signal is taken between two nodes that have <u>equal</u> and <u>opposite</u> signals with respect to a "common mode" voltage and also equal impedances to a fixed potential (usually ground).

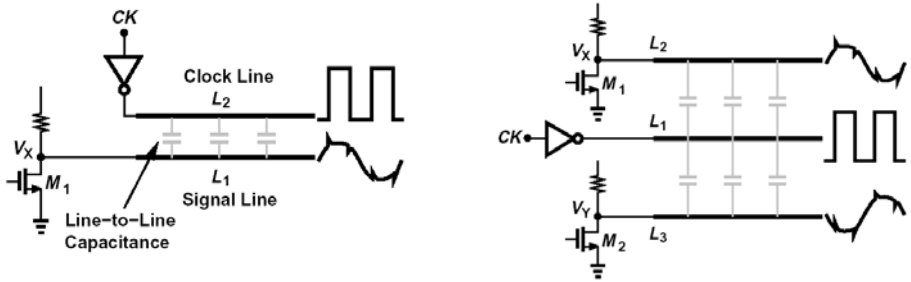


- **Why Differential?**

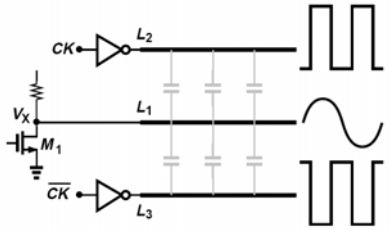
o **Rejection of common-mode disturbance: supply noise, etc.**



o **Rejection of coupling & feed through <u>from</u> other sources:**

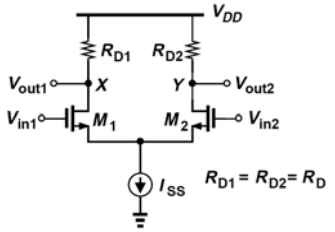


o **Reduction of coupling <u>to</u> other circuits;**

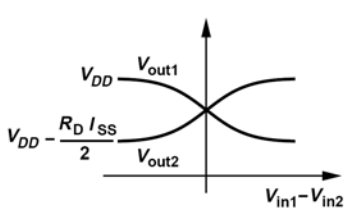


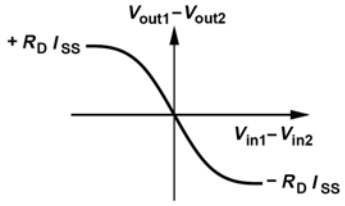
o **Maximum voltage swing almost twice that in single-ended operation;**
o **Even-order distortion suppressed (discussed later);**
o **Biasing is easier.**

<u>Basic Differential Pair</u>



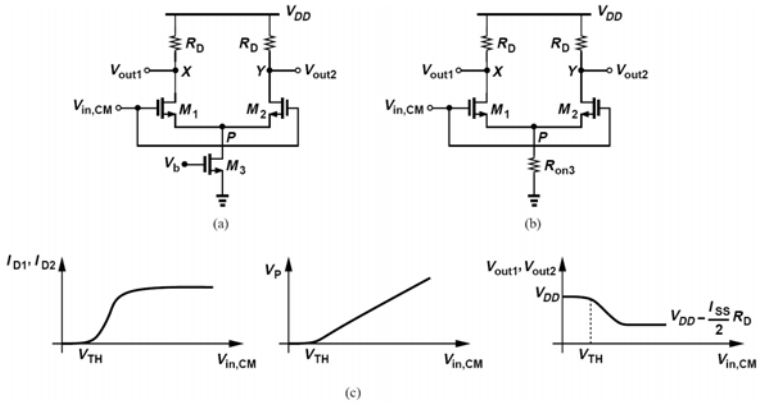
- Quantitative Analysis
Differential Behavior:





Where does the maximum small-signal gain occur?

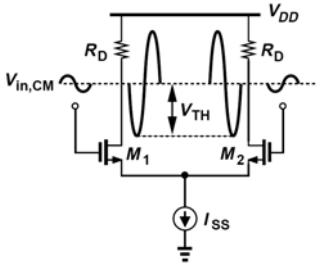
Common-Mode Behavior:



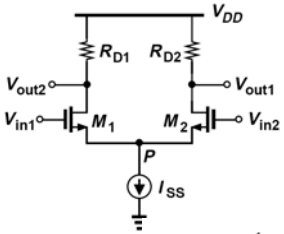
Observations:

- **The small-signal gain drops as the difference between V_{in1} and V_{in2} increases.**
- **The input and output common-mode levels must be chosen carefully. The current source requires some voltage so as to exhibit a high output impedance.**

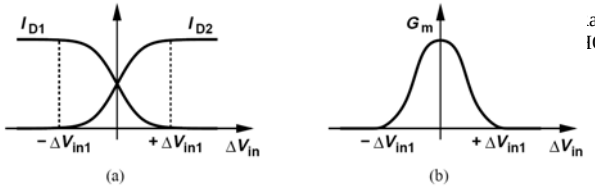
How large can the output swings be?



Large-Signal Analysis



$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$



Note: If neglect sub-threshold behavior, for some $V_{in1} - V_{in2}$ one transistor completely turns off. This occurs for a differential input of :

$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

This can be related to the overdrive at equilibrium:

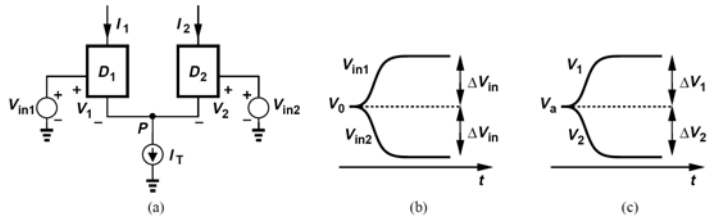
- **To achieve a wider linear range for $V_{in1} - V_{in2}$, need greater (equilibrium) overdrive. For a given bias current, this translates to lower transconductance for each device.**
- **How does the input-output characteristic change as W changes?**

Small-Signal Analysis

If the circuit is perfectly symmetric and V_{in1} and V_{in2} change by equal and opposite amounts from equilibrium, then we can use the concept of "half circuit."

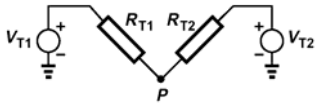
Lemma

In the following symmetric circuit, if V_{in1} changes from V_0 to $V_0+\Delta V$ and V_{in2} changes from V_0 to $V_0-\Delta V$, then V_x does not change.

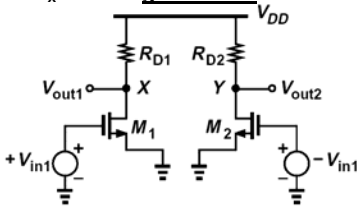


$$g_m\Delta V_1 + g_m\Delta V_2 = 0 \qquad V_0 + \Delta V_{in} - (V_a + \Delta V_1) = V_0 - \Delta V_{in} - (V_a + \Delta V_2)$$

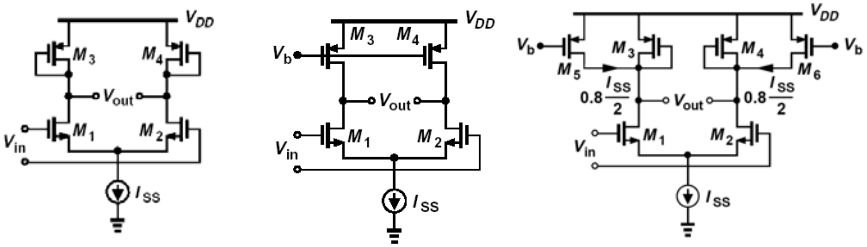
From another point of view, one transistor wants to pull V_x up while the other wants to pull it down.



=> V_x can be grounded.



Other Types of Loads

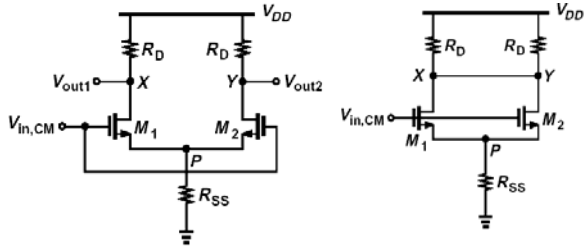


Calculate the voltage headroom requirement and small-signal gain.

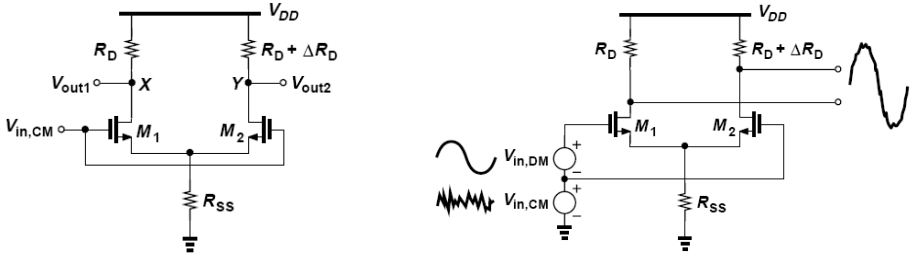
How do we increase the gain of diff pair with current source loads?

Common-Mode Response

Case I : Symmteric Circuit



Case II: Asymmetric Circuit



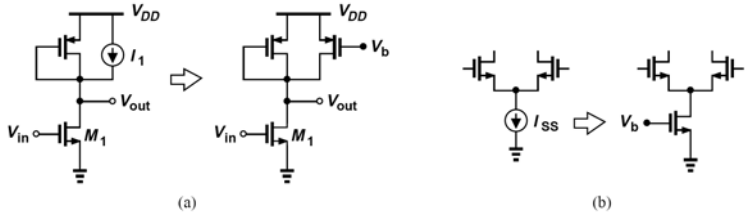
Effect of load resistance mismatch:

$$\Delta V_X = \Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} R_D$$

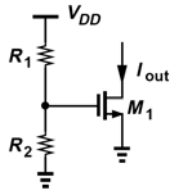
$$\Delta V_Y = \Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} (R_D + \Delta R_D)$$

Current Mirrors & Active Loads

In analog design (and sometimes digital design), we may need to generate many well-defined bias currents. For example:

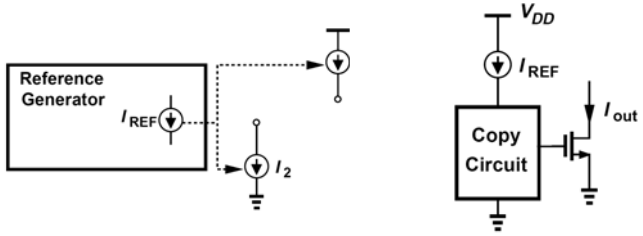


Each current source can be realized as:

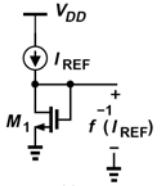


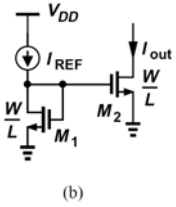
If we apply a self-defined <u>voltage</u> to the gate or the base, the current is NOT well-defined. In MOSFETs, V_{TH} can vary by tens of millivolts from wafer to wafer, causing significant error.

Better approach:

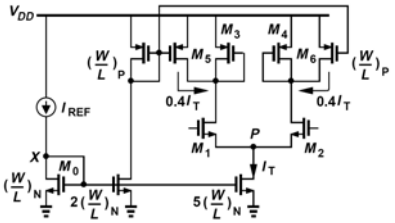


So, all we need to generate is one reference current. I_{REF} is established by precision bandgap techniques or sometimes provides externally.

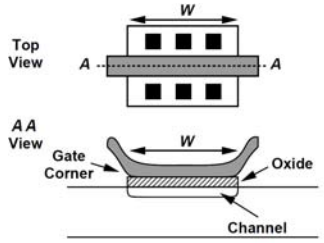


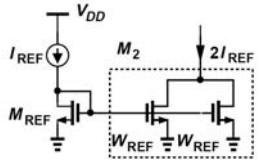


Example:



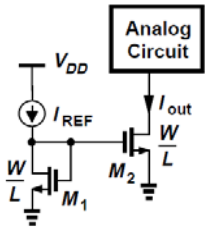
<u>The Gate Corner Problem</u>



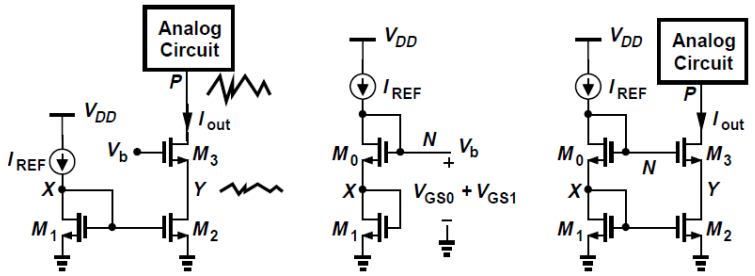


<u>Cascode Current Mirrors</u>

Channel-length modulation causes error if the voltage across the diode-connected device is not equal to V_{DS} of current sources.

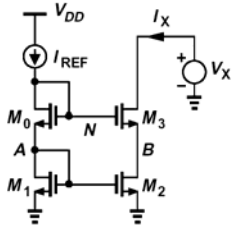


Solution 1: Standard Cascode

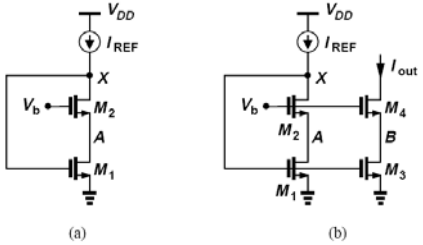


- **What is the minimum allowable voltage across the current source?**

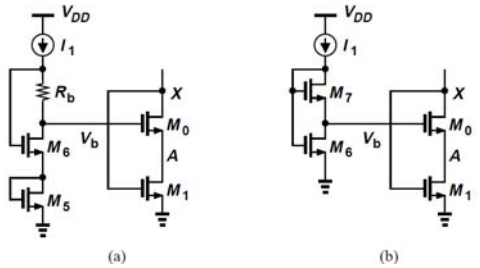
Example:



Solution 2: Low-Voltage Cascode

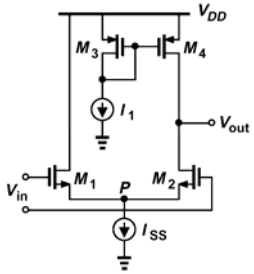


How to generate Vb?



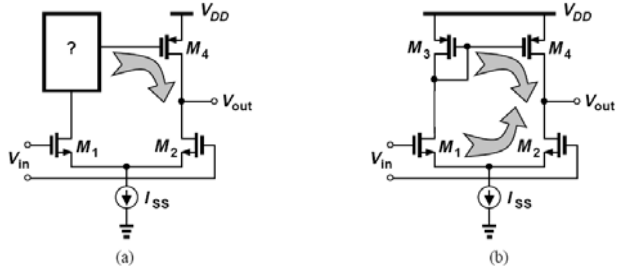
Active Current Mirrors

Diff Pair with Passive Load: Suppose we need a high-gain differential amplifier with single-ended output:

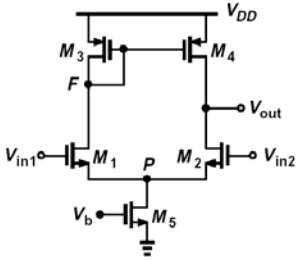


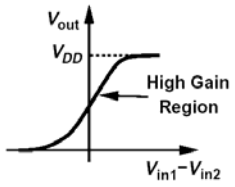
What is the voltage gain?

Diff Pair with Active Load:

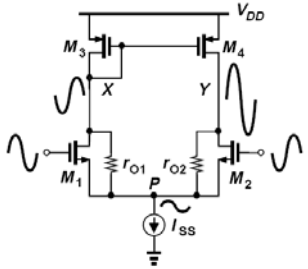


Large-Signal Behavior:

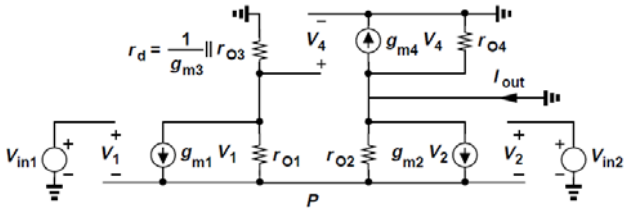




Small-Signal Behavior:



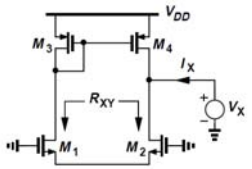
Calculate the gain as $-G_mR_{out}$. First, G_m:

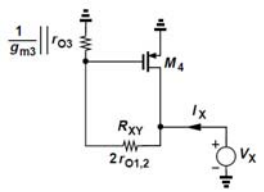


$$g_{m2}V_2 - \frac{V_{in2} - V_2}{r_{O2}} = \frac{V_4}{r_D} \qquad (-\frac{V_4}{r_d} - g_{m1}V_1)r_{O1} + V_{in1} - V_1 = V_4$$

$$G_m = -g_{m1}r_{O1}\frac{g_{m4}r_d + 1}{r_d + 2r_{O1}}$$

Second, R_{out}:





$$I_X = \frac{V_X}{2r_{O1,2} + \frac{1}{g_{m3}} \| r_{O3}} \left[1 + \left(\frac{1}{g_{m3}} \| r_{O3}\right) g_{m4}\right] + \frac{V_X}{r_{O4}}$$

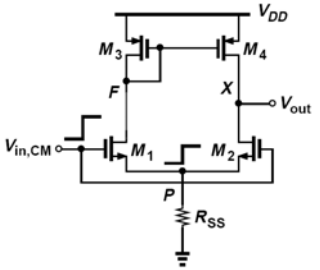
$$\frac{I_X}{V_X} = \frac{1 + g_{m4}r_d}{2r_{O1} + r_d} + \frac{1}{r_{O4}} = \frac{(1 + g_{m4}r_d)r_{O4} + 2r_{O1} + r_d}{(2r_{O1} + r_d)r_{O4}}$$

$$|A_v| = g_{m1}(r_{O1} \| r_{O4}) \frac{2g_{m4}r_{O4} + 1}{2(g_{m4}r_{O4} + 1)}$$

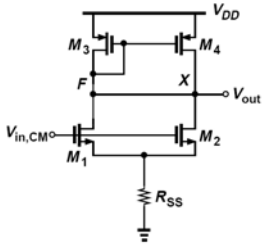
What is the dc output voltage in equilibrium?

How do we increase the voltage gain?

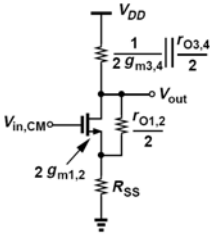
<u>Common-Mode Rejection</u>



What is the common-mode gain?

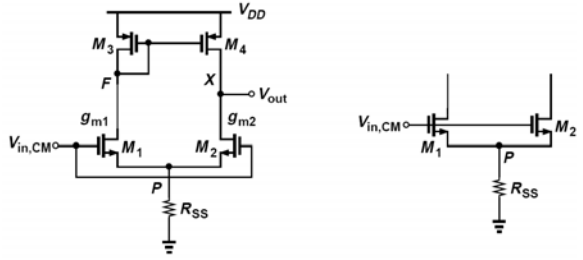


(a)



(b)

Thus, even if the circuit is perfectly symmetric, CMRR is not infinite. In practice, random mismatches between the two sides result in a finite CMRR.



(a)

(b)

$$\Delta V_P = \Delta V_{in,CM} \frac{R_{SS}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}}$$

$$\begin{aligned} \Delta I_{D1} &= g_{m1}(\Delta V_{in,CM} - \Delta V_P) \\ &= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m1}}{g_{m1} + g_{m2}} \\ \Delta I_{D2} &= g_{m2}(\Delta V_{in,CM} - \Delta V_P) \\ &= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m2}}{g_{m1} + g_{m2}}. \end{aligned}$$