EE 215A B. Razavi

Fall 14 HO #6

Homework #2

Due Tue., Oct. 21, 2014

1. Problems from text: 3.6, 3.7, 3.9, 3.16(a), 3.18(c), 3.19(d), 3.20(e), 3.21(h), 3.22(b).

2. The following circuit is a cascode amplifier with capacitive feedback (to set the gain) and dc feedback (to set the bias). For this problem, use the device models posted on the web. For all of the transistors, the *drawn* dimensions are $W/L = 30/0.18$. Assume $V_{DD} = 1.8$ V.

(a) Calculate V_{b1} and V_{b2} such that M_1 and M_4 are at the edge of saturation (when M_2 and M_3 are saturated).

(b) Find the maximum output voltage swing for "midband" frequencies.

(c) Calculate the gain from A to V_{out} (the open-loop gain) and from V_{in} to V_{out} (the closed-loop gain). Neglect the loading introduced by the capacitors.

(d) Confirm the results obtained in (c) by SPICE or Cadence simulations. (You only need to report the bias currents and the voltage gain computed by SPICE or Cadence and provide a hardcopy of your netlist or schematic.) (Do NOT print black Cadence schematics or plots; change their background as explained in the tutorial.)