EE 215A B. Razavi

Fall 14 HO #17

Final Project

Due Fri., Dec. 12 , 2014 (No Electronic Submission Except for MSOL Students)

In this project, each team of two persons will design two versions of a fully-differential high-speed high-precision amplifier.

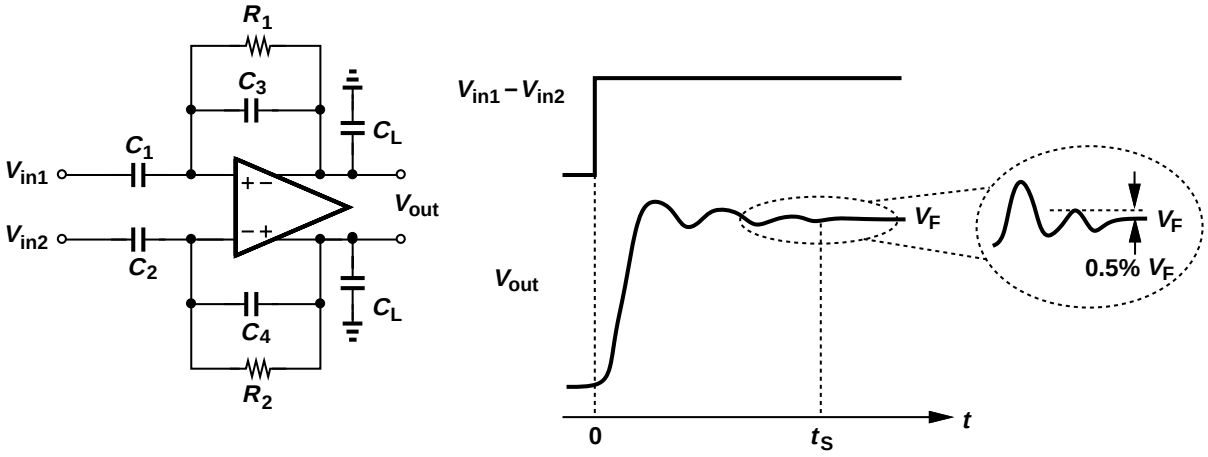
Design Specifications

Each design must satisfy the following specifications:

- Gain = 8
- Differential Output Swing = 1.8 V
- Gain Error $<$ 1%
- C_L = 1 pF
- Supply Voltage = 1.8 V

The first design will have a power budget of 10 mW and aims to minimize the large-signal settling time to 0.5% accuracy. The second design targets a 0.5% large-signal settling time of 40 ns and aims to minimize the power dissipation. It is beneficial for the two persons to interact and understand each other's speed-power trade-offs.

Illustrated below is a possible implementation of the circuit along with the definition of the settling time:



Resistors R_1 and R_2 establish dc feedback but are large enough not to affect the settling behavior for time scales of a few tens of nanoseconds. Note that each of C_1-C_4 is accompanied with a bottom-plate parasitic capacitance of 20% to ground (which you need to add in your simulations). Matching considerations limit the minimum value of each capacitor to 0.3 pF.

Simulations

You need to simulate the circuit for:

- Gain error with a full-scale output swing
- Output settling behavior near the full scale

Project Report

Each team provides one report including both designs. At the beginning of your report, mention who has designed which version. Your report is an important part of your final project. Do not leave it until the last moment. It should be a concise, yet accurate presentation of your design, describing the circuit details and simulation results. The entire report, including the simulation results, must not exceed 10 pages.