## **Low-Noise Amplifiers**

### **Design Specs**

 Noise Figure: requires very low noise in the input device. For a simple CS stage, the transistor gm must exceed 1/(25 ohms) if the noise figure is to remain below 2 dB.

Exercise: calculate the NF if the metal line connecting to the gate has a resistance of Rm.

→ Only one device should dominate NF. → limited number of topologies to choose from.

- Gain: Must be large enough to minimize noise contributed by mixer. Trades with IP3.
- Input Matching:
  - Do we need conjugate matching at the input?
  - Do these concerns pertain to the other stages in the RX chain?
- How do we quantify the matching? The input return loss is defined as 10  $\log \left| \Gamma \right|^2$  , where

 $\Gamma = \frac{Z_{in} - R_0}{Z_{in} + R_0}$ 

A return loss of better than 10 dB is considered adequate.

 Stability: Since the LNA interfaces with the outside world, it must remain stable with almost any source impedance and at <u>all</u> frequencies.
 Traditional microwave design uses the Stern factor to measure stability:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \Delta = S_{11}S_{22} - S_{12}S_{21}$$

If K>1 and  $\Delta$ <1, the circuit is unconditionally stable.

- Complications: Since the LNA output is not matched, S22 becomes rather irrelevant

Example: Determine K for a simple CS stage at low frequencies.

Conclusion: We design LNAs with high reverse isolation.

- Linearity: In most systems, LNAs do not limit the RX linearity. One exception is CDMA.
- Bandwidth: The bandwidth must accommodate the entire band specified by the standard.

Exercise: An 11a LNA has a 3-dB bandwidth from 5 to 6 GHz. If the LNA load is an inductor, determine the maximum tolerable Q.

#### **Problem of Input matching**

- As explained earlier, the input match cannot be created by tying a physical 50-ohm resistor from input to ground.

Exercise: How about tying a parallel inductor that resonates with the input capacitance and also provides a 50-ohm match?

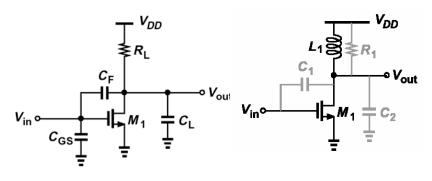
→ Need to create an input resistance of 50 ohms without the noise of a 50-ohm resistor.

#### **LNA Topologies**

Common–Source Stage with	Common–Gate Stage with	Broadband Topologies
■ Inductive Load	■ Inductive Load	■ Noise-Cancelling LNAs
■ Resistive Feedback	■ Feedback	■ Reactance–Cancelling LNAs
■ Cascode,	■ Feedforward	
Inductive Load, Inductive Degeneration	<ul><li>Cascode and Inductive Load</li></ul>	

#### CS Stage with Inductive Load

- Inductor consumes little headroom and resonates with load capacitance.
- The input impedance is given by:



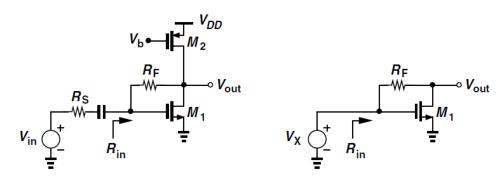
$$Z_{in}(j\omega) = \frac{1 - L_1(C_1 + C_F)\omega^2 + jR_S(C_1 + C_F)\omega}{[-(R_SC_1 + g_mL_1)\omega + j(g_mR_S - L_1C_1\omega^2 + 1)]C_F\omega} \quad \text{real part}$$

The

can be obtained as:

$$Re\{Z_{in}\} = \frac{g_{m}L_{1}^{2}(C_{1}+C_{F})\omega^{2} + R_{S}(1+g_{m}R_{S})(C_{1}+C_{F}) - (R_{S}C_{1}+g_{m}L_{1})}{D}\omega$$

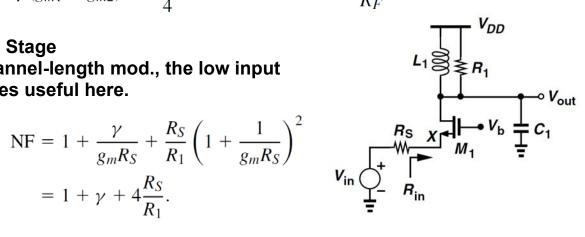
- Can choose the values to set the real part to 50 ohms. But it goes negative at lower frequencies.
- CS Stage with Resistive Feedback



$$\overline{V_{n,out}^2}|_{M1,M2} = 4kT\gamma(g_{m1} + g_{m2})\frac{(R_F + R_S)^2}{4} \qquad \text{NF} \approx 1 + \frac{4R_S}{R_F} + \gamma + \gamma g_{m2}R_S$$

 Common-Gate Stage If we neglect channel-length mod., the low input impedance proves useful here.

NF = 
$$1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1} \left( 1 + \frac{1}{g_m R_S} \right)^2$$
  
=  $1 + \gamma + 4 \frac{R_S}{R_1}$ .



Exercise: Compute the NF including the noise of the current source and Channel-length modulation.

#### **Old Mentality:**

The tight relationship between the input matching and NF in the CG stage is problematic. We can lower the NF if we allow the input resistance to be higher than Rs.  $v_{00}$ 

- In deep submicron technologies, the situation changes:

Sketch the input resistance vs. freq.

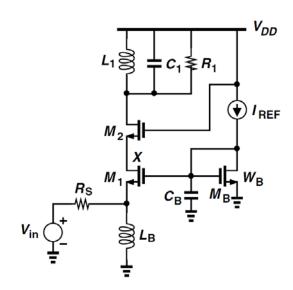
If we set the input resistance equal to Rs,

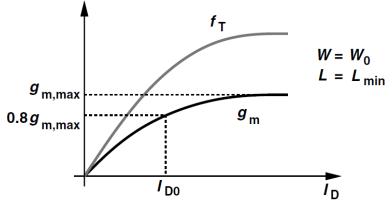
$$\begin{split} \frac{V_{out}}{V_{in}} &= \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_OR_S + R_S + R_1} R_1 \\ \frac{V_{out}}{V_{in}} &= \frac{(g_m + g_{mb})r_O + 1}{2(1 + r_O/R_1)} \end{split}$$

Remedy: Add a cascode:

But the cascode device contributes some noise and consumes headroom → the tail bias has less headroom and more noise.

- Design Procedure:
- (1) Using simulations, plot gm vs. Id for a given W. Pick the Id that gives 80-90% of saturated gm. ("~optimum Id-W combination")

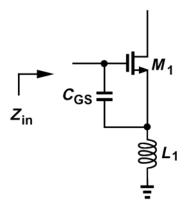


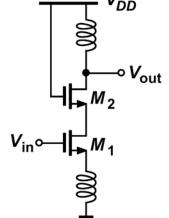


- (2) Scale W and Id to obtain 1/(gm + gmb)=50 ohms.
- (3) Compute necessary value of source inductance. → its Rp must be high enough.
- (4) As a guess, select width of cascode equal to width of input device.
- (5) Find load inductance to resonate with total output cap.

Refer to detailed example in the book.

• Cascode CS Stage with Inductive Degeneration

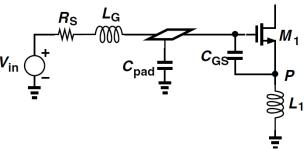




- We often need to  $\underline{reduce} \; f_T$  of the transistor to obtain 50 ohms!
- But Cgd and the input pad capacitance also lower the real part:

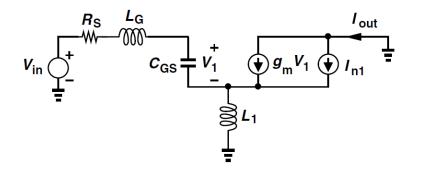
It can be proved that the real part falls to:  $R_{eq} pprox \left(rac{C_{GS1}}{C_{GS1} + C_{pad}}
ight)^2 R_1$ 

- Also need a series inductor at input:



Exercise: A 5-GHz LNA requires an Lg of 2 nH. If the Q is 5, can we build this on-chip?

- → In most cases, both inductors are off-chip.
- Computation of Noise Figure



$$\overline{I_{n,out}^2}|_{M1} = kT\gamma g_m$$

$$NF = 1 + g_m R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2$$

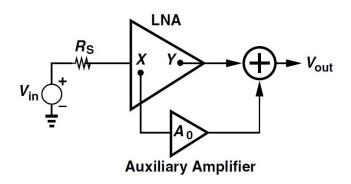
- Design Procedure: Start with three knowns: center freq., value of deg. Inductance, value of input series inductance. The following two equations govern the design:  $NF = 1 + g_{m1}R_S\gamma \left(\frac{\omega_0}{\omega_T}\right)^2$ 

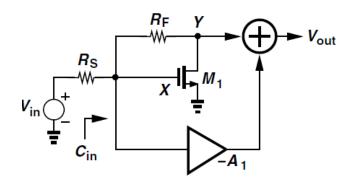
$$R_S = \left(\frac{C_{GS1}}{C_{GS1} + C_{rad}}\right)^2 L_1 \omega_T$$

- (1) Compute Cgs1, gm1, and  $\omega_{T1}$
- (2) May need to reduce ft.
- (3) As a guess, choose width of cascode device equal to width of input device (with minimum length).
- (4) Choose load inductance to resonate with the load cap.
- (5) Reexamine input match.

Refer to example in the book.

# Noise-Canceling LNAs Identify two nodes at which signal appears with opposite polarities and noise of input devices with the same polarity. [Bruccoleri, JSSC, Feb.04]



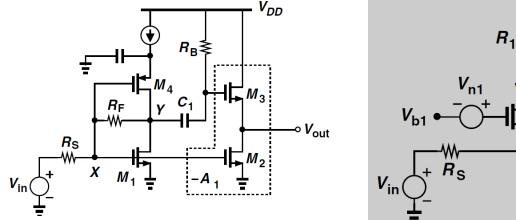


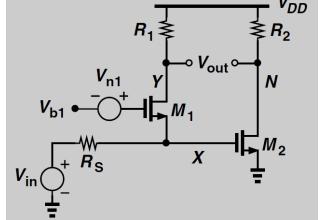
#### How do we choose A1 to ensure noise cancellation?

$$NF = 1 + \frac{R_S}{R_F} + \frac{\overline{V_{nA1}^2}}{4kTR_S} \left(1 + \frac{R_S}{R_F}\right)^2$$

Exercise: Find the NF of the circuit including the input-referred noise voltage of the aux. amplifier.

#### - Implementations:





### **Differential LNAs**

To achieve a high IP2, direct-conversion receivers may incorporate differential LNAs. But now a "balun" is required:

