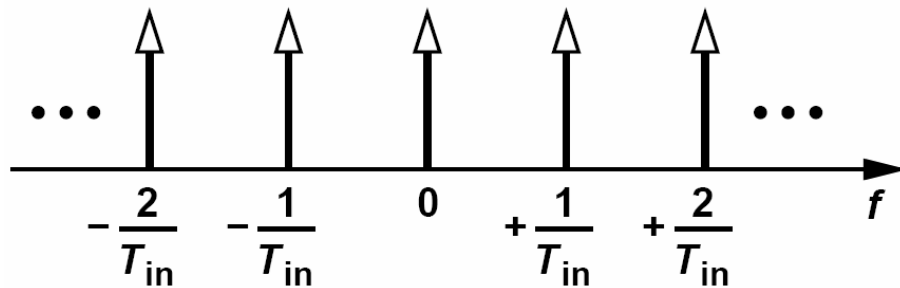# *Other Effects in PLLs*

Behzad Razavi
Electrical Engineering Department
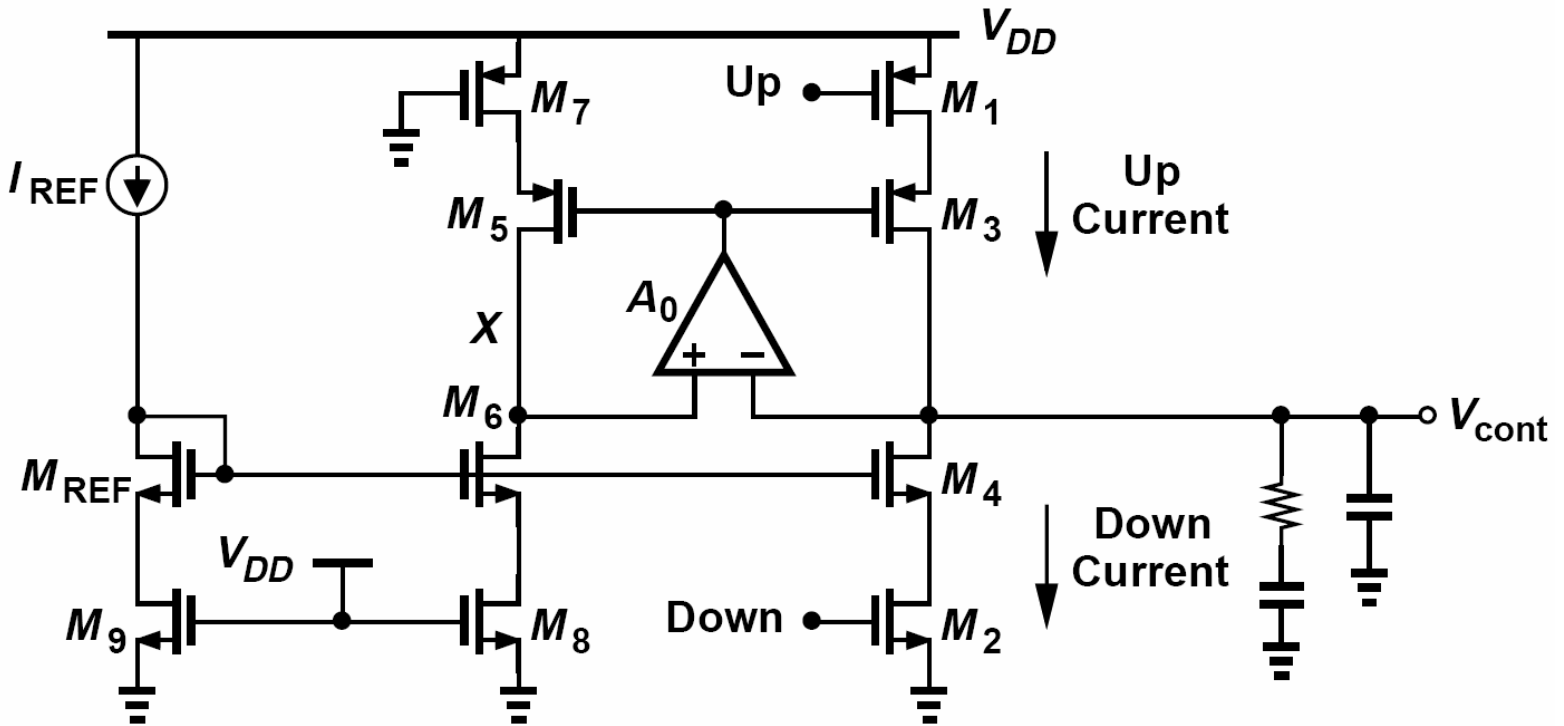**University of California, Los Angeles**

Approximating the pulses on the control line by impulses, determine the magnitude of the resulting sidebands at the output of the VCO.

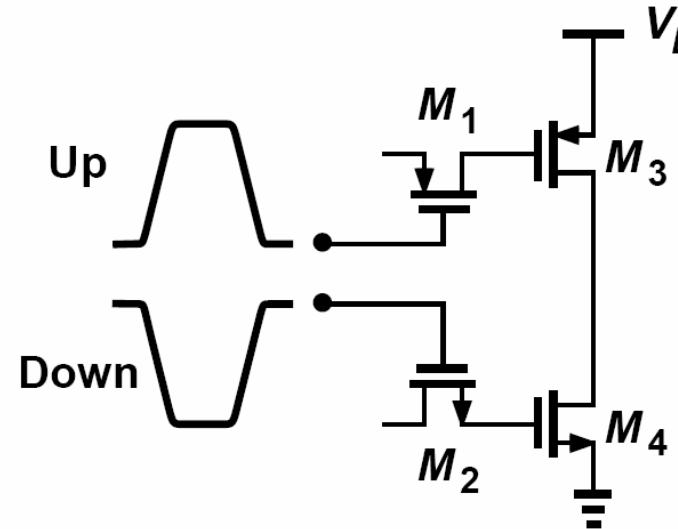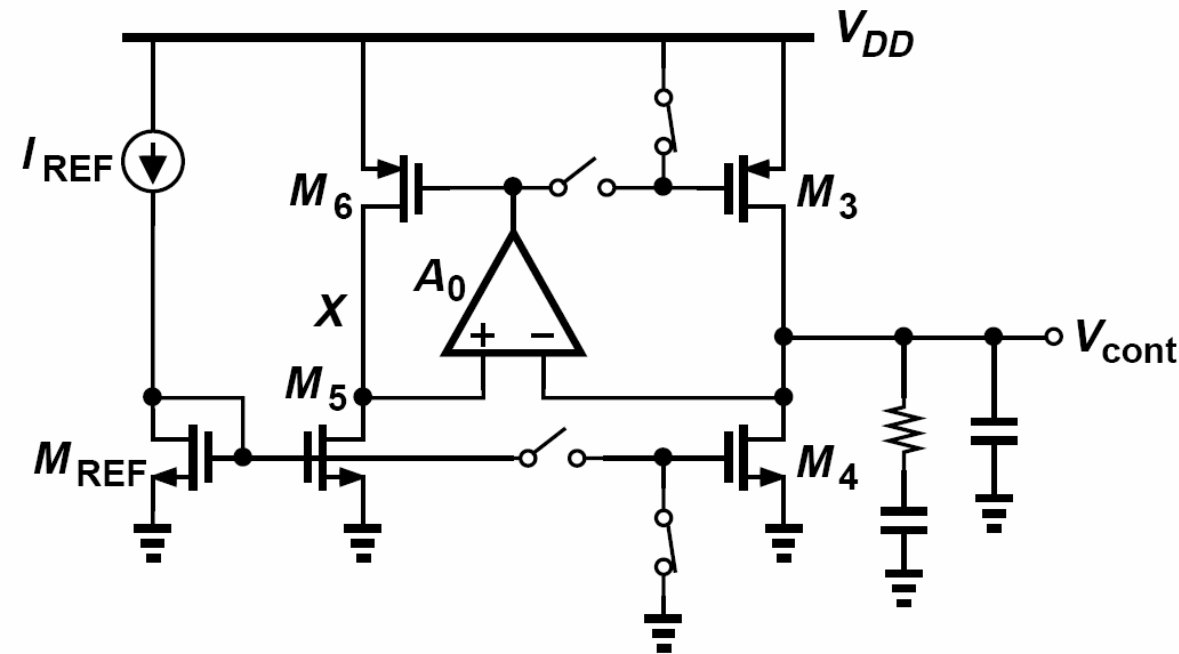$$\frac{A_{side}}{A_{carrier}} = \frac{1}{2\pi}\frac{\Delta TI_p}{C_2}T_{res}K_{VCO}$$

Sidebands at $f_c \pm n\, f_{in}$ are scaled down by a factor of n.

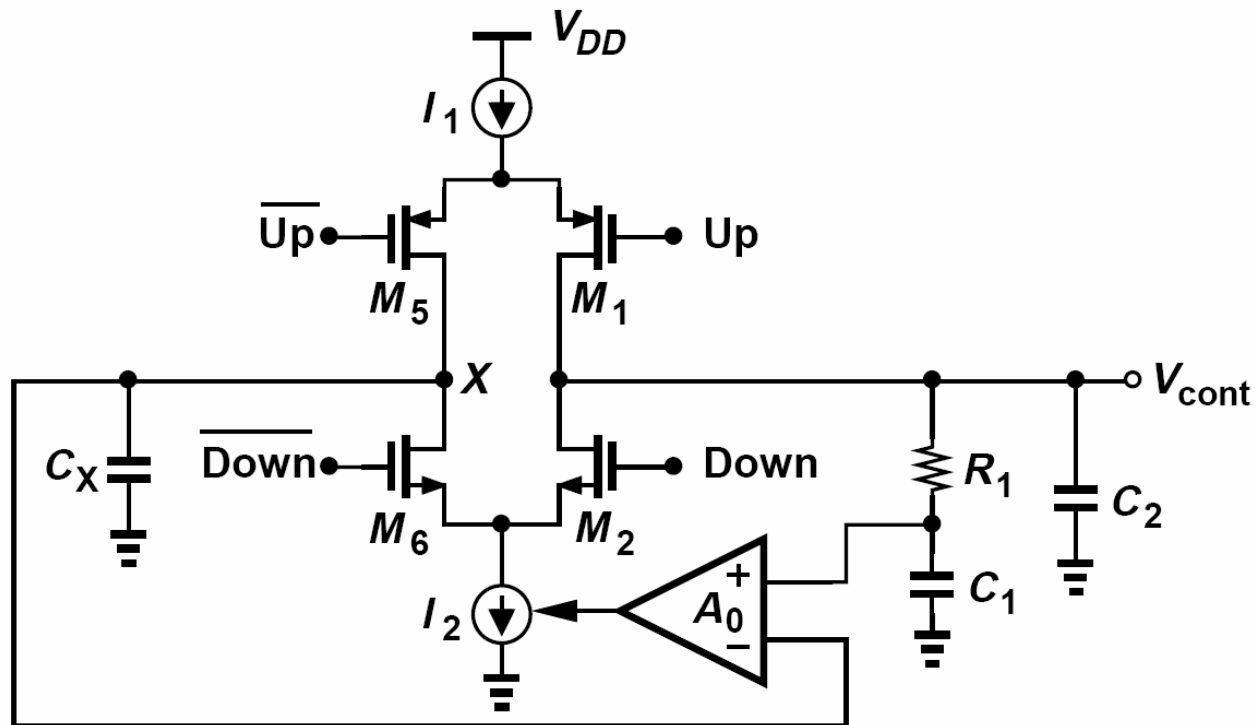## Circuit Techniques to Deal with Channel Length Modulation: Use of a Servo Loop

> ➤ A_0 need not provide a fast response
> ➤ Performance limited by random mismatches between NMOS current sources and between PMOS current sources.
> ➤ Op amp must operate with a nearly rail-to-rail input common-mode range.

Gate Switching

- ➢ **Voltage headroom saved**
- ➢ **But exacerbates the problem of Up and Down arrival mismatch.**
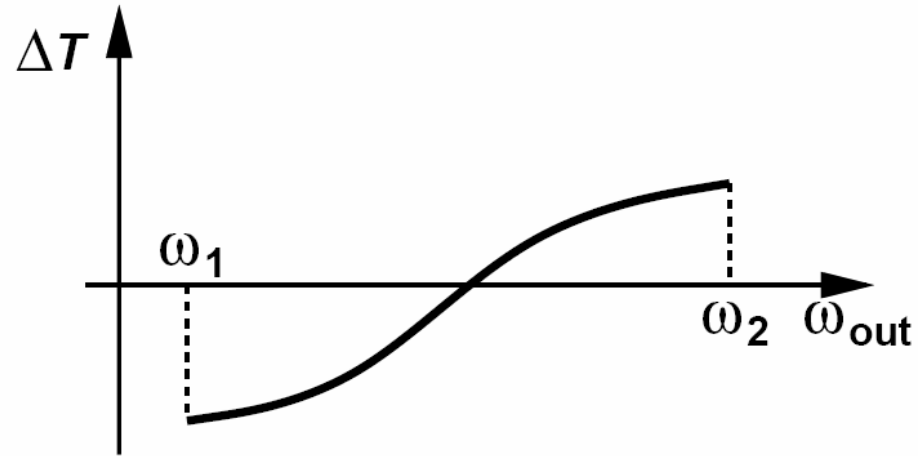- ➢ **Op amp must operate with a wide input voltage range.**

➢ **The accuracy of the circuit is ultimately limited by the charge injection and clock feedthrough mismatch between M_1 and M_5 and between M_2 and M_6**

The phase offset of a CPPLL varies with the output frequency. Explain why.
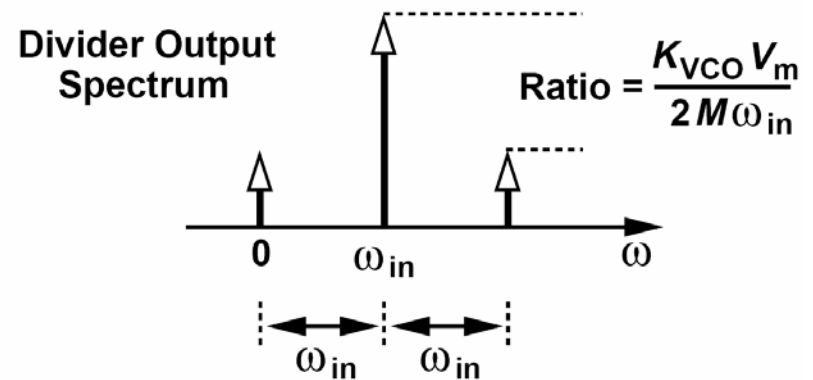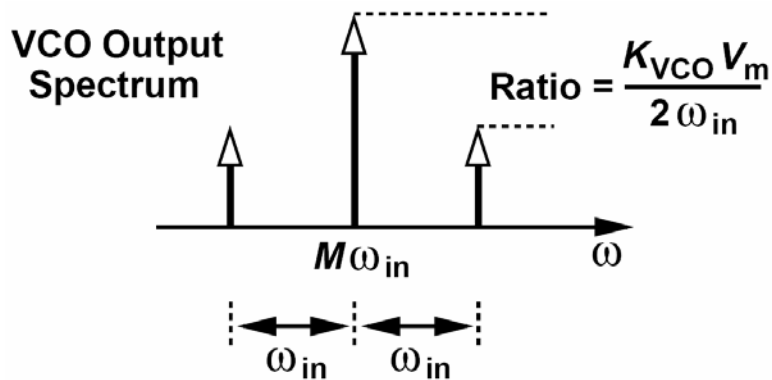
Solution:

Example of Divider Response to FM Sidebands

The control voltage of a VCO experiences a small sinusoidal ripple of amplitude V_m at a frequency equal to ω_{in}. Plot the output spectra of the VCO and the divider.

$$
\begin{aligned}
V_F(t) &= V_0 \cos\left[\frac{1}{M}\left(M\omega_{in}t + K_{VCO}\int V_m \sin\omega_{in}t\,dt\right)\right] \\
&\approx V_0 \cos\omega_{in}t - \frac{K_{VCO}V_m}{2M\omega_{in}}V_0\cos(\omega_{in}+\omega_{in})t + \frac{K_{VCO}V_m}{2M\omega_{in}}V_0\cos(\omega_{in}-\omega_{in})t.
\end{aligned}
$$

VCO Output Spectrum

$\text{Ratio} = \dfrac{K_{VCO}V_m}{2\omega_{in}}$

$M\omega_{in}$ ω

ω_{in} ω_{in}

Divider Output Spectrum

$\text{Ratio} = \dfrac{K_{VCO}V_m}{2M\omega_{in}}$

0   ω_{in} ω

ω_{in} ω_{in}

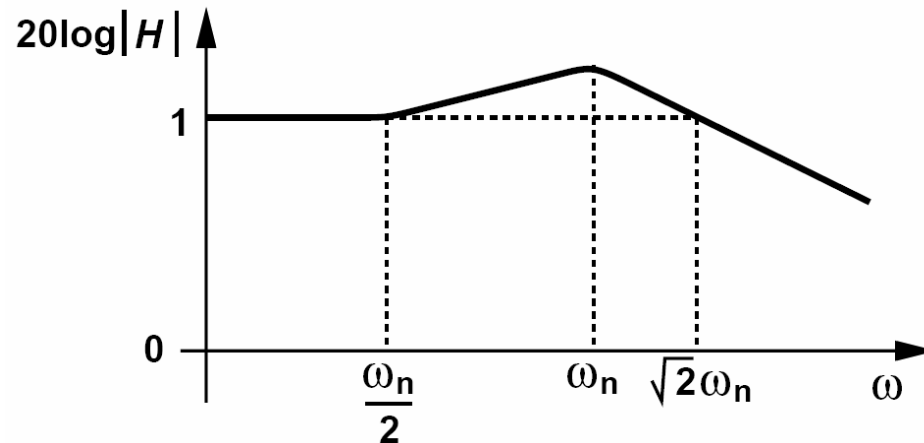**Plot the magnitude of the closed-loop transfer function as a function of ω if $\zeta = 1$**

> **Solution:**

$$H(s) = \frac{\dfrac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \dfrac{I_p}{2\pi}K_{VCO}R_1 s + \dfrac{I_p}{2\pi C_1}K_{VCO}}$$
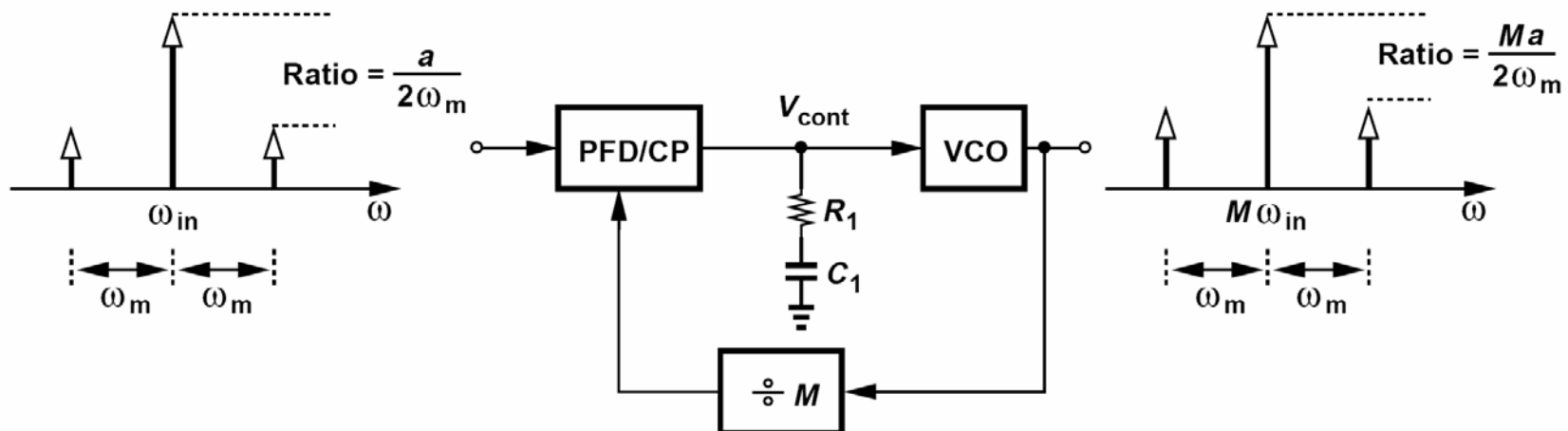
The input to a multiplying PLL is a sinusoid with two small "close-in" FM sidebands, i.e., the modulation frequency is relatively low. Determine the output spectrum of the PLL.

$$
\begin{aligned}
V_{in}(t) &= V_0 \cos(\omega_{in} t + a \int \cos \omega_m t\, dt) \\
&= V_0 \cos \left(\omega_{in} t + \frac{a}{\omega_m} \sin \omega_m t \right).
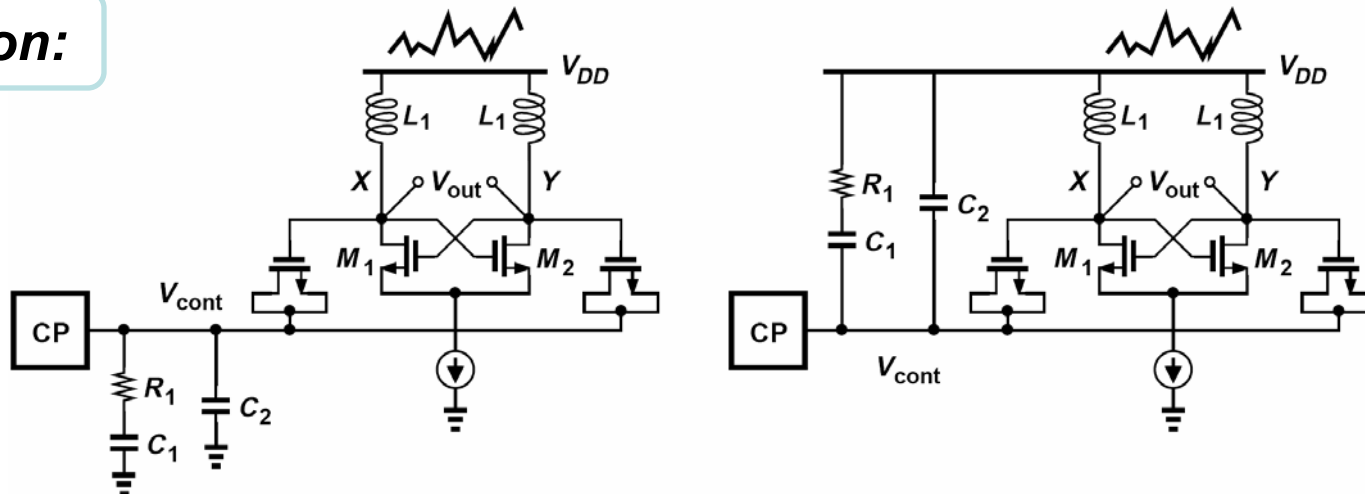\end{aligned}
$$

$$
\frac{\phi_{out}}{\phi_{in}}(s \approx 0) = M \qquad V_{out}(t) = V_1 \cos \left(M \omega_{in} t + \frac{Ma}{\omega_m} \sin \omega_m t \right)
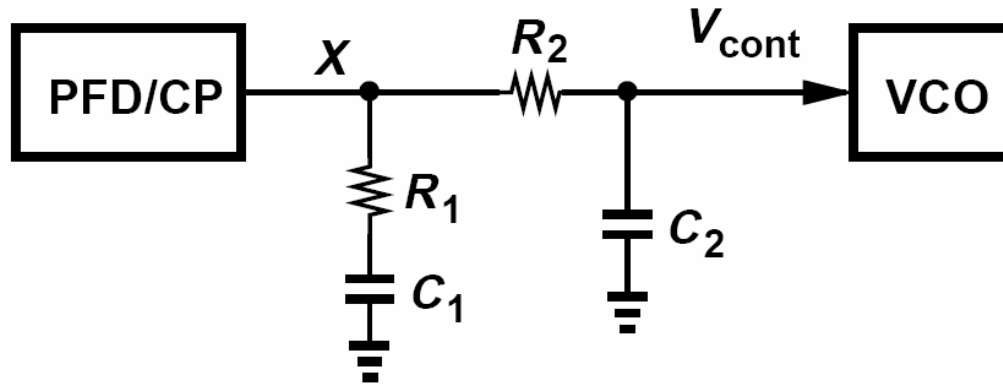$$

Ratio $= \dfrac{a}{2\omega_m}$

ω_{in}

ω

$\omega_m \quad \omega_m$

PFD/CP

V_{cont}

VCO

R_1

C_1

$\div M$

Ratio $= \dfrac{Ma}{2\omega_m}$

$M\omega_{in}$

ω

$\omega_m \quad \omega_m$

9

Consider the two filter/VCO topologies shown in figure below and explain which one is preferable with respect to supply noise.
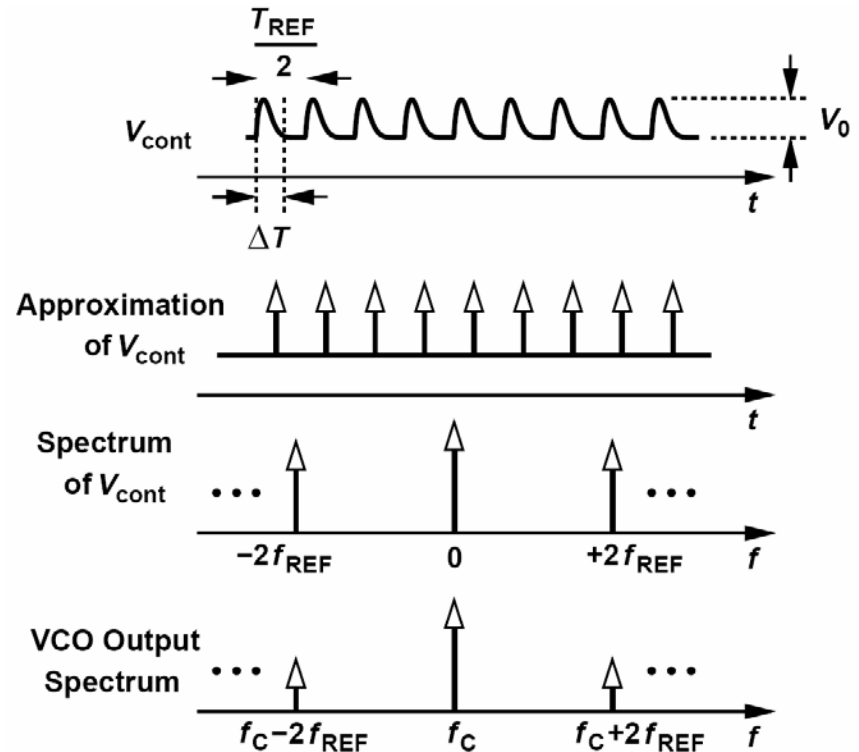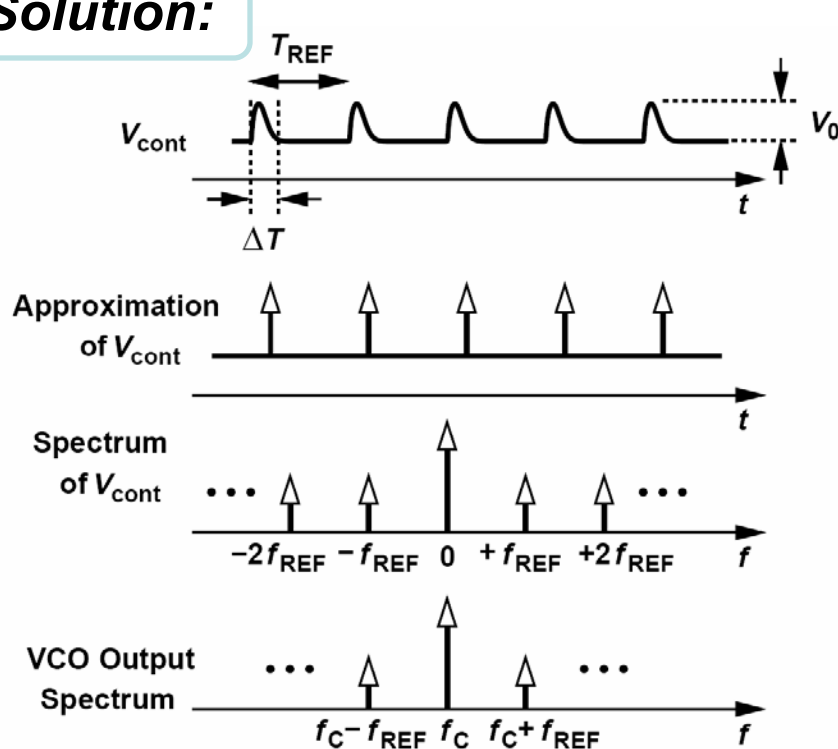
Solution:

Alternative Second-Order Loop Filter

$$\mathrm{PM} \approx \tan^{-1}(4\zeta^2) - \tan^{-1}\left(4\zeta^2 \frac{R_2 C_2}{R_1 C_1}\right)$$

- ➢ **The ripple at node *X* may be large but it is suppressed as it travels through the low-pass filter consisting of R_2 and C_2**
- ➢ **$(R_2 C_2)^{-1}$ must remain 5 to 10 times higher than ω_z so as to yield a reasonable phase margin.**
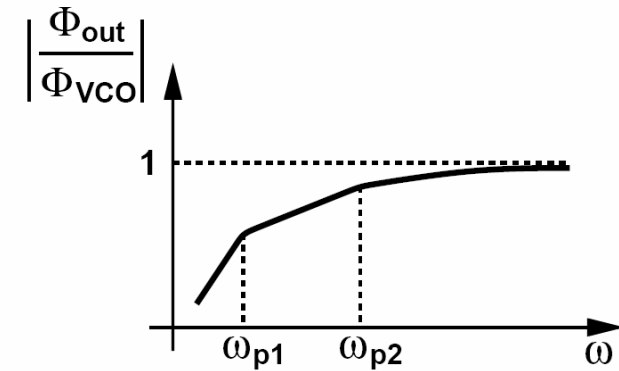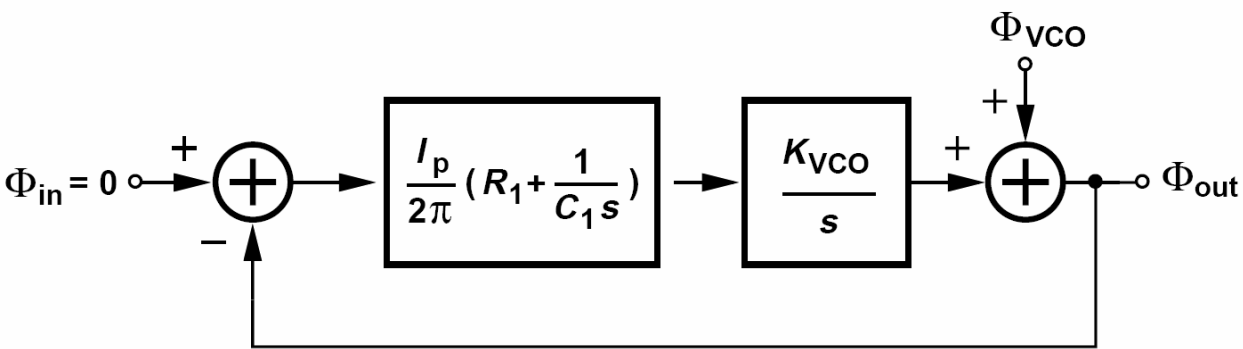
Puzzle

A PLL having a reference frequency of f_{REF} and a divide ratio of N exhibits reference sidebands at the output that are 60 dB below the carrier. If the reference frequency is doubled and the divide ratio is halved (so that the output frequency is unchanged), what happens to the reference sidebands? Assume the CP nonidealities are constant and the time during which the CP is on remains much shorter than $T_{REF} = 1/f_{REF}$.

Solution:
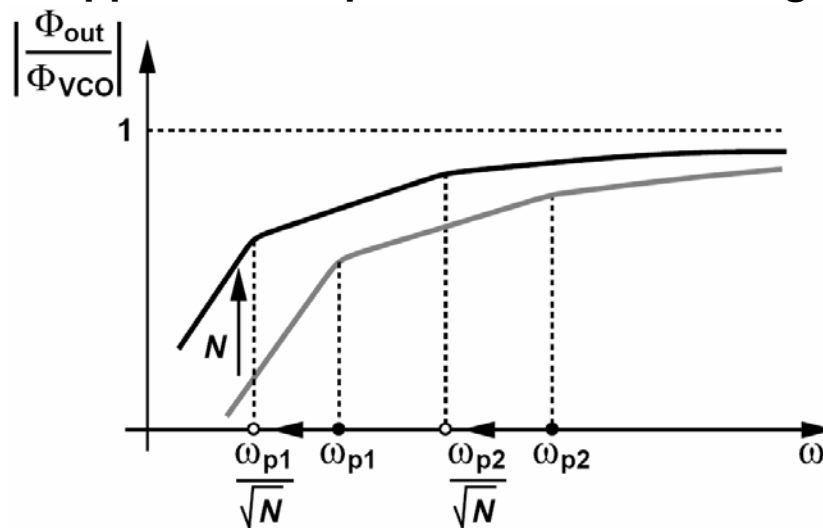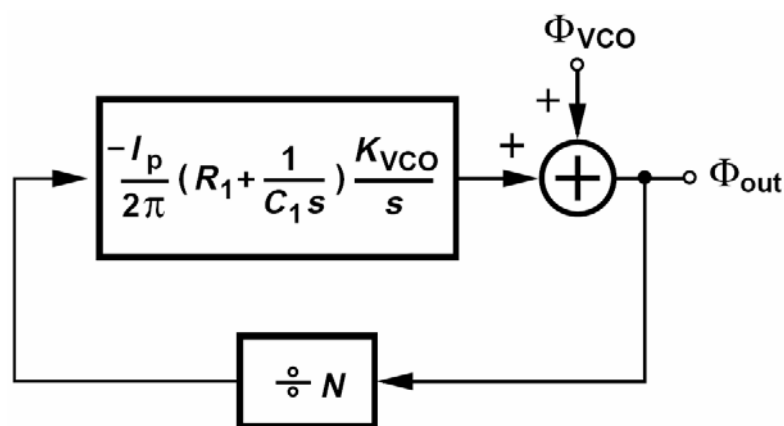
Phase Noise in PLLs: VCO Phase Noise

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$
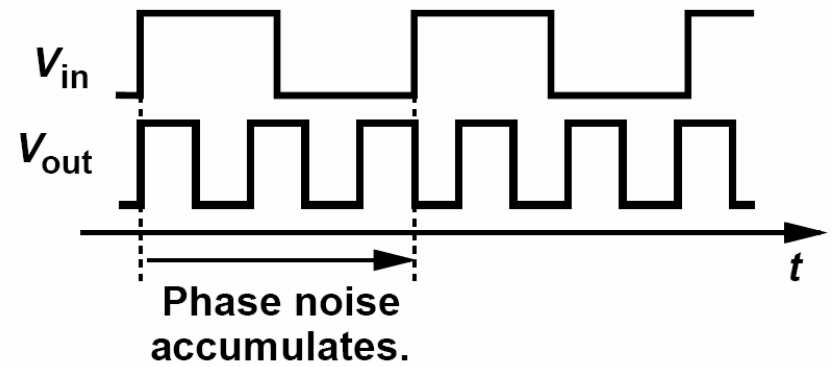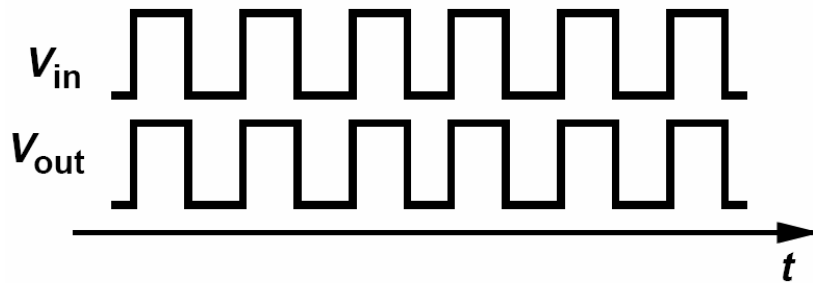
Another Example of VCO Phase Noise(I)

Consider a PLL with a feedback divide ratio of *N*. Compare the phase noise behavior of this case with that of a dividerless loop. Assume the output frequency is unchanged.

Redrawing the loop above as shown below on the left, we recognize that the feedback is now weaker by a factor of *N*. The transfer function still applies, but both ζ and ω_n are reduced by a factor of $\sqrt{N}$.

What happens to the magnitude plot? We make two observations. (1) To maintain the same transient behavior, ζ must be constant; e.g., the charge pump current must be scaled up by a factor of *N*. Thus, the poles given by previous equation simply decrease by factor of $\sqrt{N}$.
(2)For $s \to 0$, $\Phi_{out}/\Phi_{VCO} \approx s^2/\omega_n^2$, which is a factor of *N* higher than that of the dividerless loop. The magnitude of the transfer function thus appears as depicted below on the right.
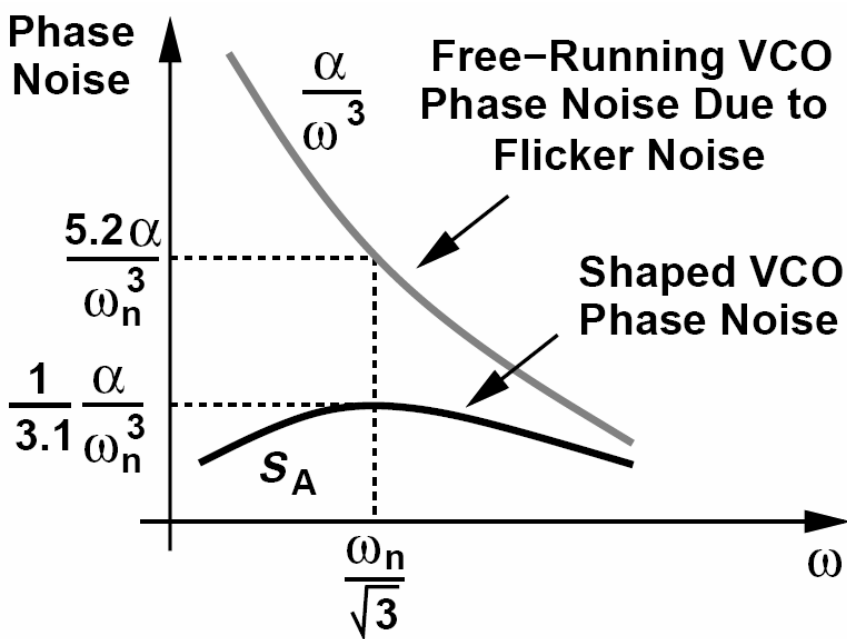
Time-Domain Perspective

Phase noise accumulates.

$$\overline{\phi_{out}^2} = \frac{\omega^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \omega_n^2 \omega^2} \left(\frac{\alpha}{\omega^3} + \frac{\beta}{\omega^2} \right)$$
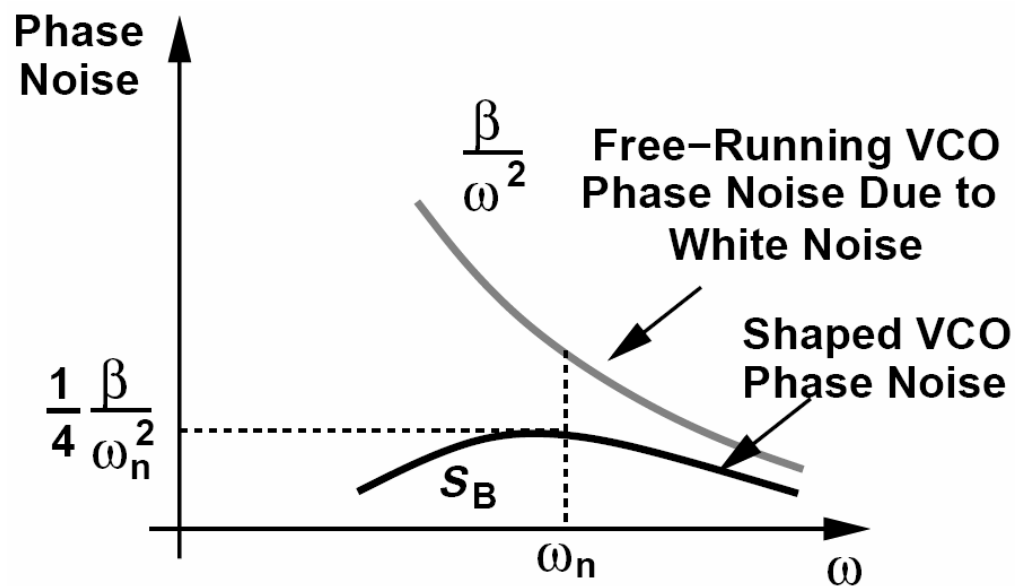
low offset frequencies

$$\overline{\phi_{out}^2}\Big|_{\text{small } \omega} \approx \frac{\alpha\omega}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \omega_n^2 \omega^2}$$
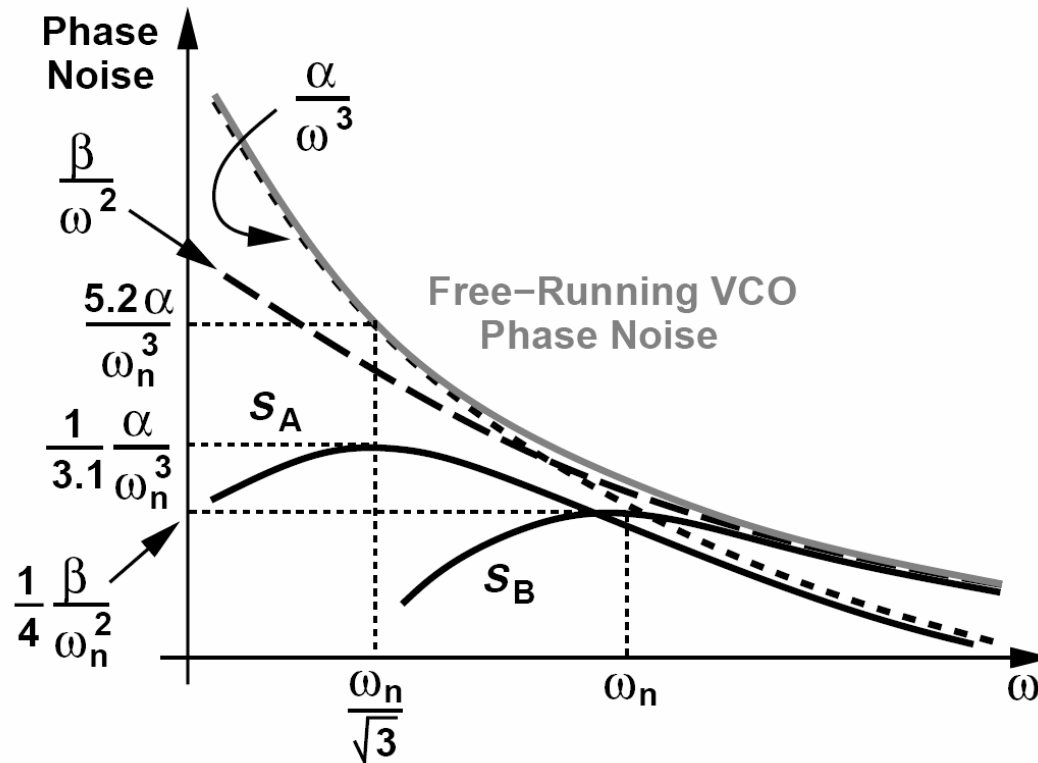
high offset frequencies

$$\overline{\phi_{out}^2}\Big|_{\text{large } \omega} = \frac{\beta\omega^2}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \omega_n^2 \omega^2}$$

Phase Noise

$\frac{\alpha}{\omega^3}$

Free−Running VCO Phase Noise Due to Flicker Noise

$\frac{5.2\alpha}{\omega_n^3}$

Shaped VCO Phase Noise

$\frac{1}{3.1}\frac{\alpha}{\omega_n^3}$

S_A

$\frac{\omega_n}{\sqrt{3}}$

ω

Phase Noise

$\frac{\beta}{\omega^2}$

Free−Running VCO Phase Noise Due to White Noise

Shaped VCO Phase Noise

$\frac{1}{4}\frac{\beta}{\omega_n^2}$
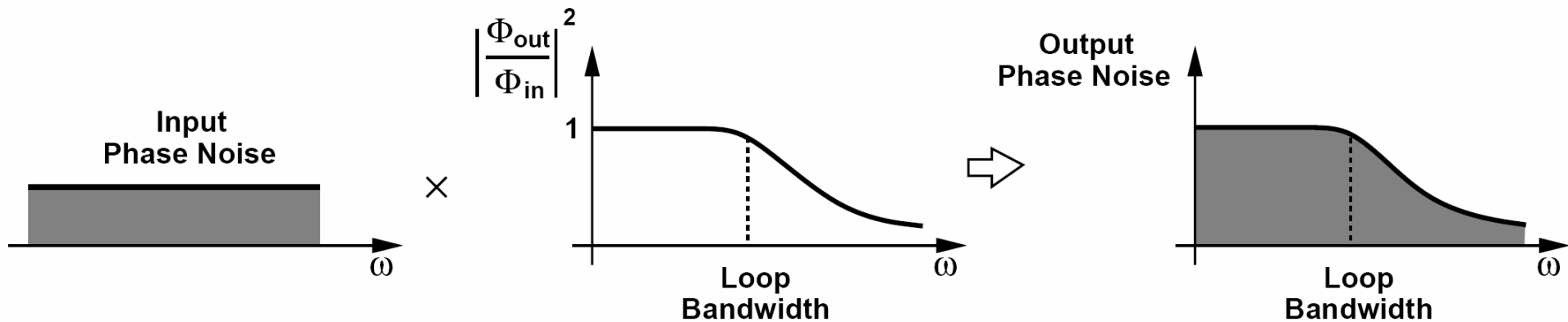
S_B

ω_n

ω

16

Shaped VCO Noise Summary

- ➤ **The overall PLL output phase noise is equal to the sum of S_A and S_B**
- ➤ **The actual shape depends on two factors:**
  - **(1) the intersection frequency of α/ω^3 and β/ω^2**
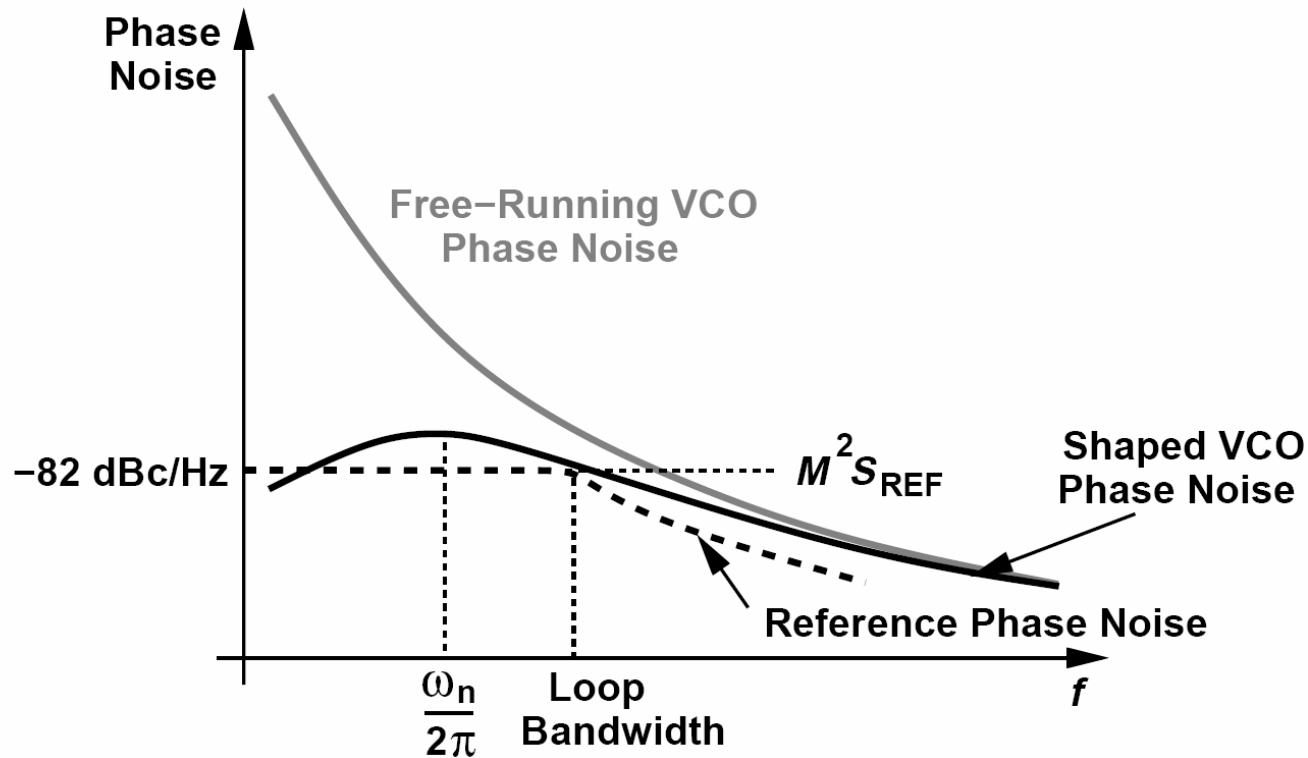 - **(2) the value of ω_n**

Reference Phase Noise: the Overall Behavior

Input Phase Noise

$\times$

$\left|\dfrac{\Phi_{out}}{\Phi_{in}}\right|^2$

1

Loop Bandwidth

ω

$\Rightarrow$

Output Phase Noise

Loop Bandwidth

ω

$$S_{out} = \frac{4\zeta^2\omega_n^2\omega^2 + \omega_n^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2} S_{REF}$$
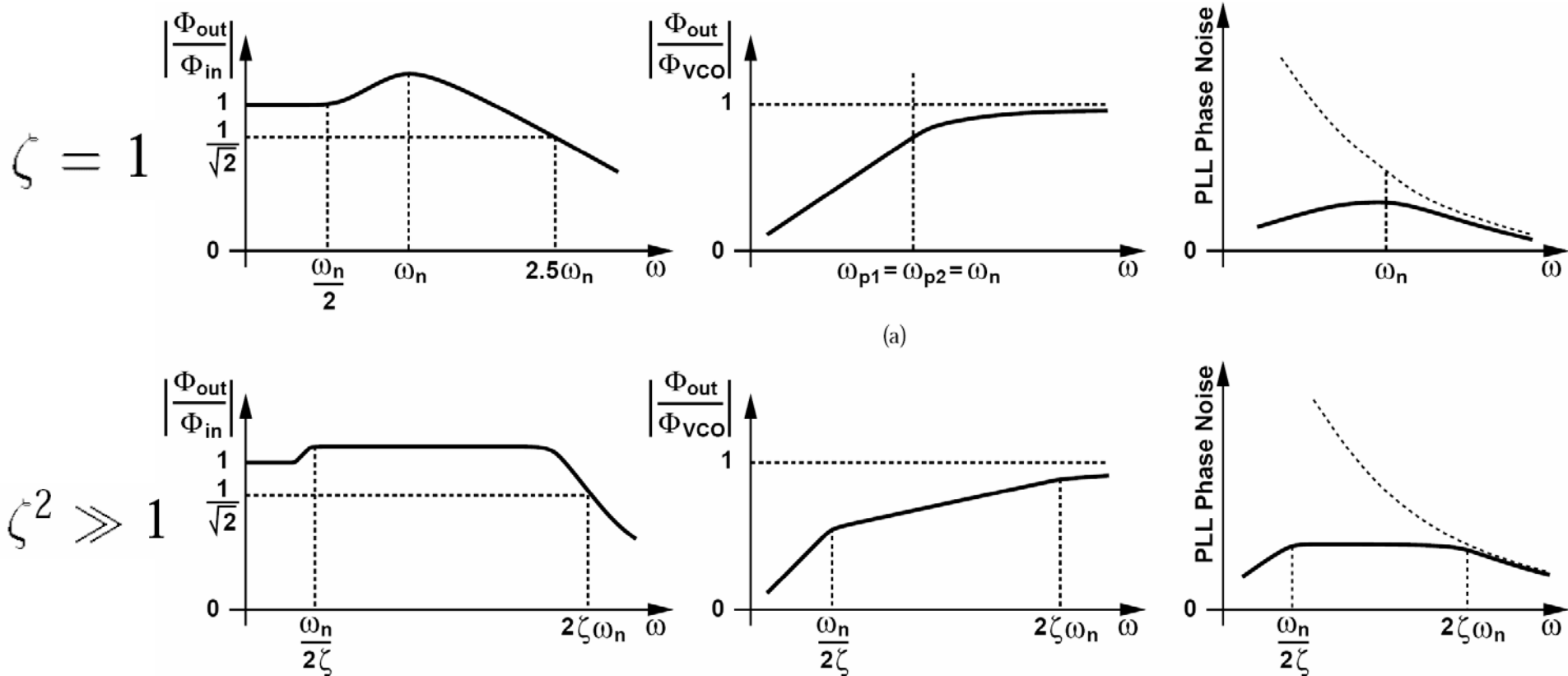
➢ **Crystal oscillators providing the reference typically display a *flat* phase noise profile beyond an offset of a few kilohertz**

> ➤ **PLLs performing frequency multiplication "amplify" the low-frequency reference phase noise proportionally.**
> ➤ **The total phase noise at the output increases with the loop bandwidth**

(a)

$$\frac{(2\zeta\omega_n\omega_{-3dB})^2 + \omega_n^4}{(\omega_{-3dB}^2 - \omega_n^2)^2 + (2\zeta\omega_n\omega_{-3dB})^2} = \frac{1}{2}$$

20