Introduction to PLLs

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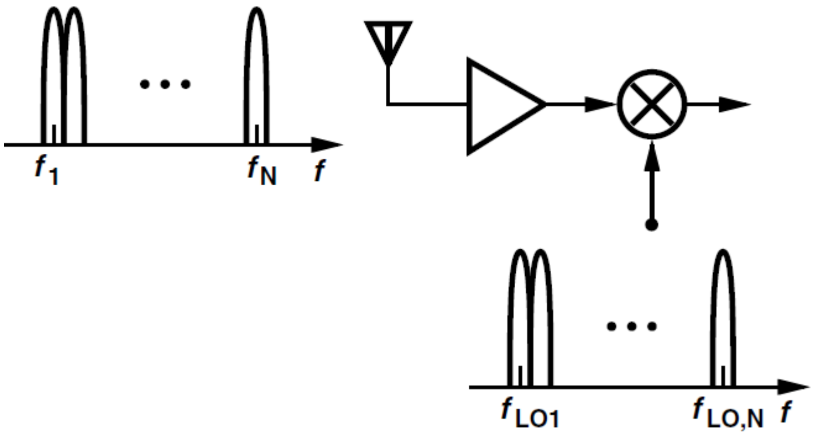
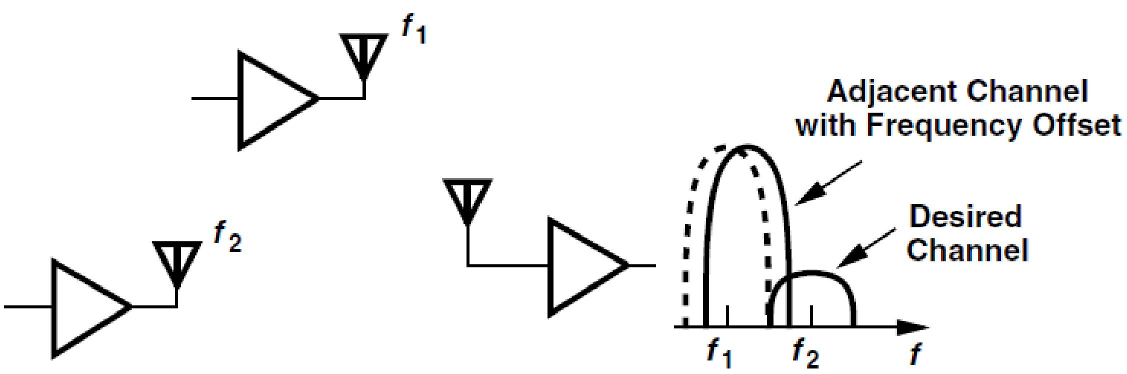
Outline

- Need for Frequency Synthesis
- Phase Detector
- Type I and II PLLs
- PFD/Charge Pump Nonidealities
- PLL Design Procedure

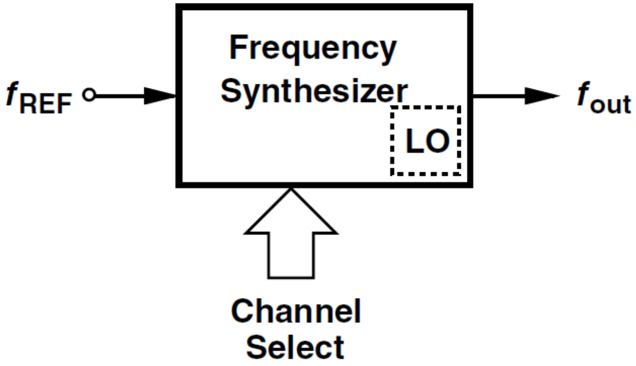
The Need for RF Synthesis



- What happens if the LO freq is not exactly what we want?

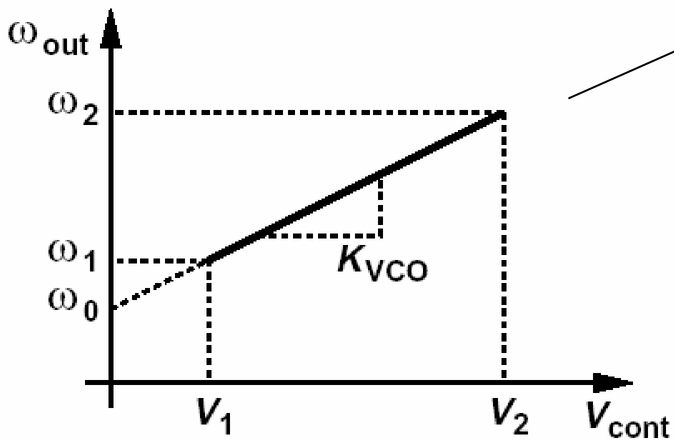


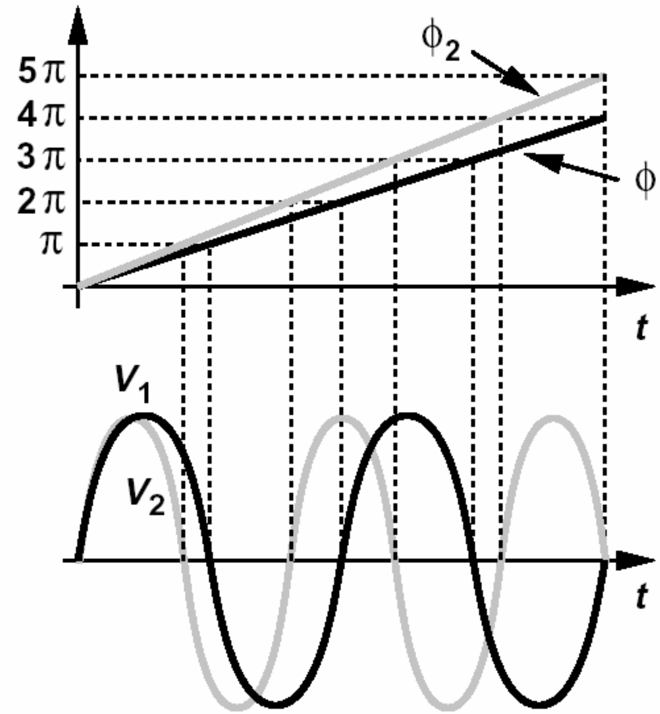
- Need a freq. synthesizer:



Mathematical Model of VCO

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$





$$V_1(t) = V_m \sin[\phi_1(t)]$$

$$V_2(t) = V_m \sin[\phi_2(t)]$$

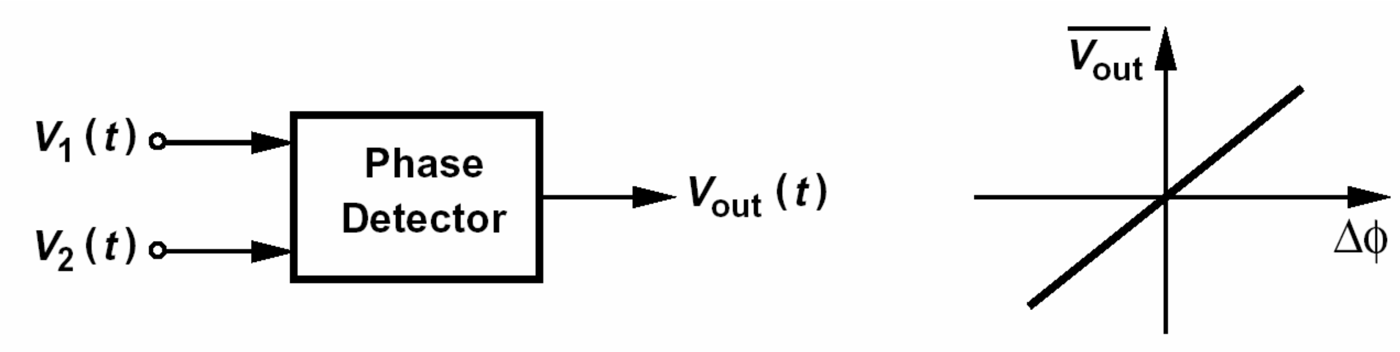
$$\phi_1(t) = \omega_1 t, \phi_2(t) = \omega_2 t$$

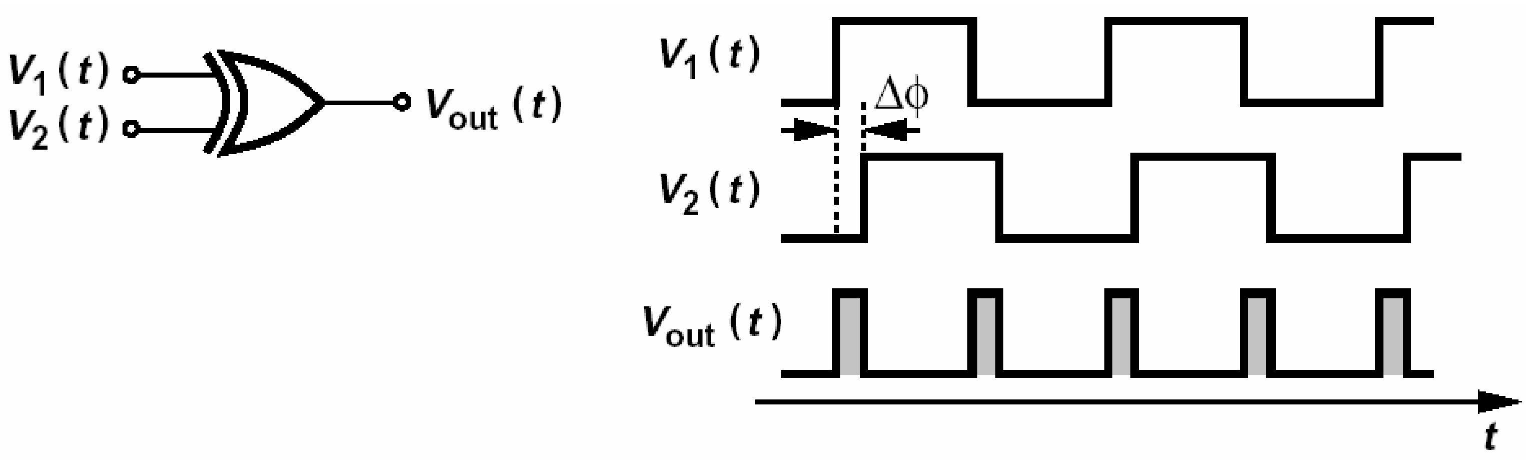
$$\Rightarrow \quad \omega = \frac{d\phi}{dt}$$

$$V_{out}(t) = V_m \cos(\omega_0 t + K_{VCO} \int V_{cont} dt)$$

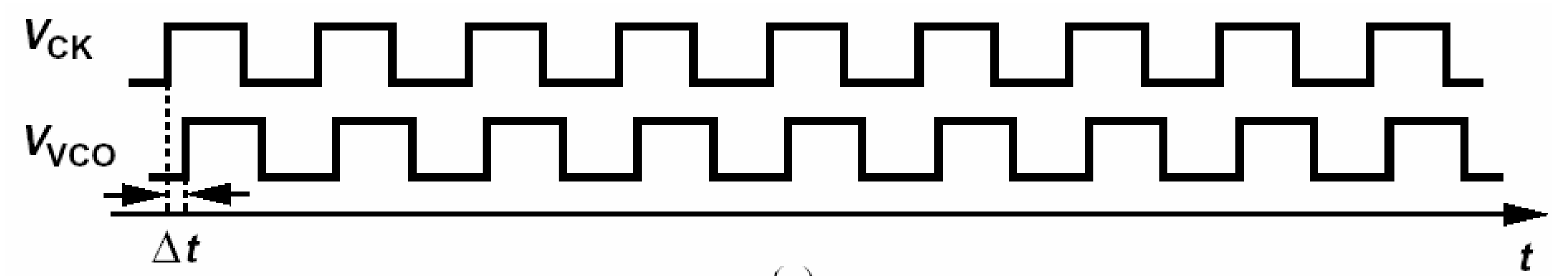
- **What happens if a small sine appears on Vcont?**

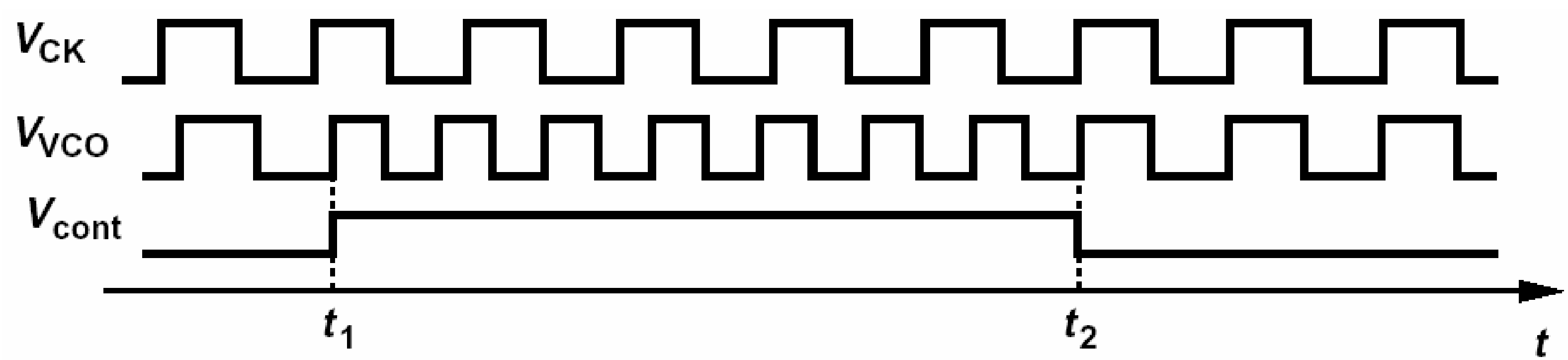
Phase Detector

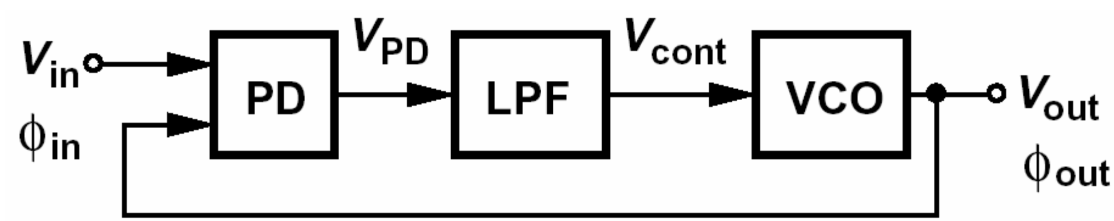




Problem of Phase Alignment

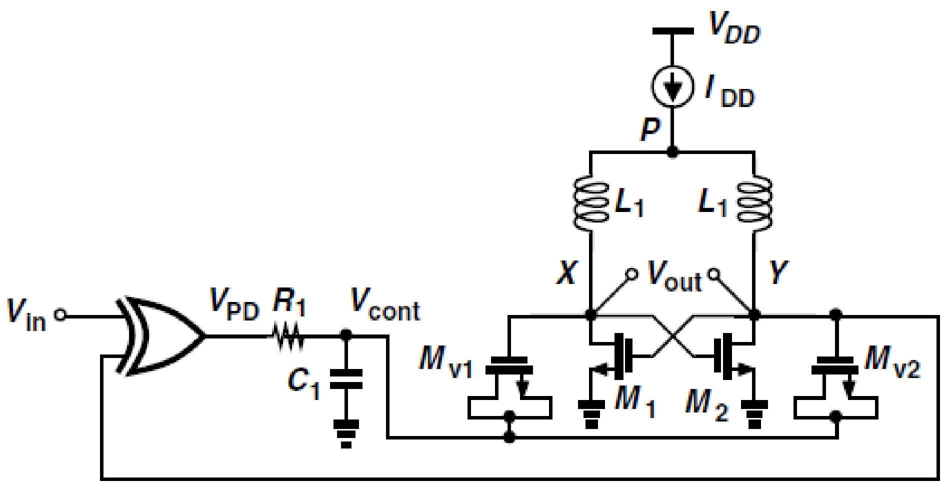


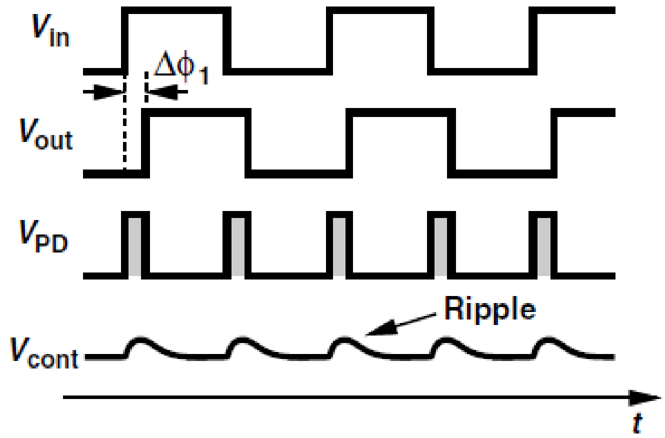


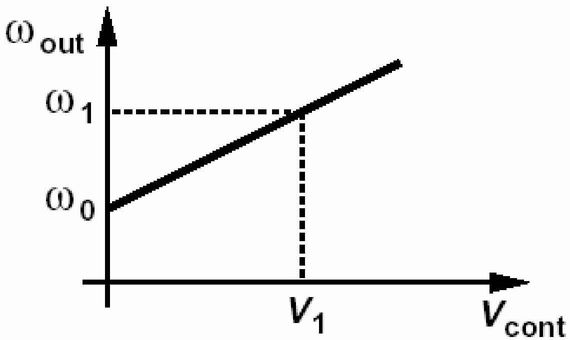


- **Loop is locked if phase difference is constant.**

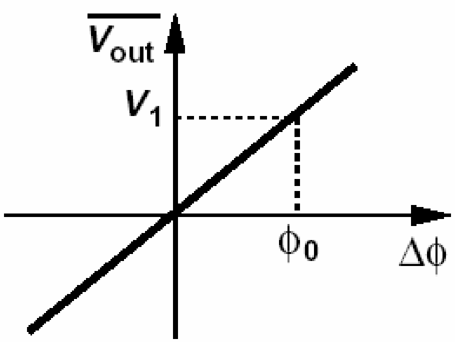
Example





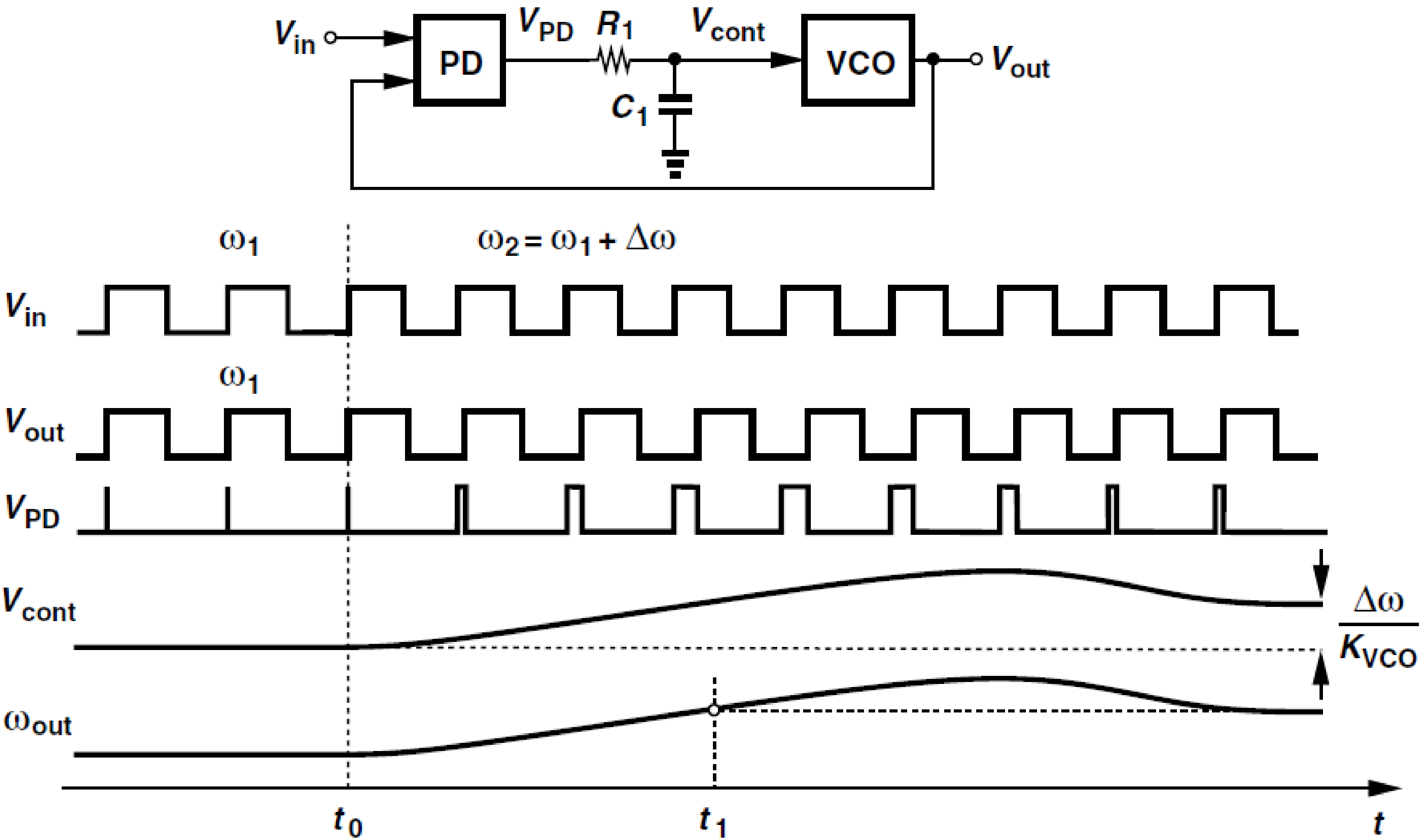


- **Ripple modulates VCO, producing sidebands.**

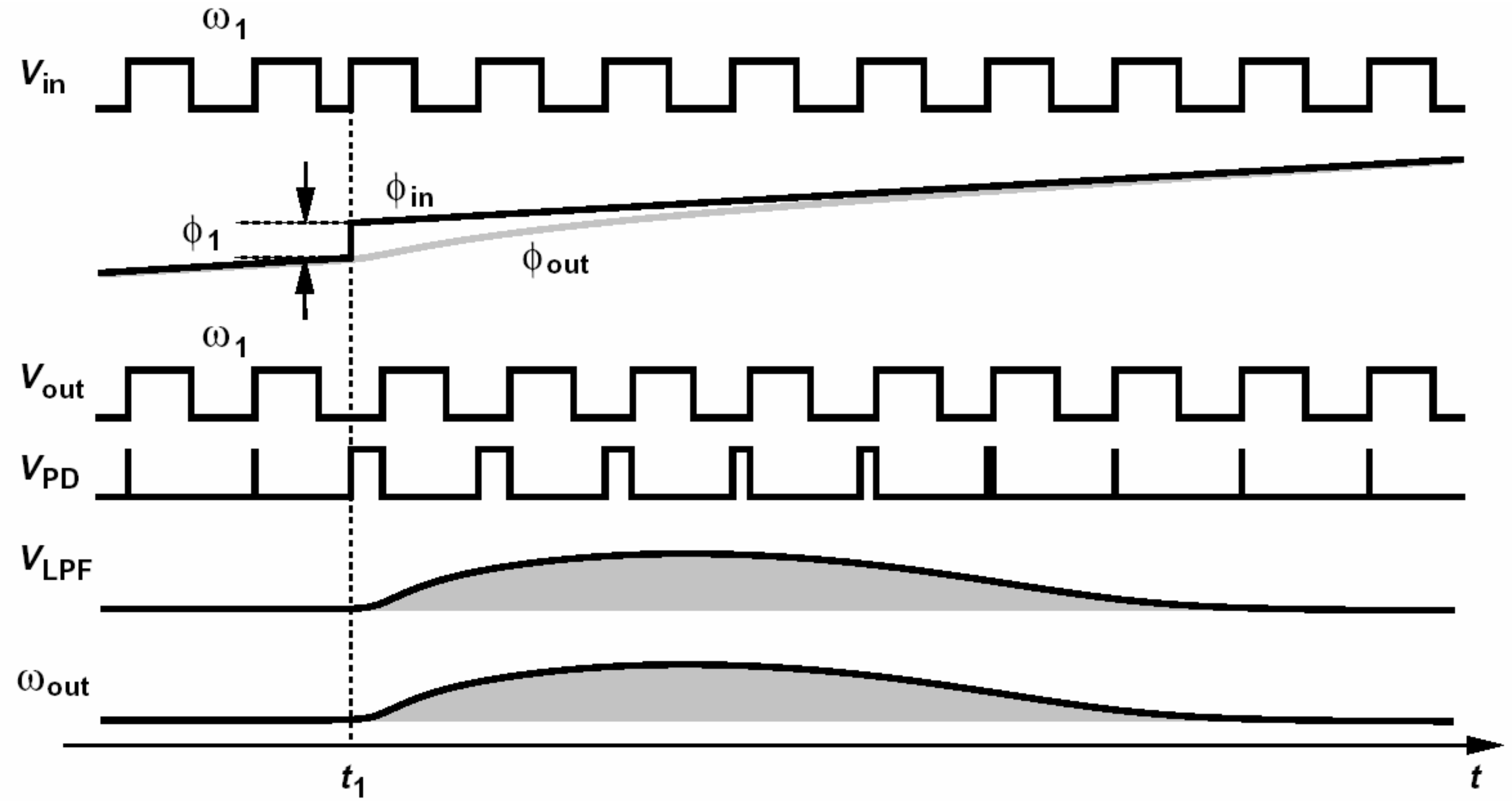


$$\phi_0 = \frac{\omega_1 - \omega_0}{K_{PD} K_{VCO}}$$

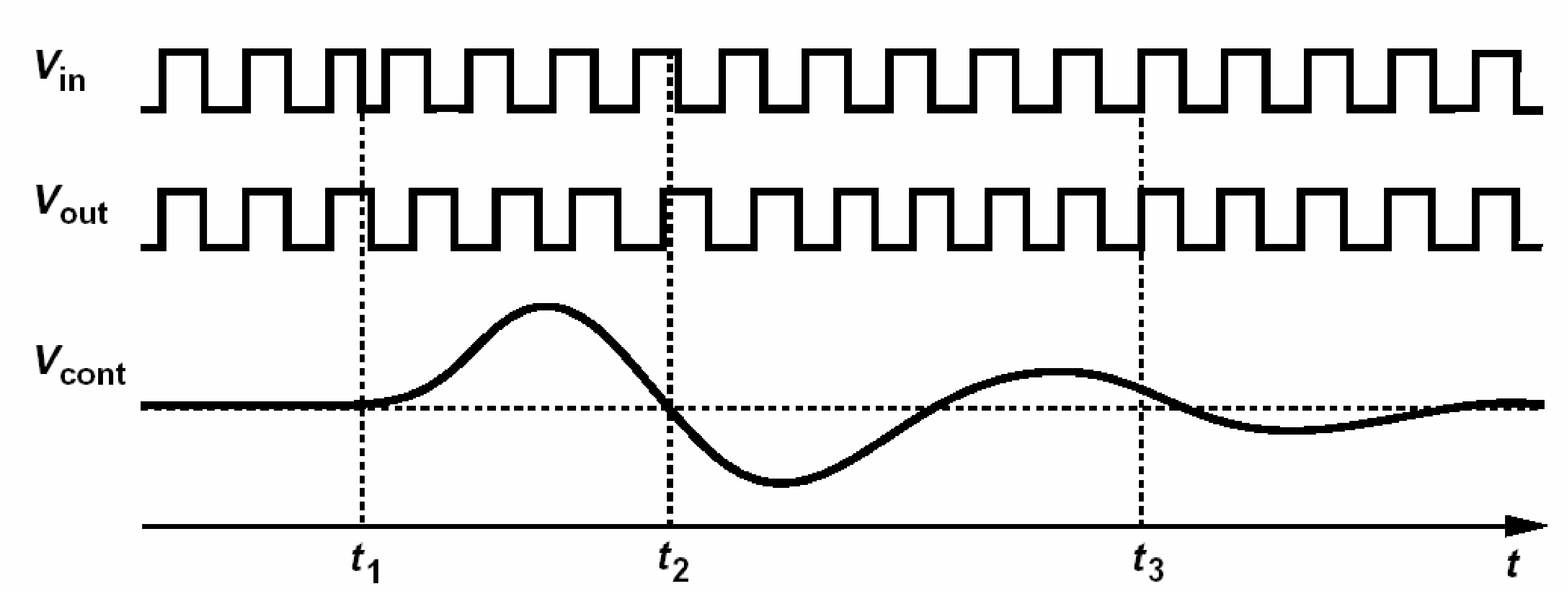
Response to Frequency Step



Response to Phase Step

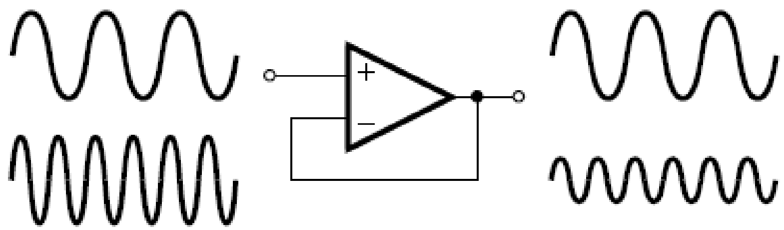


Phase and Frequency Settling

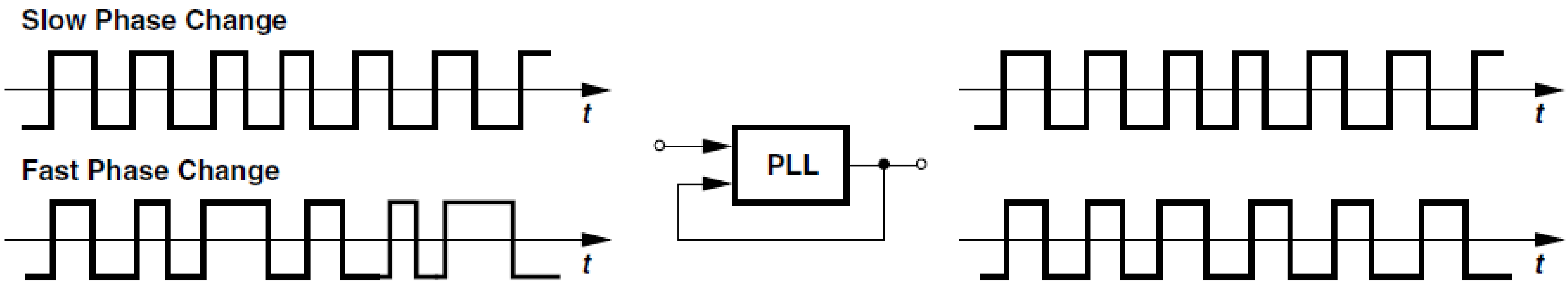


PLL Dynamics

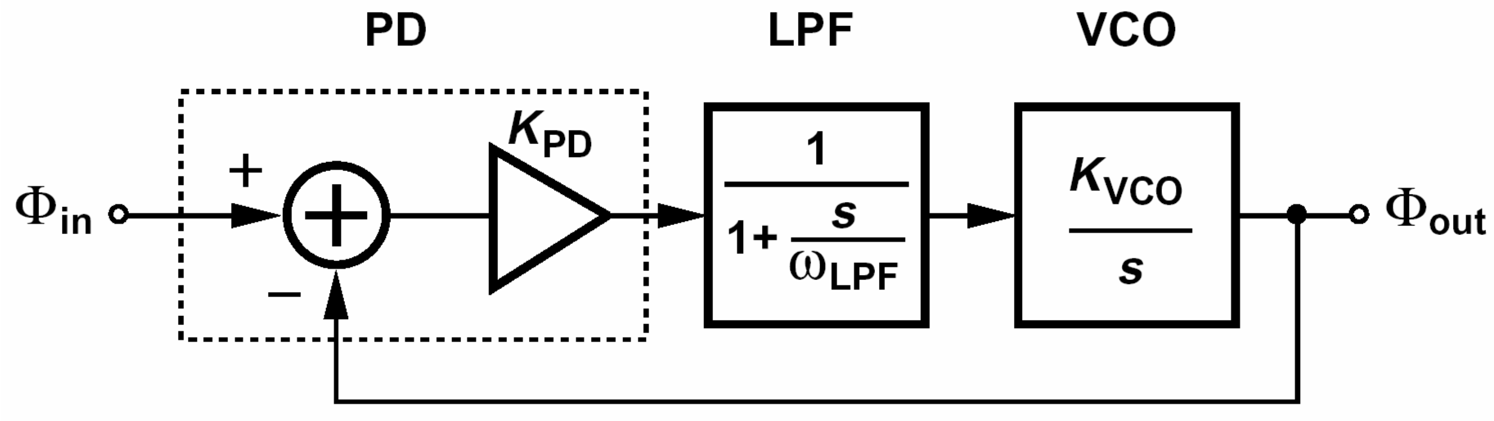
- How do we compute the time or frequency response of a PLL?



(a)



Type I PLL



$$H(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

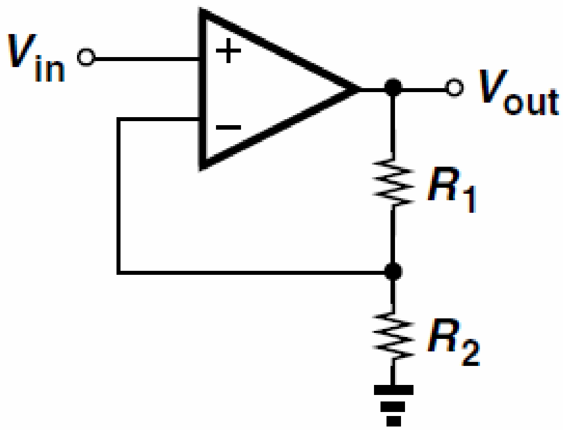
$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.$$

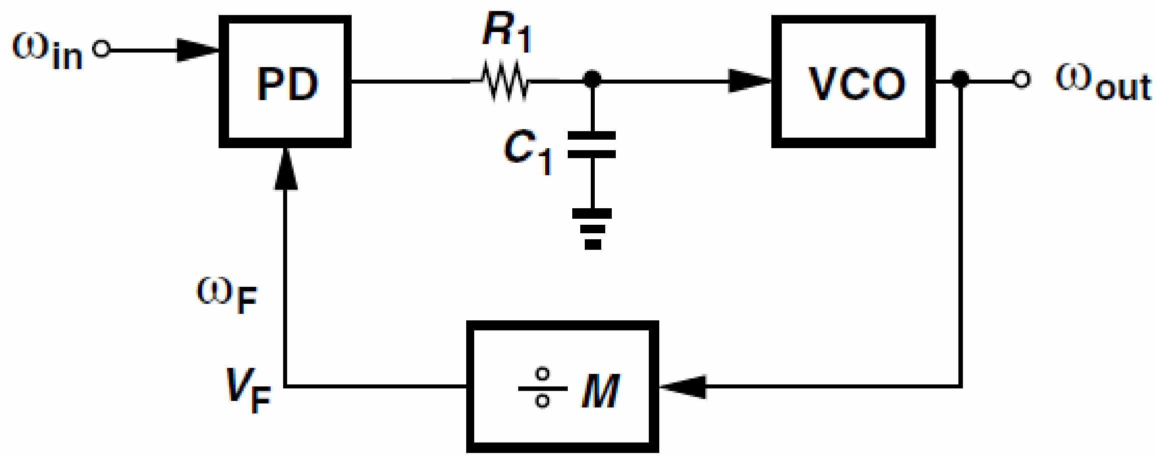
- **Trade-offs among stability, ripple, and phase offset**
- **Limited capture range**
- **Why is this better than a piece of wire?**

Frequency Multiplication

Voltage Type



Phase or Freq Type



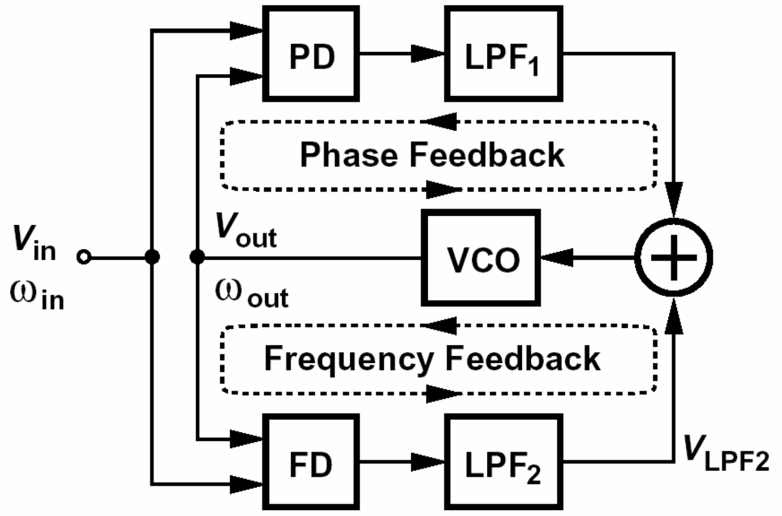
- **How do these change for this type of loop:**

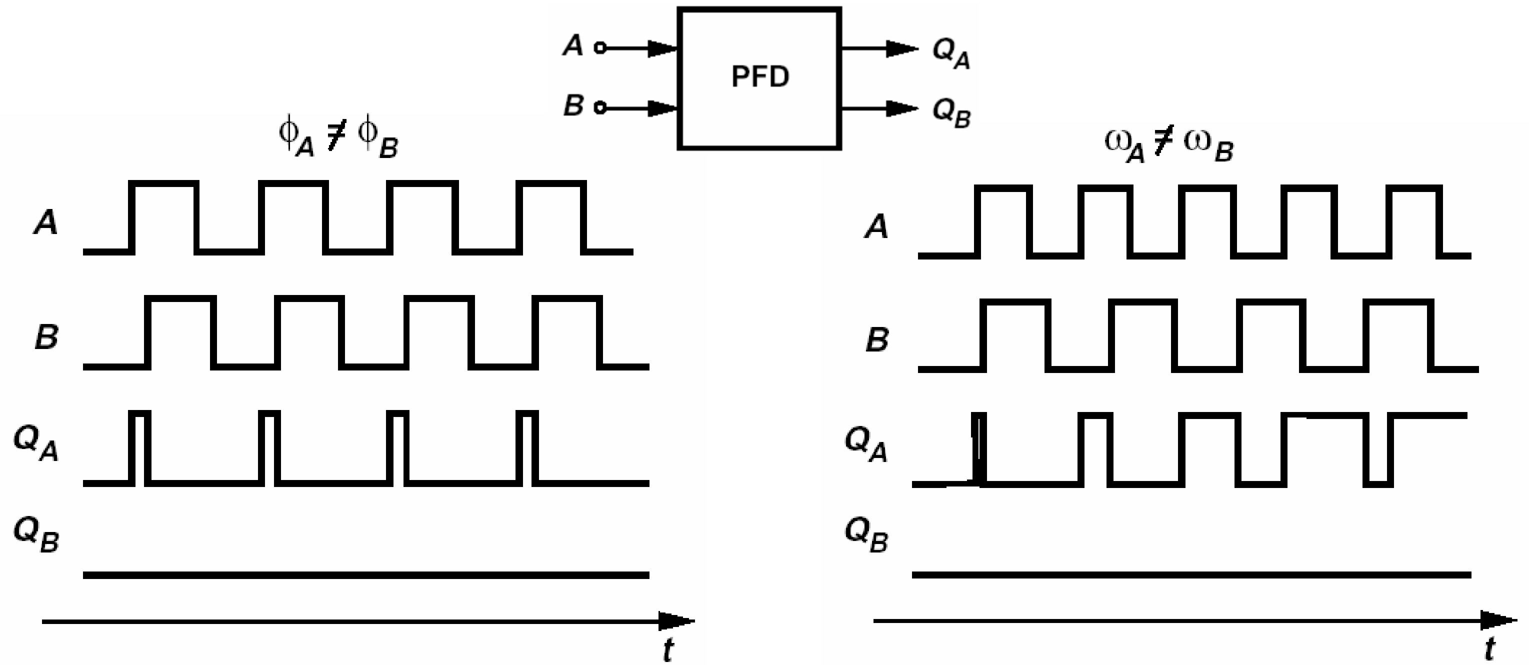
$$H(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}}$$

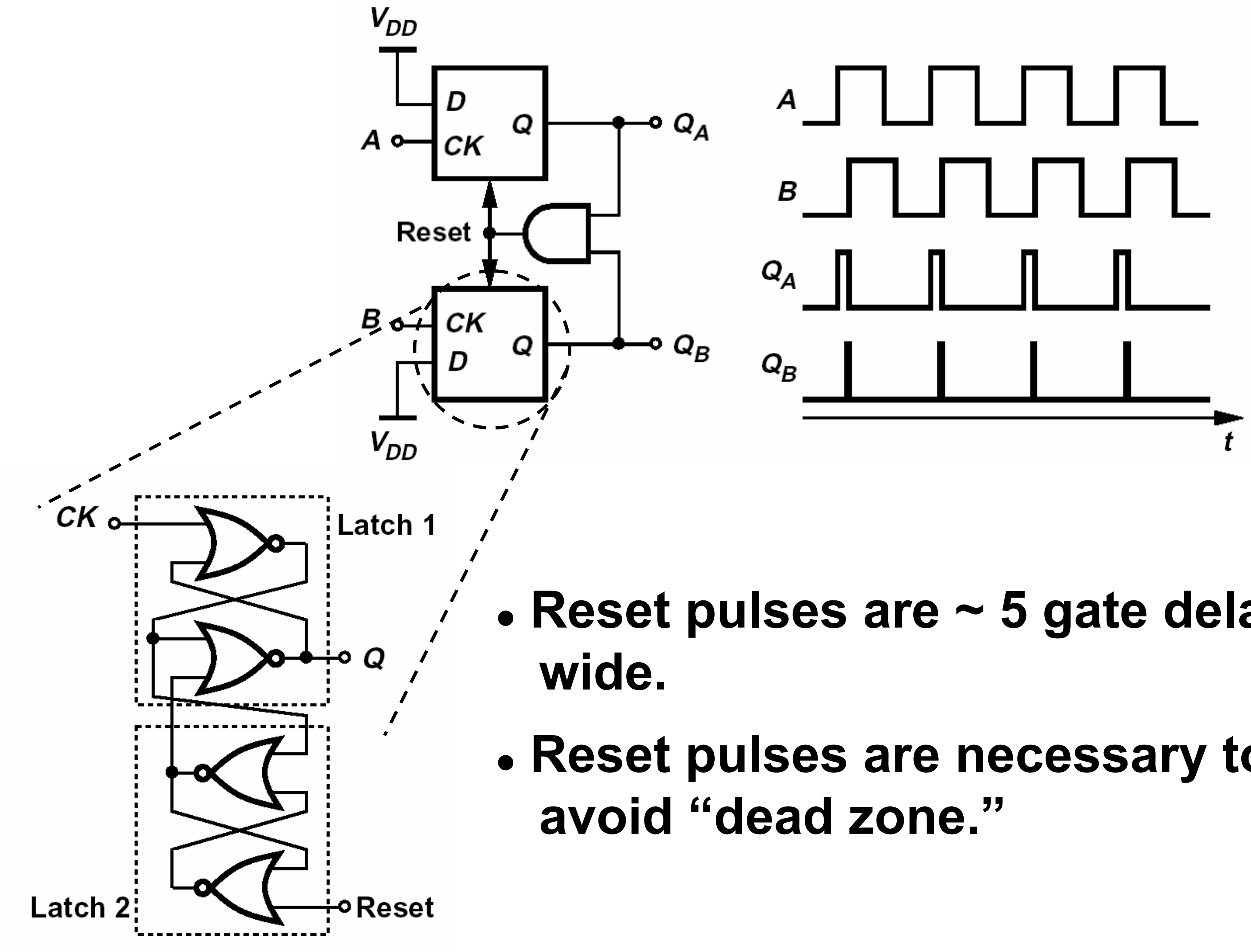
$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.$$

Aided Acquisition



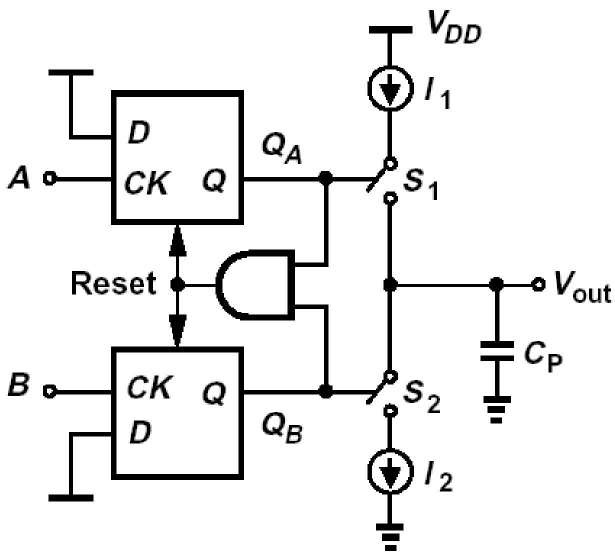


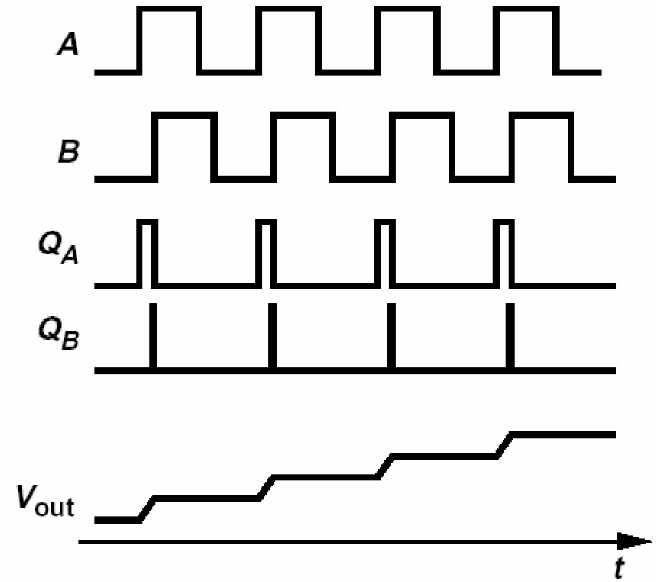
PFD Implementation

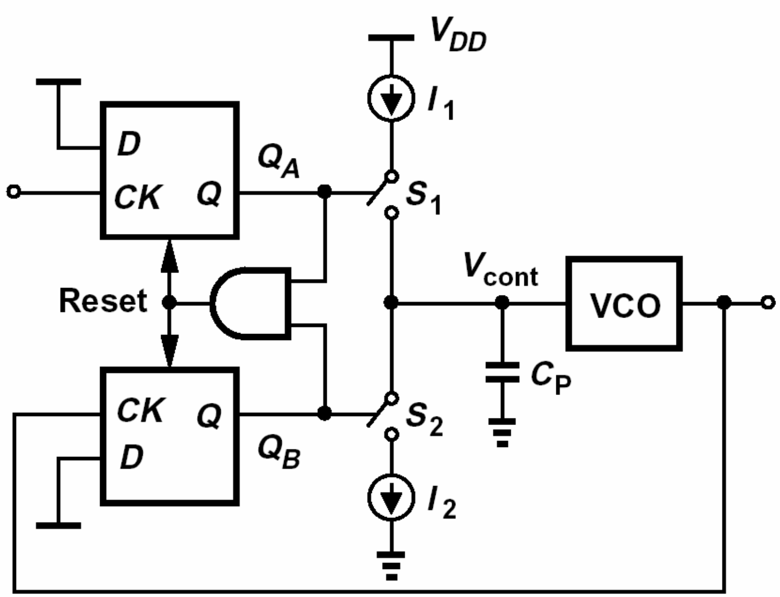


- **Reset pulses are ~ 5 gate delays wide.**
- **Reset pulses are necessary to avoid "dead zone."**

PFD and Charge Pump

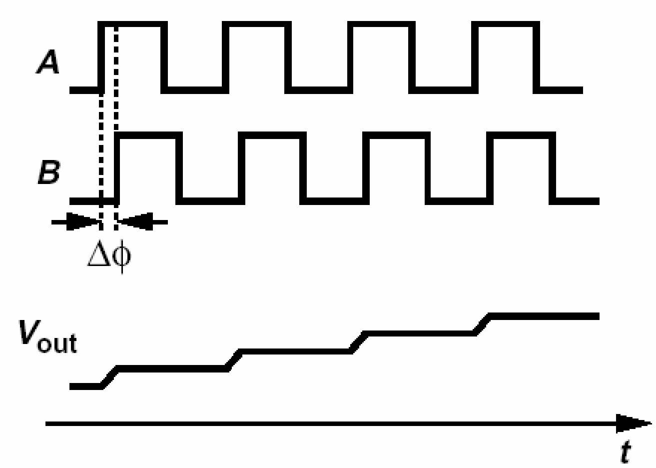


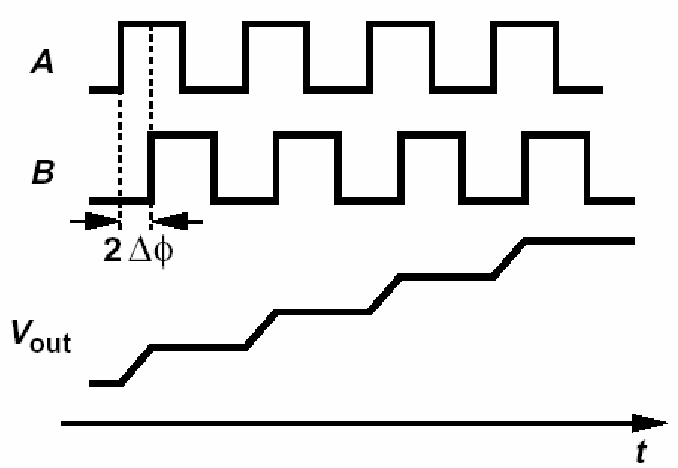


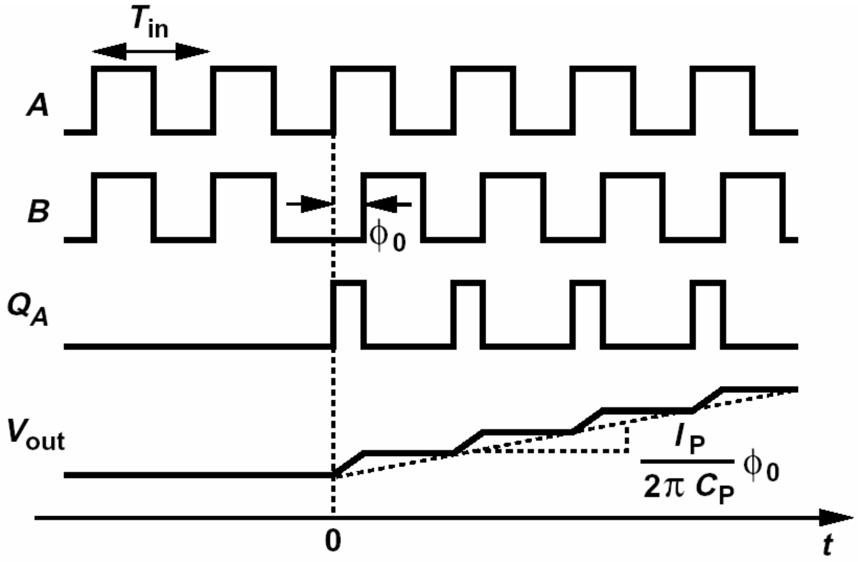


- Infinite gain yields zero phase offset.
- Q_A and Q_B are called "Up" and "Down" pulses, respectively.

PFD/CP/Capacitor Behavior

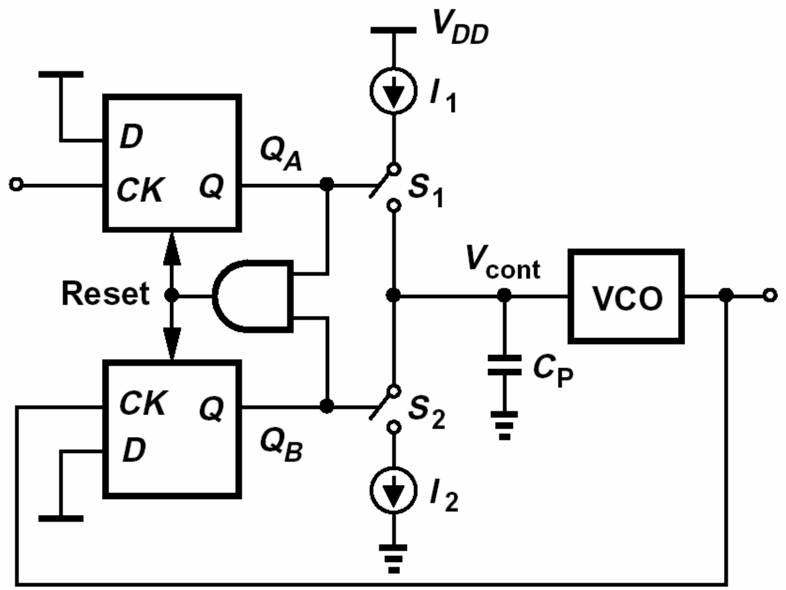


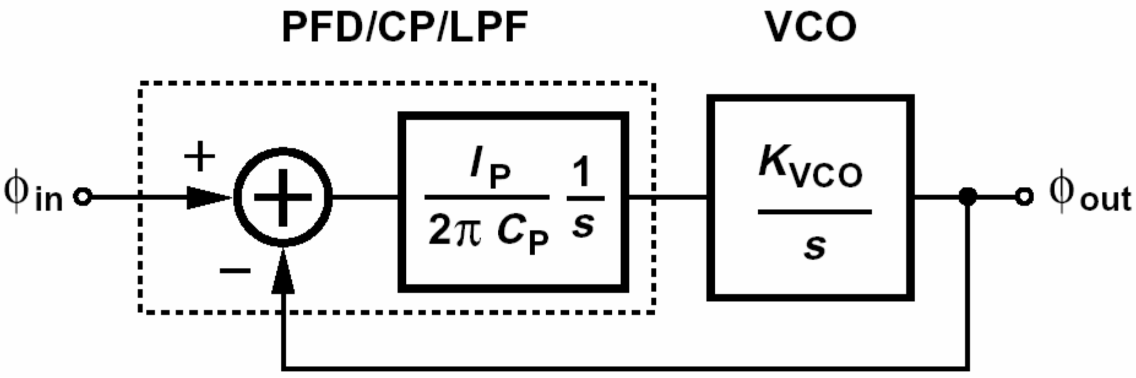




$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{s}$$

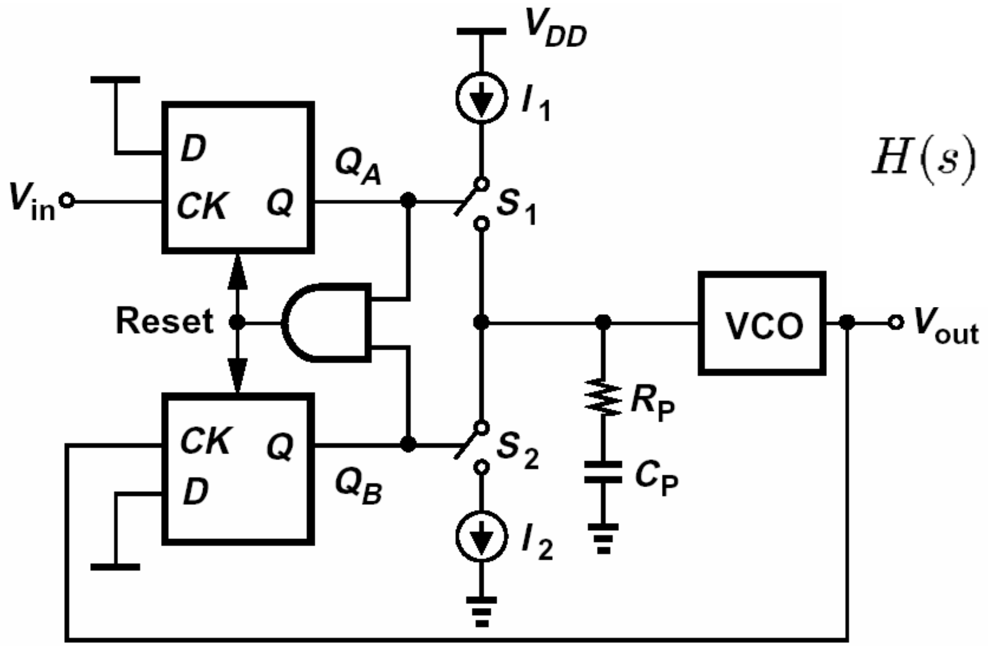
First Attempt to Close the Loop





$$H(s) = \frac{\dfrac{I_P K_{VCO}}{2\pi C_P}}{s^2 + \dfrac{I_P K_{VCO}}{2\pi C_P}}$$

Type II (Charge-Pump) PLL

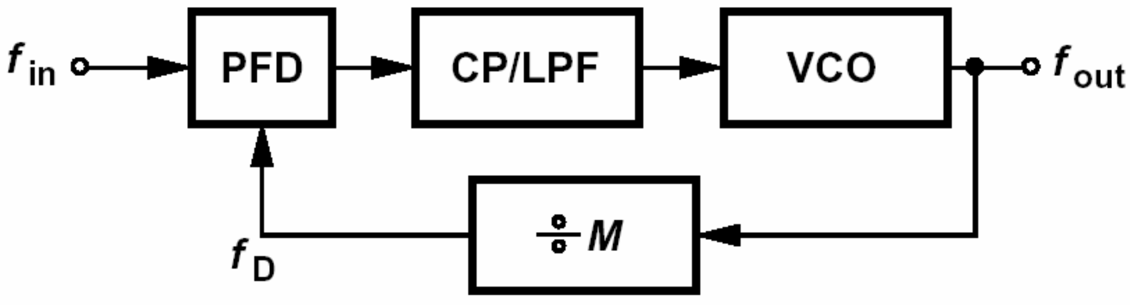


$$H(s)=\frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s+1)}{s^2+\frac{I_P}{2\pi}K_{VCO}R_P s+\frac{I_P}{2\pi C_P}K_{VCO}}.$$

$$\omega_n=\sqrt{\frac{I_P K_{VCO}}{2\pi C_P}}$$

$$\zeta=\frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}}$$

Frequency Multiplication Revisited



$$H(s) = \frac{\frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s}}{1 + \frac{1}{M}\frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s}}$$

$$= \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}\frac{K_{VCO}}{M}R_P s + \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}}$$

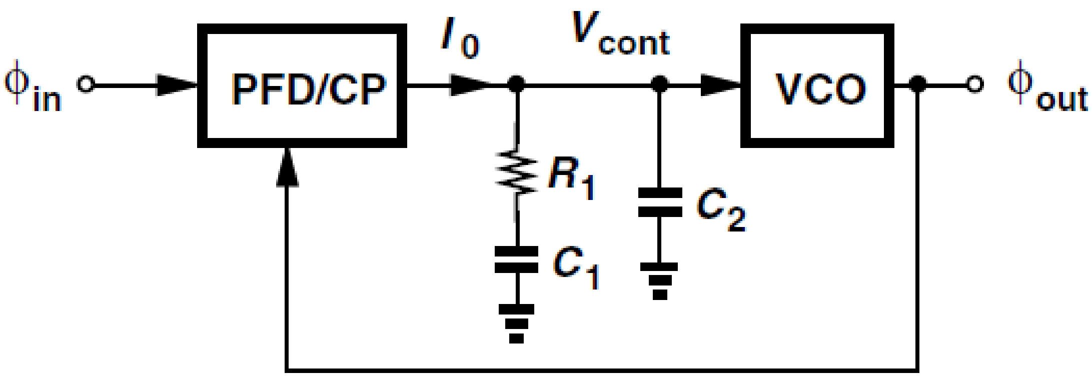
$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}}$$

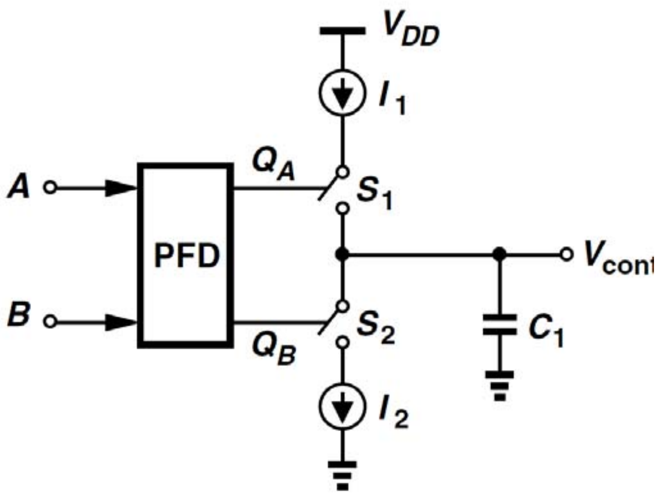
$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P}{2\pi}\frac{K_{VCO}}{M}}$$

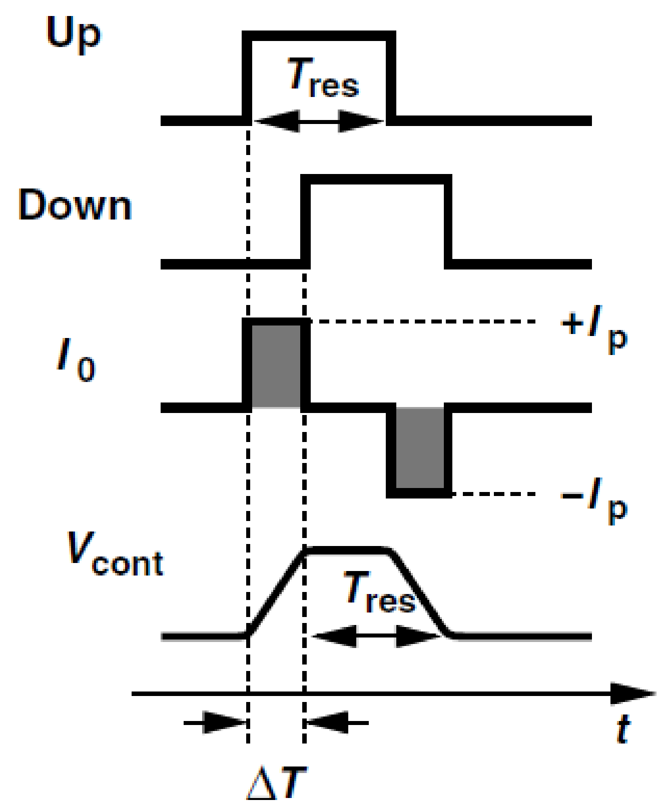
PFD/CP Nonidealities

- Skew between Up and Down Pulses
- Mismatch between Up and Down Currents
- Charge Sharing
- Channel-Length Modulation
- Charge Injection Mismatch

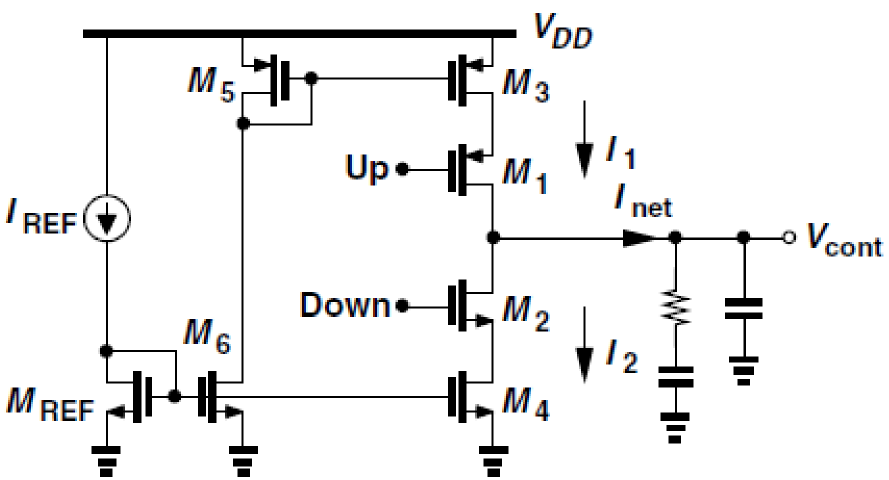
Problem of Skew

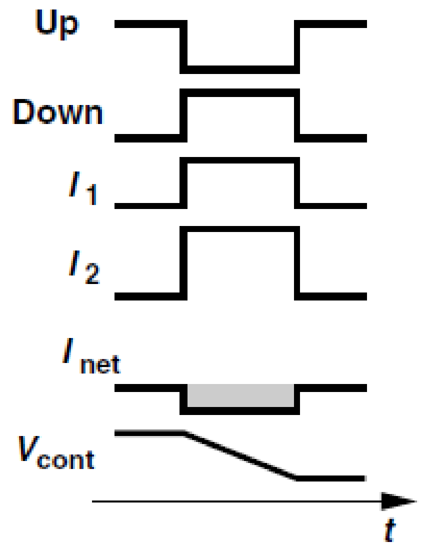


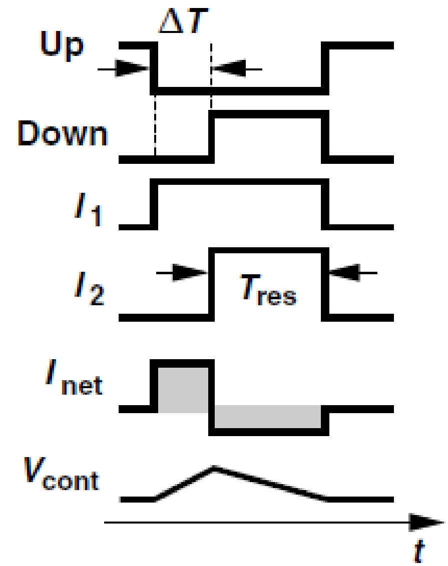




Up and Down Current Mismatch

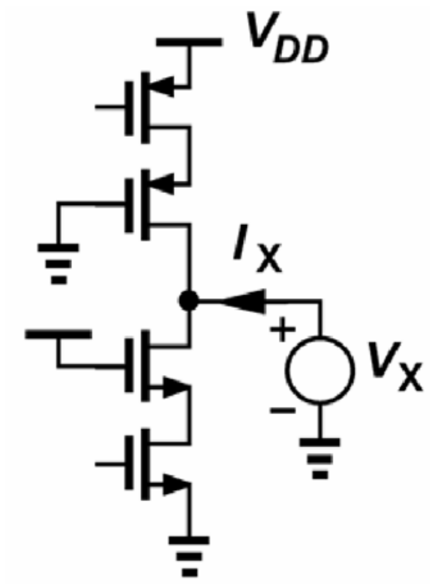


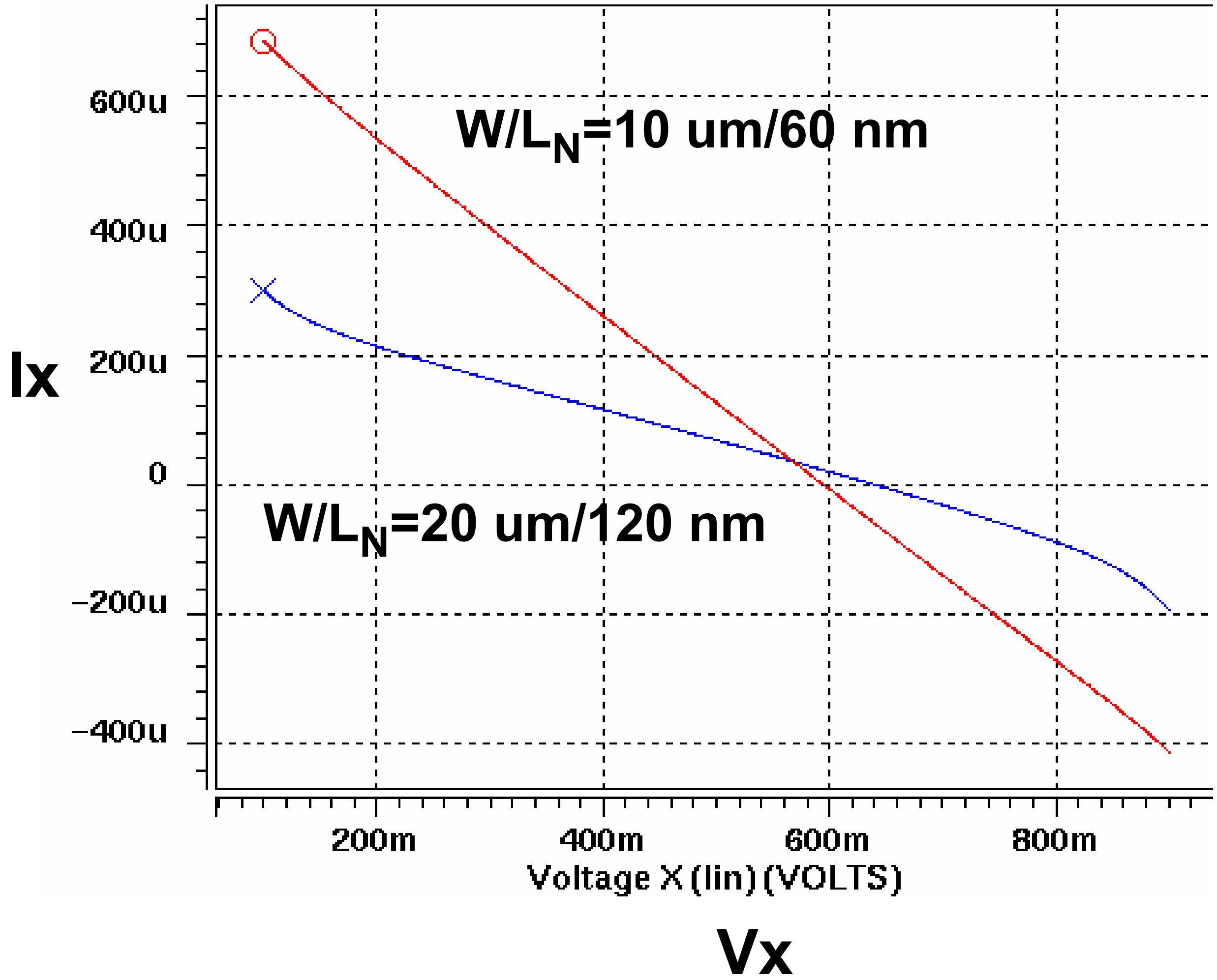




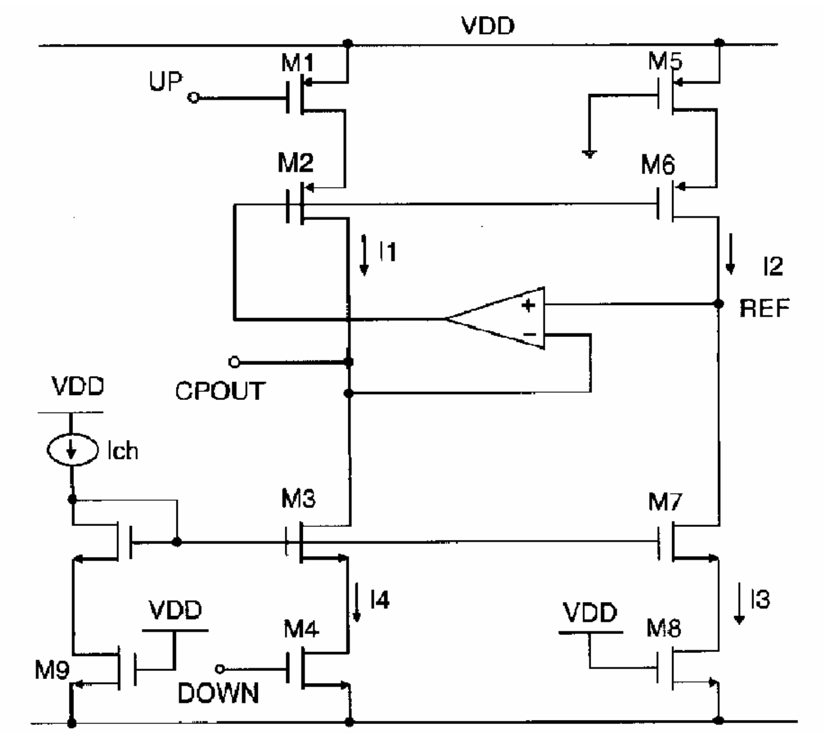
- Produces both ripple and phase offset.

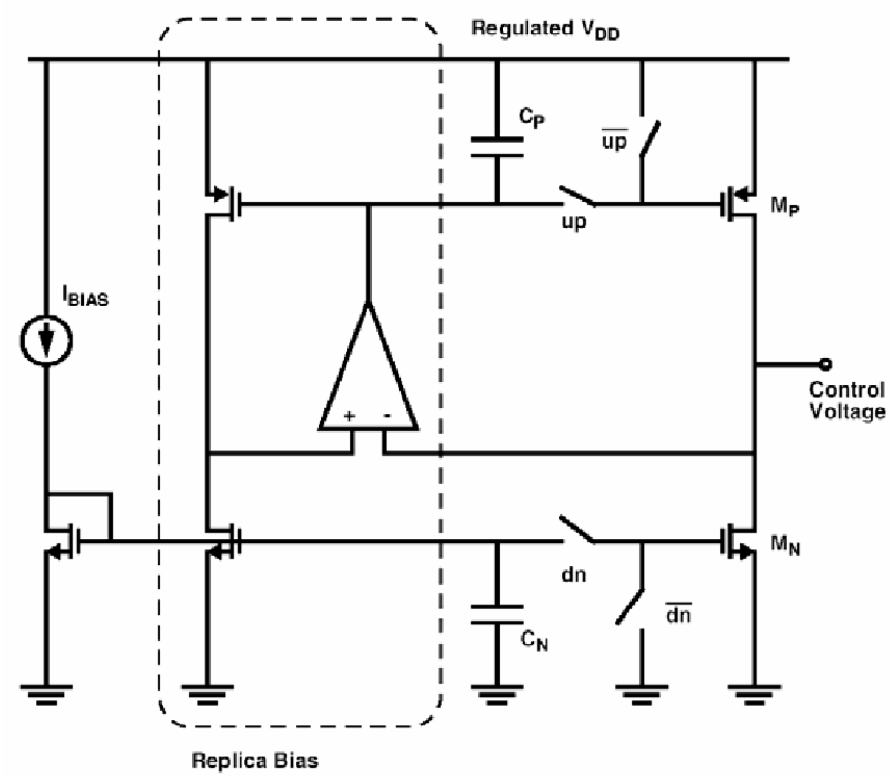
Channel-Length Modulation





Reduction of Channel-Length Modulation

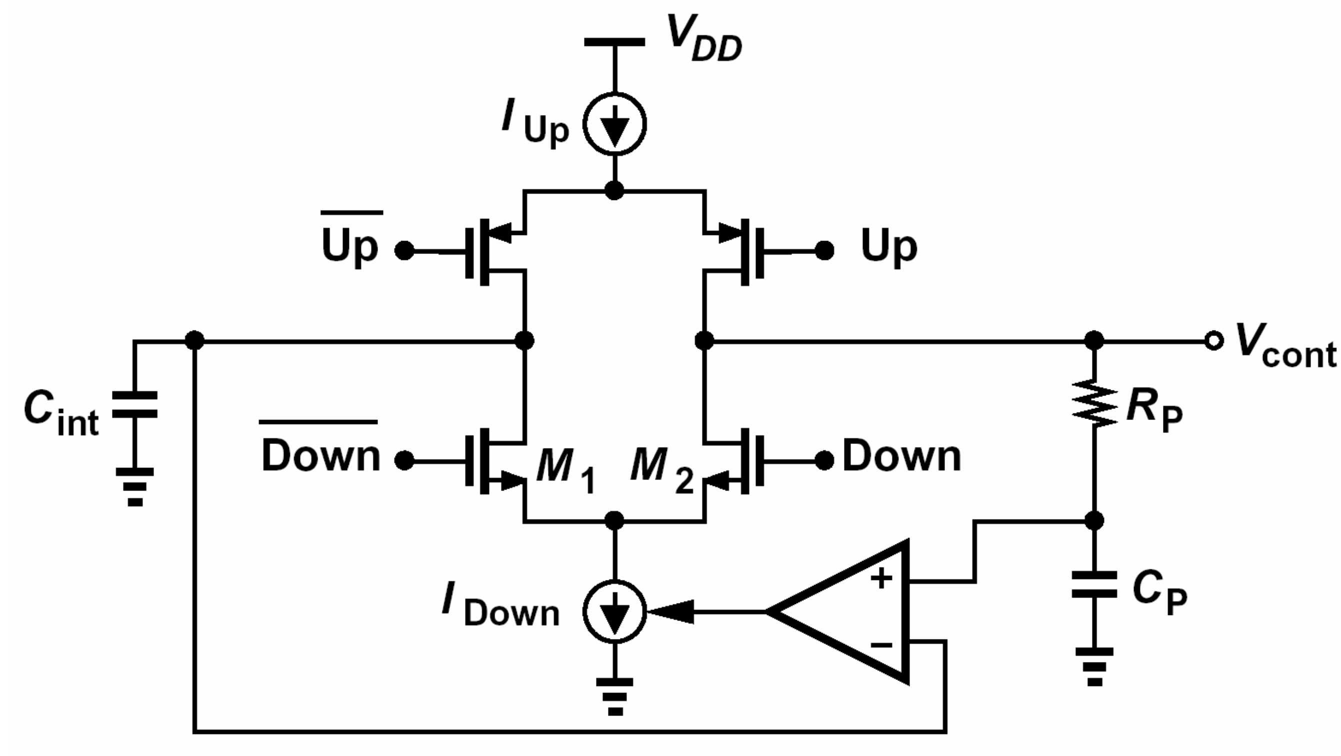




[Lee, Elec. Let., Nov. 00]

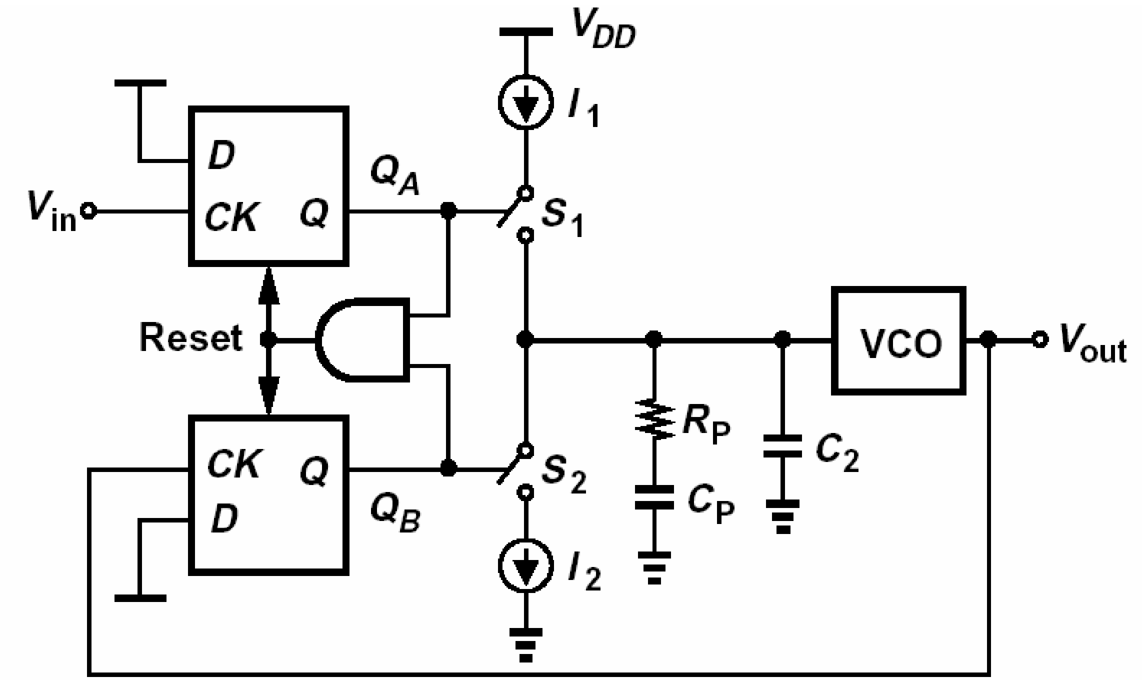
[Terrovitis, ISSCC04]

Reduction of Both Mismatches



[Wakayama, US Patent 7,057,465 B2]
(Also, see Gierkink, ISSCC08]

Addition of Second Capacitor



- C_2 can reach 0.2Cp with little degradation in settling behavior.
- But imposes an upper bound on Rp.

PLL Design Procedure

- Design VCO for frequency range of interest and obtain K_{VCO}.
- Set the "loop bandwidth" to one-tenth of input frequency:

$$\omega^2_{-3dB} = \left[(2\zeta^2 + 1) + \sqrt{(2\zeta^2 + 1)^2 + 1}\right] \omega_n^2$$

(Loop BW ~ $2.5\omega_n$ for $\zeta = 1$.)

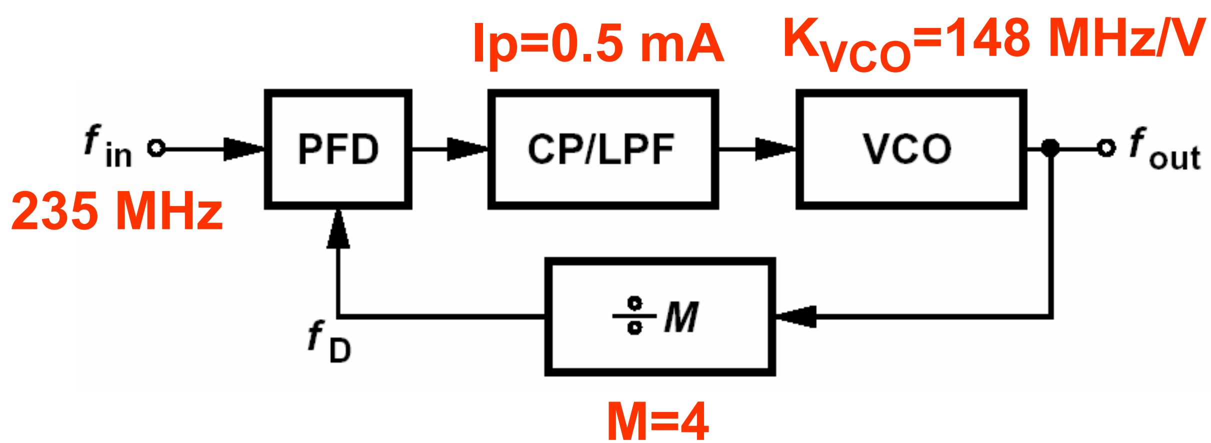
- Select a charge pump current (tens of microamps to some milliamps).
- Set the damping factor to 1 and compute Rp and Cp.

$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P} \frac{K_{VCO}}{M}}$$

$$\zeta = \frac{R_P}{2} \sqrt{\frac{I_P C_P}{2\pi} \frac{K_{VCO}}{M}}$$

Charge Pump Design

- Select W/L of current sources for an overdrive of about 50-100 mV.
- Choose L such that mismatch due to channel- length modulation remains below 10-20%.
- Choose switch dimensions for a headroom consumption of 20-30 mV.
- If mismatch due to channel-length modulation results in excessive jitter or sidebands:
  (a) Increase C_2 and Cp (BW goes down).
  (b) Use one of the circuit techniques to reduce effect of channel-length modulation.



Simulated Behavior