Integer-N and Fractional-N Synthesizers

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Outline

- General Synthesizer Requirements
- Integer-N Synthesizers
- Basic Fractional-N Synthesizer
- Randomization and Noise Shaping

General Considerations



- Channel Spacing
- Frequency Accuracy
- Phase Noise
- Sidebands (Spurs)
- Lock Time
- Power Dissipation

Channel Spacing and Frequency Accuracy

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Slight shift leads to significant spillage of high-power interferer.

Phase Noise



Corruption of Signal:

$$x_{QPSK}(t) = A\cos\left[\omega_c t + (2k+1)\frac{\pi}{4} + \phi_n(t)\right] \quad k = 0, \cdots, 3$$

Lock Time



> If damping factor is $\sqrt{2}/2$ then the settling time is given by

$$t_s = \frac{\sqrt{2}}{\omega_n} \ln \left| \sqrt{2} \left(1 - \frac{N_1}{N_2} \right) \frac{1}{\alpha} \right|$$

Causes spillage of TX output power to other channels.

A well-designed PLL settles in roughly 100 input cycles.

Sidebands



- Manifests itself in blocking tests and adjacent channel tests.
- Trades with settling time.

Basic Integer-N Synthesizer



- Frequency channel is assigned by the base station at the beginning of communication.
- Output frequency step = reference frequency
- > Example: Find the reference frequency for a Bluetooth receiver using sliding-IF conversion with $f_{LO} = (2/3)f_{RF}$.

Integer-N Synthesizer Design

- > VCO
- Dual-Modulus Divider
- PFD/CP
- Loop Filter
- Spur Reduction Techniques
 - Up/Down Skew Reduction
 - Up/Down Current Mismatch Reduction
 - Sampling Loop Filter

Pulse Swallow Divider



- Prescaler begins with N+1 and counts until swallow counter fills up.
- Prescaler now divides by N until program counter fills up.

Drawbacks of Integer-N Synthesizers



- Output frequency step = reference frequency
- Slow settling if channel spacing is small.
- Little phase noise suppression of VCO if channel spacing is small.
- High amplification of reference phase noise
- Difficult to operate with different crystal frequencies.

Fractional-N Synthesizers: Preview

- Toggle the divide ratio between N and N+1 periodically to create an average value equal to N+α.
- But this modulates the VCO frequency periodically, generating sidebands.



Toggle the divide ratio between N and N+1 randomly to convert sidebands to noise.

- But the phase noise is now too high.
- Shape" the spectrum of noise to move its energy to high frequencies, and let the PLL filter out the highfrequency noise.





- ➤ Decouples output frequency step from the input reference frequency → Wider loop bandwidth →
 - Faster settling
 - Greater VCO phase noise suppression
 - Less amplification of reference phase noise

Fractional Spurs



VCO produces sidebands at ±0.1MHz×n around 10.1MHz.

Conversion of Spurs to Noise



Instantaneous frequency of feedback signal:

$$f_{FB}(t) = \frac{f_{out}}{N + b(t)}$$

b(t) randomly toggles between 0 an 1 and has an average value of α :



Basic Noise Shaping



Generate a random binary sequence, b(t), that switches the divider modulus between N and N+1 such that

(1) the average value of the sequence is α .

(2) the noise of the sequence has a high-pass spectrum.

Negative Feedback System as a High-Pass System



Discrete-time version:





Σ-Δ Modulator Example



- Quantization from *m*+2 bits to 1 bit introduces significant noise, but the feedback loop shapes this noise in proportion to *1-z⁻¹*.
- Choice of *m* is given by the accuracy with which the synthesizer output frequency must be defined.

Noise Shaping in a $\Sigma\Delta$ Modulator



Basic $\Sigma \Delta$ Fractional-N Synthesizer



- > Σ-Δ modulator toggles divide ratio between *N* and *N*+1 so that the average is equal to $N+\alpha$.
- Quantization noise in divide ratio is high-pass shaped.

Higher-Order Noise Shaping

High-Order Loop: Replace 1-bit quantizer with a finer quantizer:



Replace delaying integrator with non-delaying integrator:



Noise Shaping in First- and Second-Order Modulators



Problem of Out-of-Band Noise

> Transfer function from quantization noise to frequency noise:

$$\begin{split} Y(z) &= (1-z^{-1})^2 Q(z). & \qquad \text{Second-Order} \\ \Phi(z) &= (1-z^{-1}) Q(z). \end{split}$$

> Spectrum of $\Sigma\Delta$ phase noise:

$$S_{\Phi}(f) = |1 - z^{-1}|^2 S_q(f)$$

= $|2 \sin(\pi f T_{CK})|^2 S_q(f).$

Spectrum of PLL output phase noise:

$$S_{out}(f) = |2\sin(\pi f T_{CK})|^2 S_q(f) N^2 \frac{4\zeta^2 \omega_n^2 \omega^2 + \omega_n^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \omega_n^2 \omega^2},$$



Nonlinearity Due to Charge Pump Mismatch



(ΔT_{in} is proportional to quantization noise)

> Total charge delivered to the loop filter in (b) is equal to:

$$Q_{tot1} = I_1 \cdot \Delta T_{in} + (I_1 - I_2) \cdot \Delta T_1.$$

> Now reverse the polarity of the input phase difference:

$$Q_{tot2} = I_2 \cdot \Delta T_{in} + (I_1 - I_2) \Delta T_1$$

 ΔT_{in} is negative here

Effect of Charge Pump Nonlinearity



- > Approximate the error by a parabola, $\alpha \Delta T^2_{in}$ b, and write $Q_{tot} \approx I_{avg} \Delta T_{in} + \alpha \Delta T^2_{in}$ -b
- > The multiplication of ΔT_{in} by itself is a mixing effect and causes convolution:



Effect of Charge Pump Nonlinearity



[Huh, JSSC, Nov. 05]