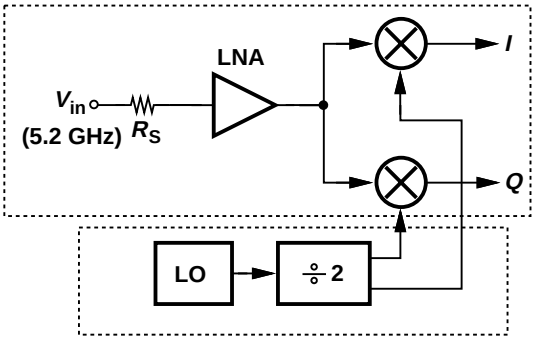
Final Project

Due Fri., March 15, 2013 (No electronic submission)

In this project, each team of two members will design a 5.2-GHz direct-conversion CMOS receiver. Shown below, the circuit employs an oscillator and a divide-by-2 circuit. Assume $R_S = 50\ \Omega$.



The dashed boxes suggest a possible partitioning between the two partners.

Design Requirements

- $NF_{tot} = 6$ dB, $IIP_3 = -12$ dBm
- Input Resistance $\approx 50\ \Omega$, Output Resistance $< 1200\ \Omega$
- $V_{DD} = 1.8$ V
- Phase noise of 5.2-GHz LO < -110 dBc/Hz at 1-MHz offset

Design Constraints

The challenge in this project is to achieve the above specifications with minimum power consumption while meeting the following constraints:

- On-chip inductors have a Q of 6. Use the model described in the fourth homework.
- Chip area considerations limit the total on-chip inductance to 200 nH.
- You may use only one external inductor with a relatively high Q at the input of the receiver. In addition, you can use one bondwire inductance with a Q of 15 for degeneration of the input stage.
- Each on-chip capacitor has a bottom-plate parasitic of 5%.

Project Report

Your report is an important part of your final project. Do not leave it until the last moment. It should be a concise and accurate presentation of your design, not exceeding 10 pages. Do not turn in raw SPICE results. I grade projects based on: innovation, credibility, overall performance, and the quality of the project report.