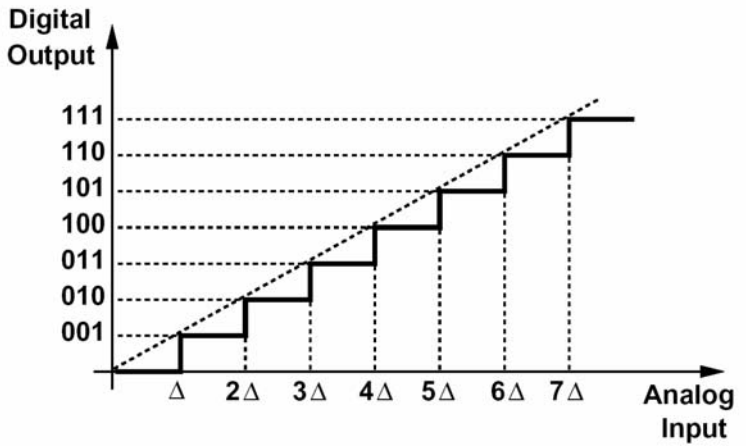
Introduction to A/D Conversion

Basic Concepts

D = f(A)

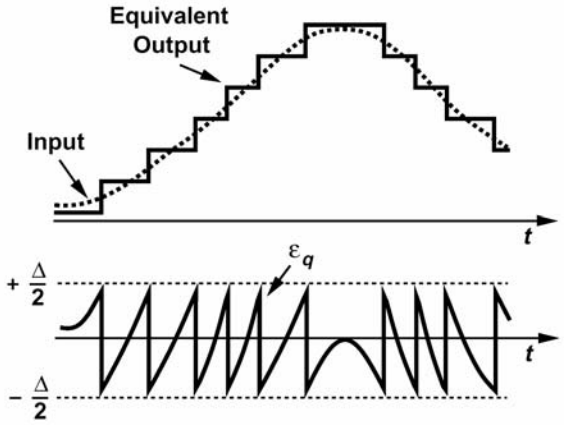
The input can assume an infinite number of values, whereas the output can be selected from a finite set of codes ("quantization").

Example:



Quantization Error

The Difference between the original input and the quantized output is called the quantization error, ε_q.
For resolution above 4 bits, ε_q can be regarded as random noise.



We assume ε_q is:

1. a random variable uniformly distributed between $-\Delta/2$ and $+\Delta/2$.
2. independent of the analog input.

➢ Quantization noise power:

$$\overline{\varepsilon_q^2} = \int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} \varepsilon_q^2 \cdot \frac{1}{\Delta} \cdot d\varepsilon_q$$

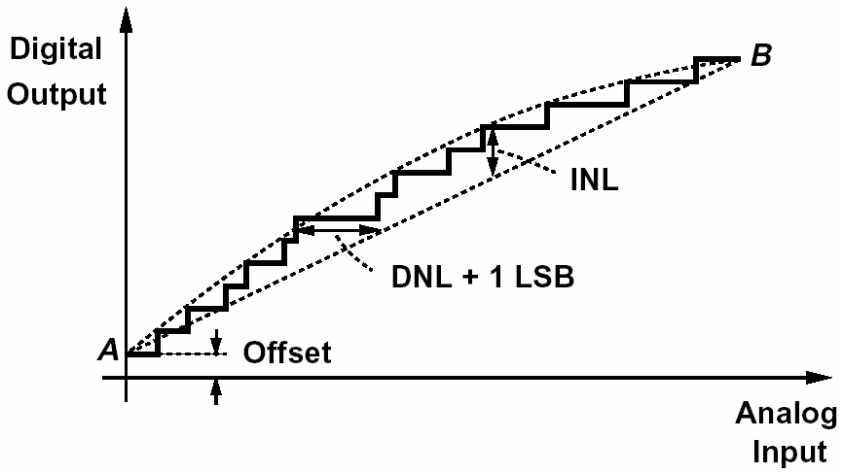
$$= \frac{\Delta^2}{12}$$

For a full-scale sinusoid: $V_{in} = \frac{V_{ref}}{2} \sin\omega t$,

$$SNR_{peak} = \frac{3}{2} \cdot 2^{2m}$$

$$= 6.02m + 1.76 \text{ dB}$$

Performance Metrics



- DNL is the maximum deviation in the difference between two consecutive code transition points on the input from the ideal value of 1 LSB.

- INL: same as that of DACs.

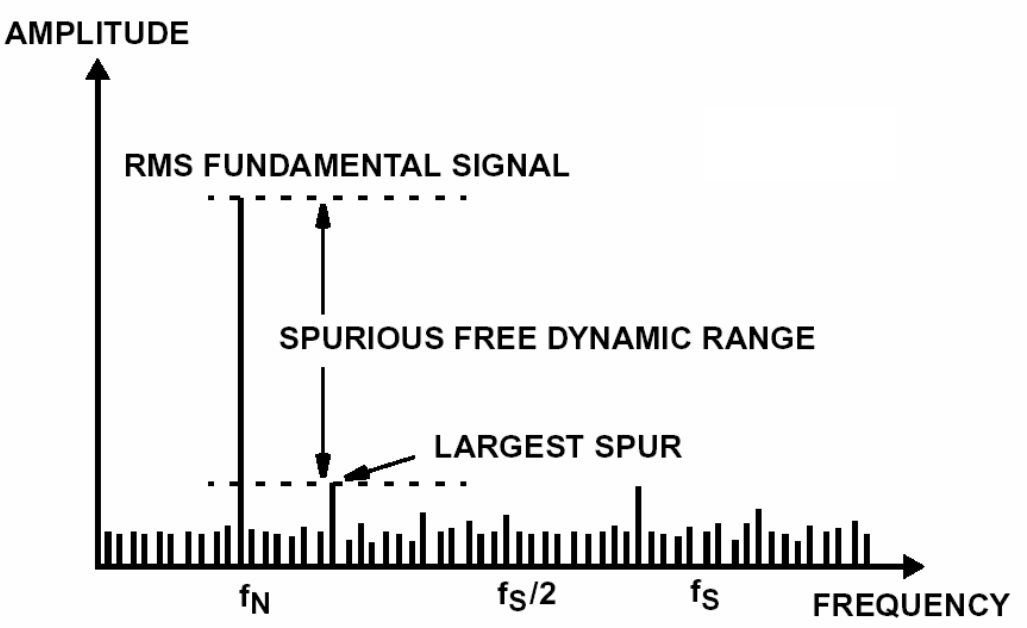
- Signal-to-(Noise + Distortion) (SNDR) is the ratio of the signal power to the total noise and harmonic power at the output, when the input is a sinusoid.
- Effective Number of Bits (ENOB):

$$ENOB = \frac{SNDR_p - 1.76}{6.02},$$

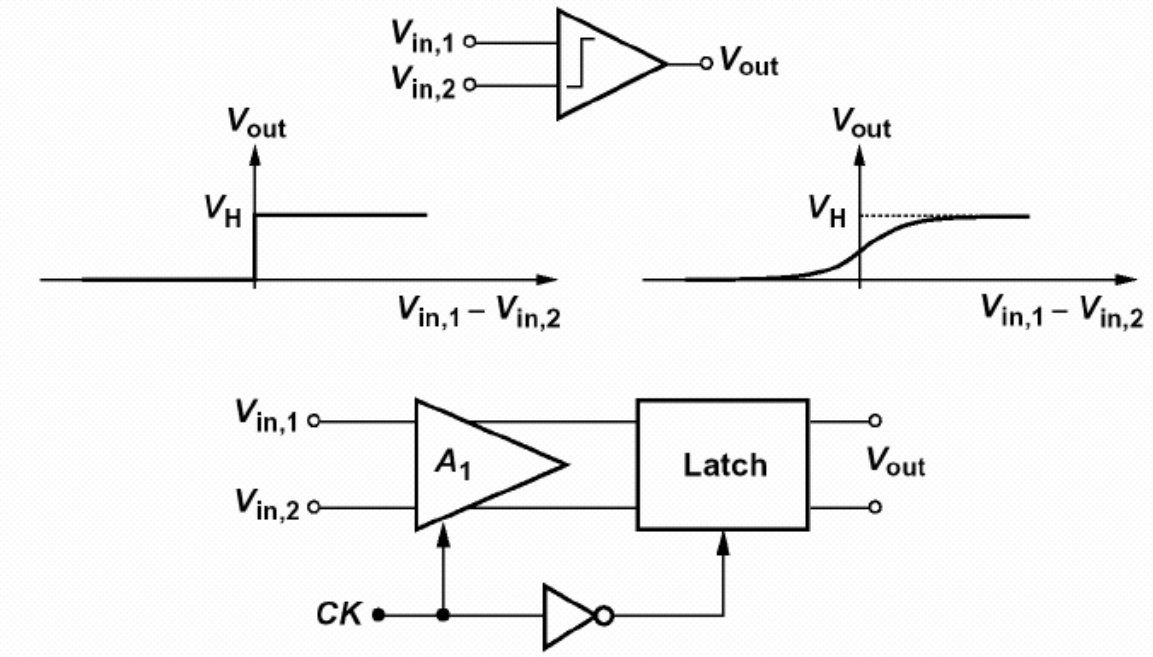
where $SNDR_p$ is the peak SNDR expressed in dB.

- **Dynamic Range is the ratio of the power of a full-scale sinusoid to the power of a sinusoid for which SNR = 0dB.**

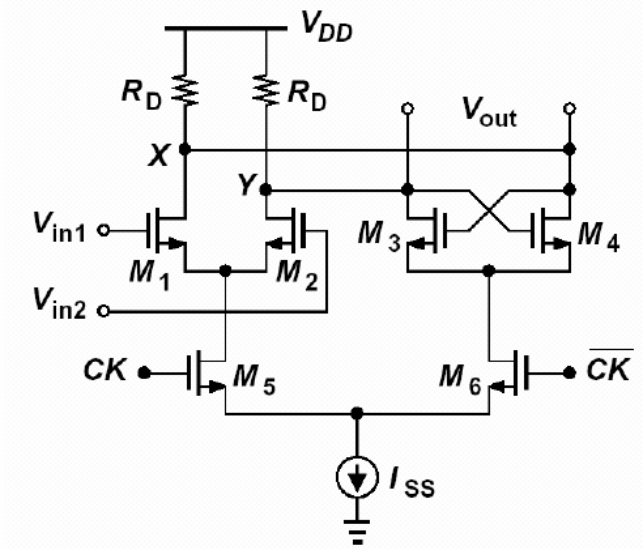
- **Spurious-Free Dynamic Range (SFDR): The difference (in dB) between the amplitude of the fundamental and the largest harmonic or spur (from dc to half of sampling rate).**



Comparator Basics



Example:



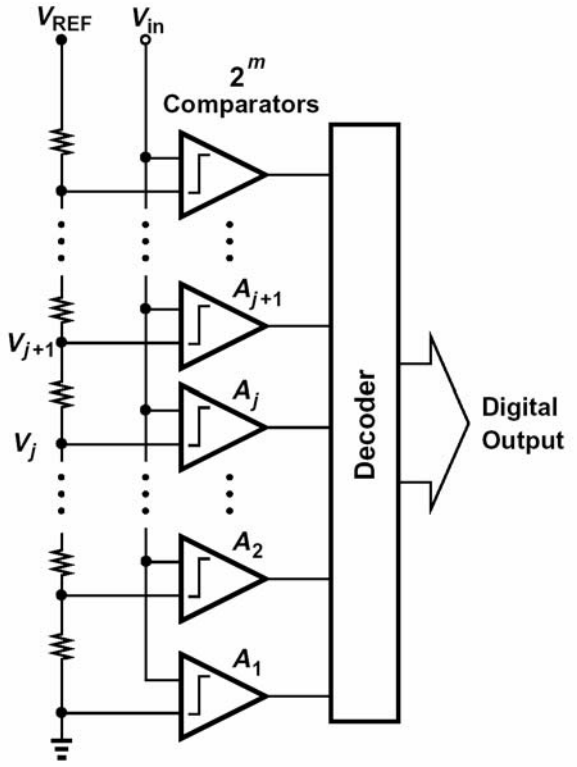
Metastability:

If the input difference is small, the outputs take a long time to reach logical levels.

Flash A/D Converters

Architecture

Need to figure out where the analog input is with respect to a set of evenly-spaced references.
-->Compare the input with all of the references on one clock edge.



If the comparators are designed as described before, they perform "sampling" in addition to quantization. This is because, at the moment of strobe, each comparator sores with polarity of its input difference.

➔ **Flash converters, in principle, need no front-end SHA. Since comparators achieve much higher speeds than SHAs, flash architectures can be very fast.**

Issues

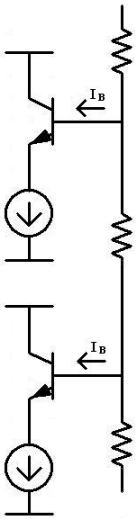
Area, Power, Input Cap. α 2^m
Comparator Offset
Nonlinear Input Cap
Reference Ladder Bowing
Kickback Noise
Sparkles (Bubbles) & Metastability
Slew-Dependent Delay

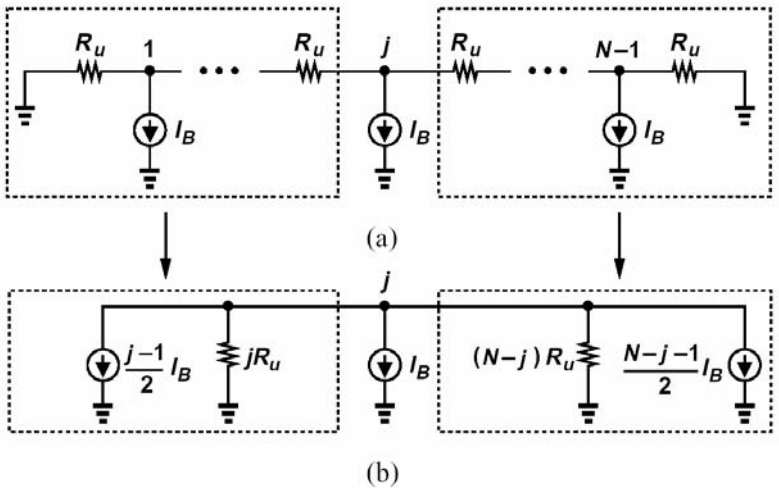
Problem of Input Capacitance

Suppose the resolution must be increased from 4 bits to 6 bits. What happens to the input capacitance?

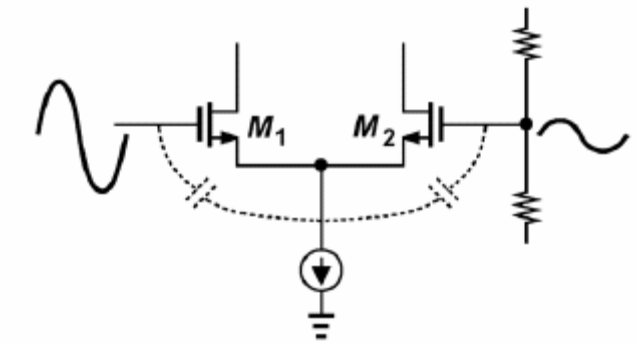
Reference Ladder Bowing

Each comparator may draw an input bias current from the ladder. This causes dc bowing.



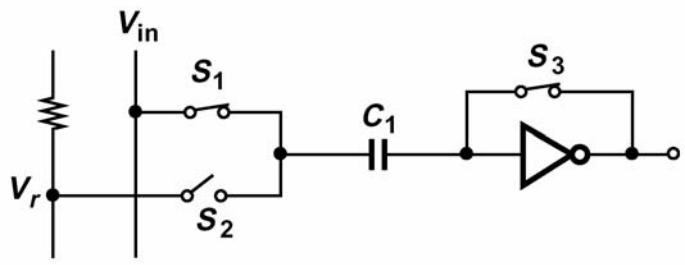


In addition, capacitive paths between the two inputs of each comparator feed part of the analog input to the ladder. This causes ac bowing.

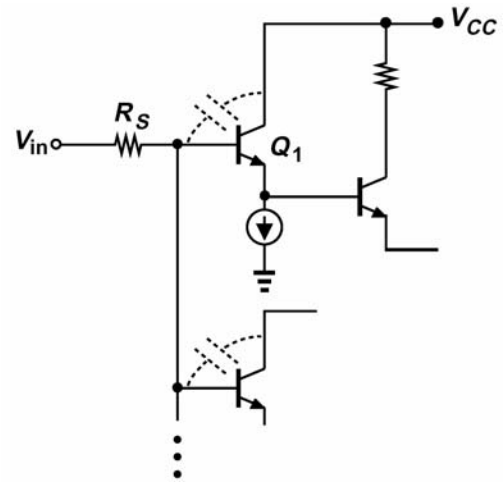


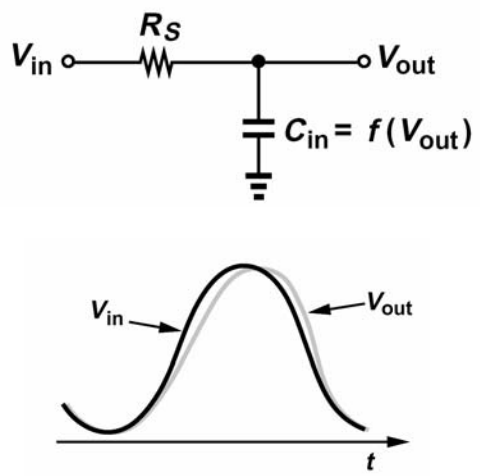
How to reduce this effect?

A More Subtle Bowing:



Nonlinear Input Cap

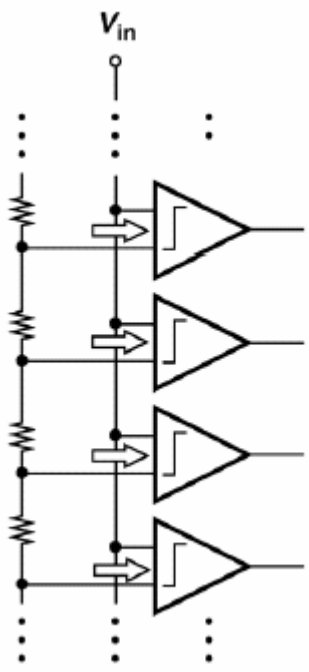




Kickback Noise

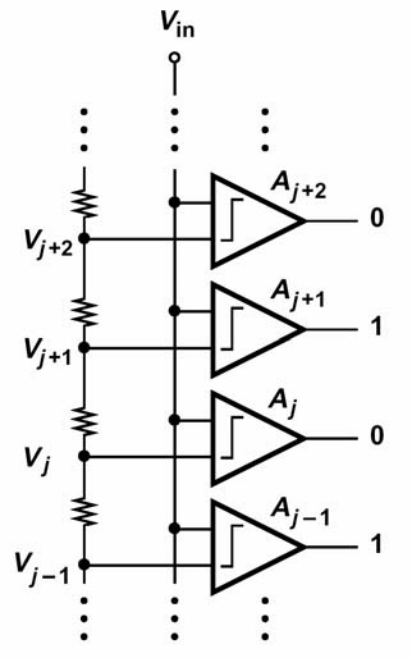
The switching operations inside each comparator generally result in transient currents drawn from the input. For a large number of comparators, the effect can be approximated in the same way as dc

bowing. The importance issue is that the kickback noise must diminish before the next conversion.

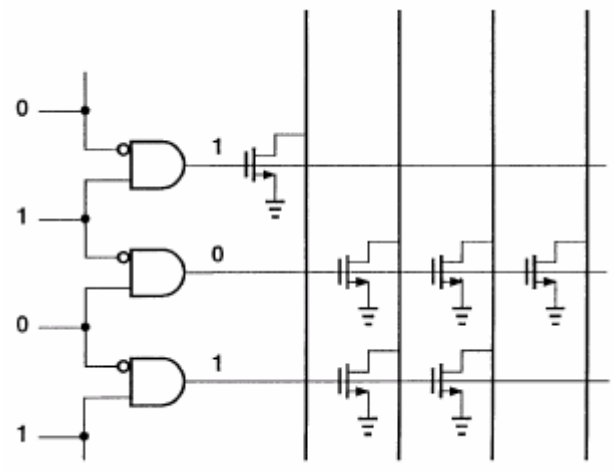


Bubbles in Thermometer Code

If a fast-varying analog input is applied to a flash converter, the thermometer output may exhibit a "sparkle" or "bubble." This occurs because the comparators perform sampling and sometimes their decisions are not consistent.



Effect of Bubbles on Decoding:

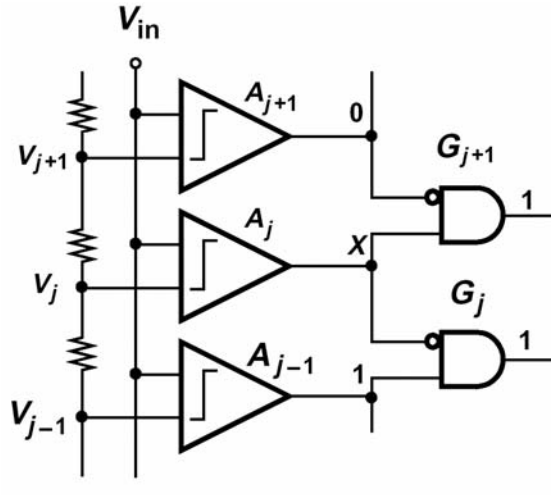


How do we correct for bubbles?

Metastability

If the "sampled" value of V_{in} is very close to V_r, the comparator will have an indeterminate output for a long time, possibly causing an erroneous digital output.

Example:



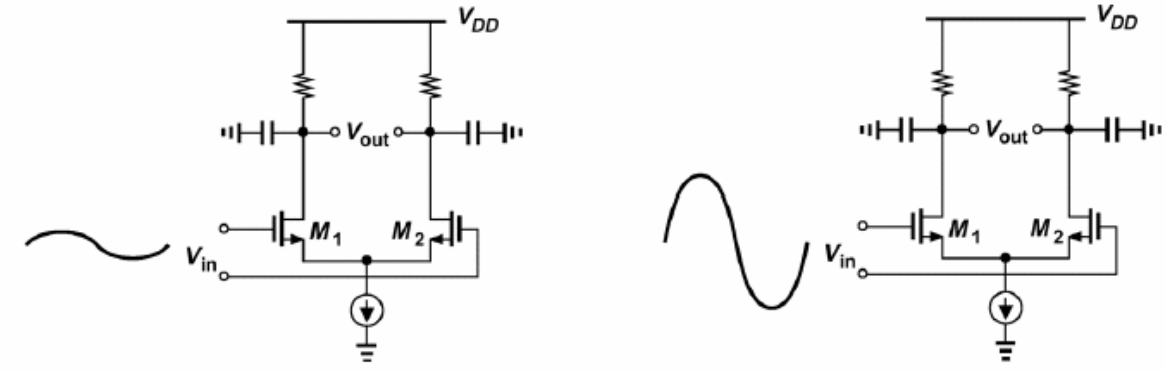
Important Observation:

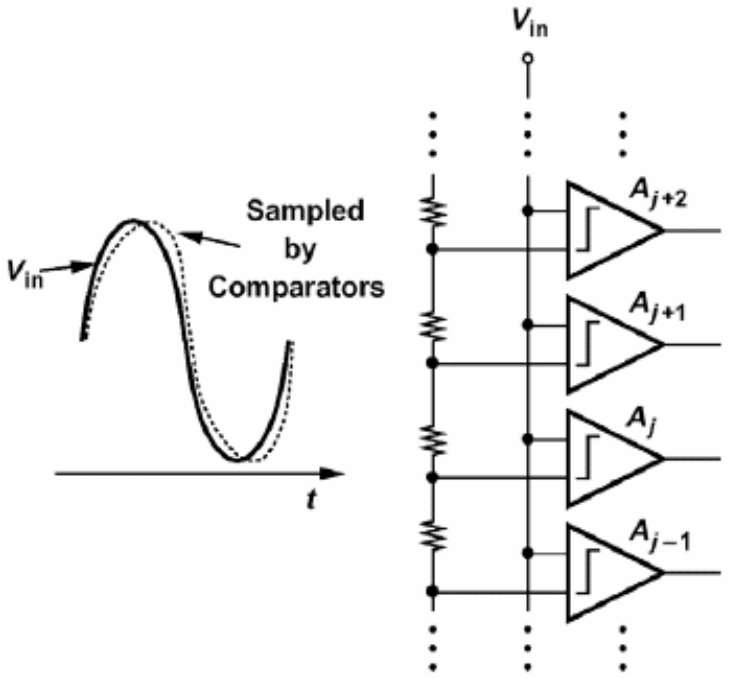
If a metastable level splits (going to more than one gate), it can cause an error, even with pipelining. If it does not split, we can continue to pipeline.

How to reduce metastability errors?

- **Lower τ_R in latch (i.e. burn more power)**
  (has imitations in every technology.)
- **Use direct pipelining after each latch.**
- **Use Gray encoding with pipelining.**

Slew-Dependent Phase Shift





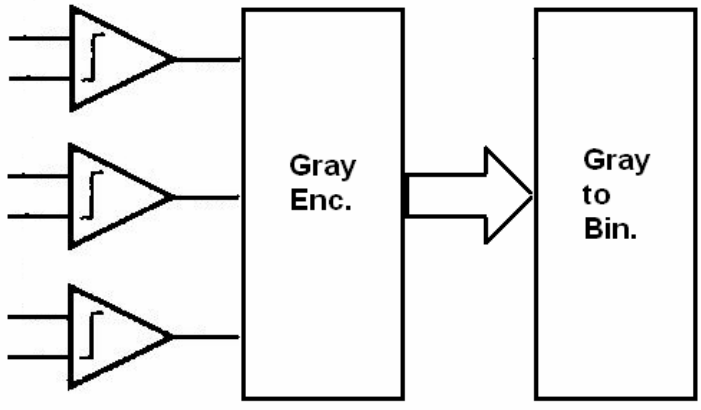
Clock Jitter & Dispersion

If clock and analog input are distributed on a large chip, they may experience different delays due to different loading. Also, the clock waveform is "dispersed" due to RC effects.

Gray Encoding

Both metastablility and sparkles can be reduced using Gray encoding.

Two properties of Gray encoding prove useful in reducing metastability:



1. No Signal splits in the encoder:

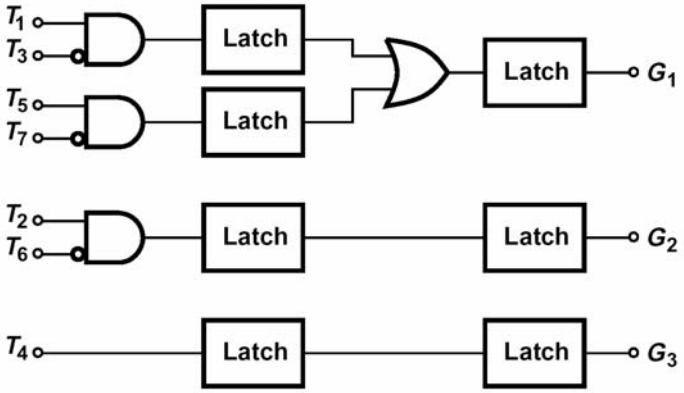
Thermometer							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	A	B	C
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$

$G_2 = T_2\overline{T_6}$

$G_3 = T_4$

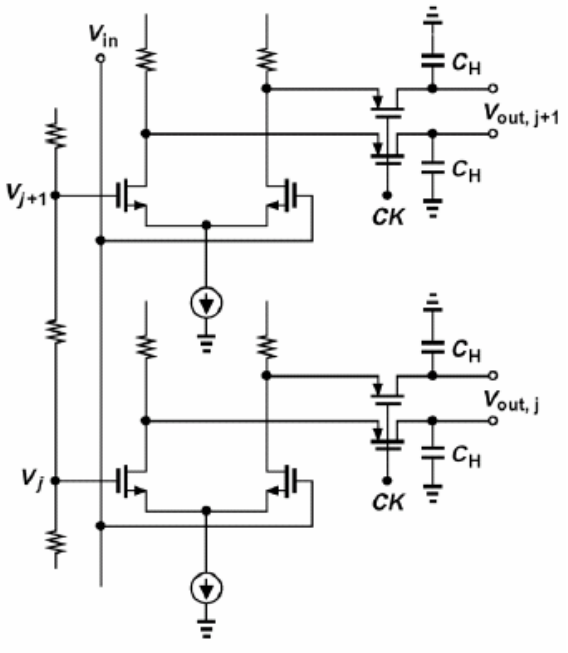
2. The number of latches after every level of logic reduces by a factor of 2.



Gray encoding improves the response to bubbles because its accuracy degrades gracefully as the number of sparkles increases:

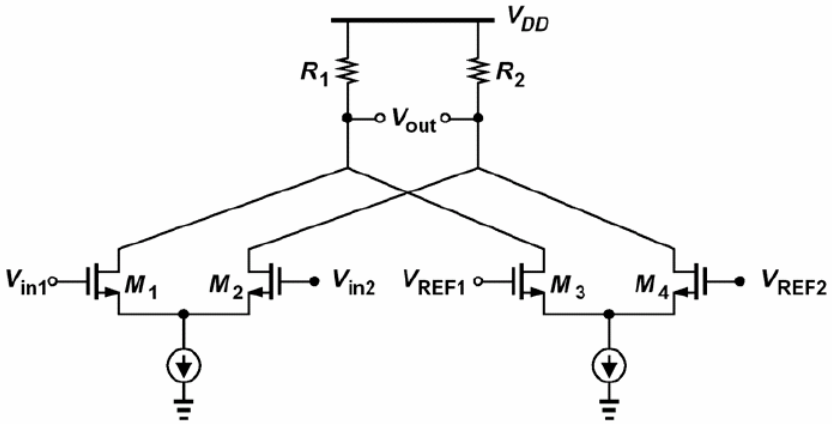
	Thermometer Code	Gray Code	Equivalent Decimal Output
No Sparkle:	11111111111100	1011	13
One Sparkle:	11111111111010	1000	15
Two Sparkles:	11111111111001	1010	12

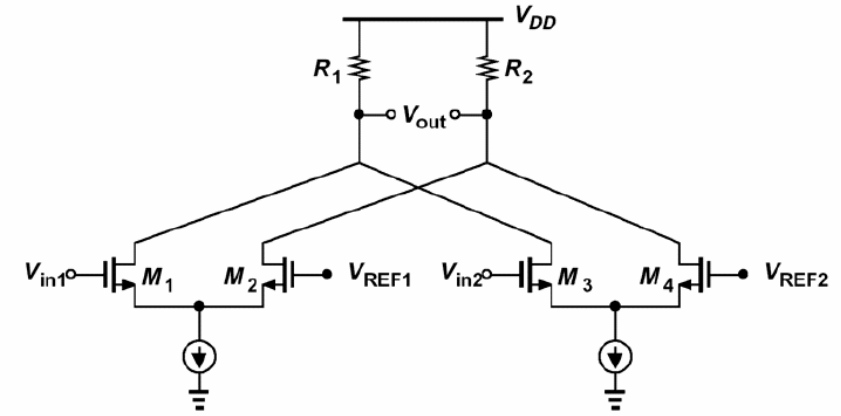
Lumped vs. Distributed Sampling (Venes, JSSC, Dec. 96)



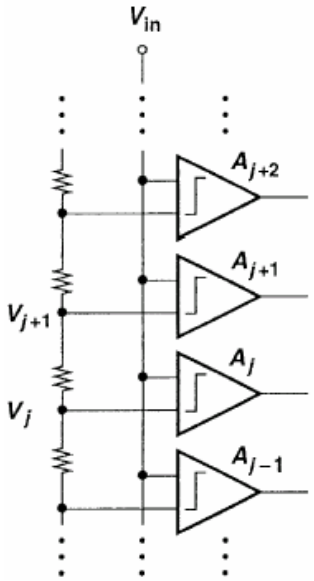
Differential Difference Amplfier

For fully differential inputs:

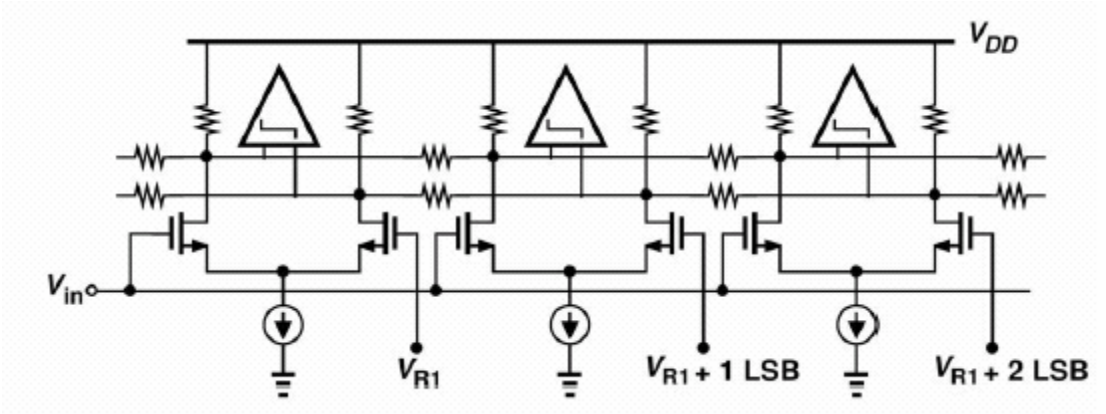


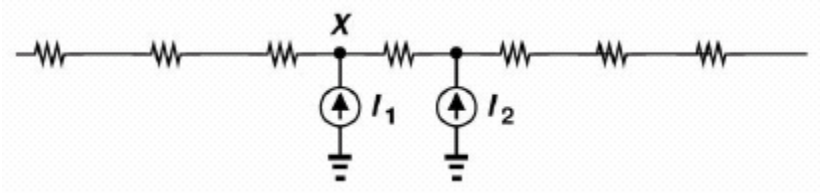


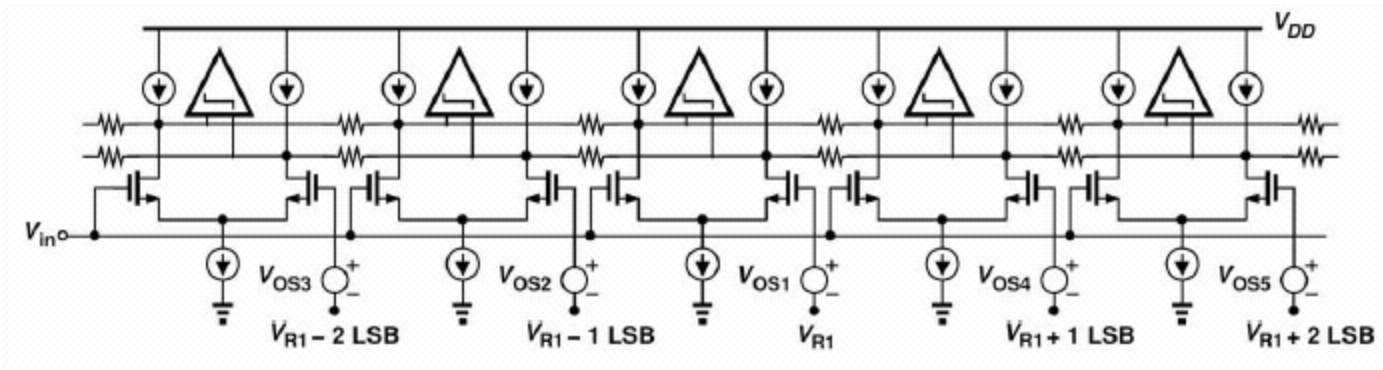
Effect of Comparator Offset



Resistor Averaging






V_{DD}
V_{in}
V_{OS3}
V_{OS2}
V_{OS1}
V_{OS4}
V_{OS5}
V_{R1} – 2 LSB
V_{R1} – 1 LSB
V_{R1}
V_{R1} + 1 LSB
V_{R1} + 2 LSB

Two-Step ADC Architectures

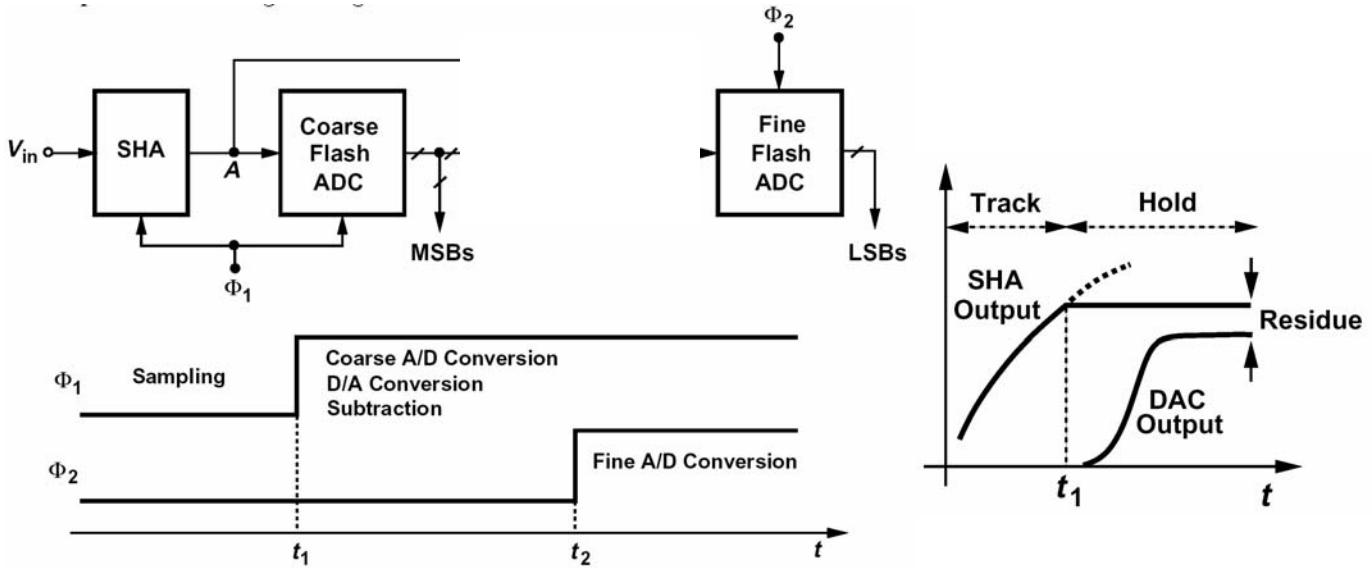
General Concepts

With flash (i.e., one-pass) conversion, the system complexity and power dissipation make it difficult to exceed 8 bits of resolution.

- **Need to do conversion in two or more passes (or "steps".)**

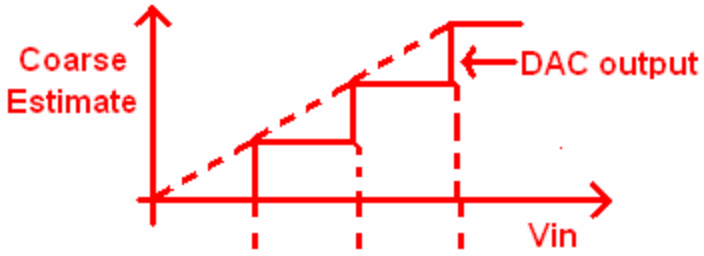
In a two-step ADC, we first perform a coarse conversion to find an estimate of the input. Next, we perform a fine conversion to determine the input level with higher accuracy:

How do we build a two step ADC?



How do speed, area, and power compare with those of straight flash?

Concept of Residue



The effect of errors can be studied at the output of the coarse flash stage, the output of the DAC, the output of the subtractor, or the output of the fine flash stage.

Example: Effect of Subtractor Offset

Design Issues

- SHA Settling: The coarse conversion cannot begin immediately after the SHA enters the hold mode because the SHA output takes a while to settle:

- SHA Linearity & Noise: The input signal is processed by the SHA before it gets to the converter

- Coarse Comparator Offset: How much offset can we tolerate in the first-stage comparators?

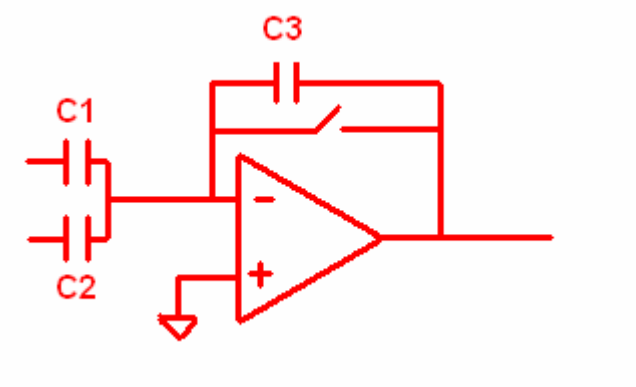
- DAC Nonlinearity: Since the DAC output is subtracted from the analog input, any nonlinearity in the DAC output can be considered as a nonlinear term corrupting the input.

Important Note: Here, the DAC has a relatively low resolution but must have a high linearity.

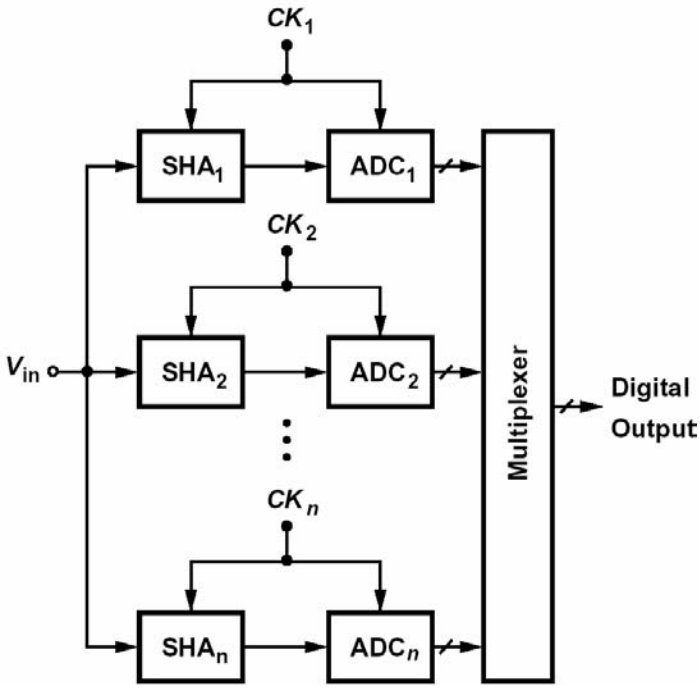
- DAC Settling: The DAC must settle within <0.5 LSB of its final value before the subtractor can trust its output.
- Can we use pipelining in the DAC?

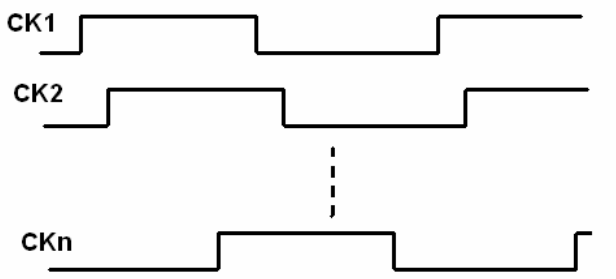
- Subtractor offset voltage

Example of Subtractor Implementation



Interleaved ADCs

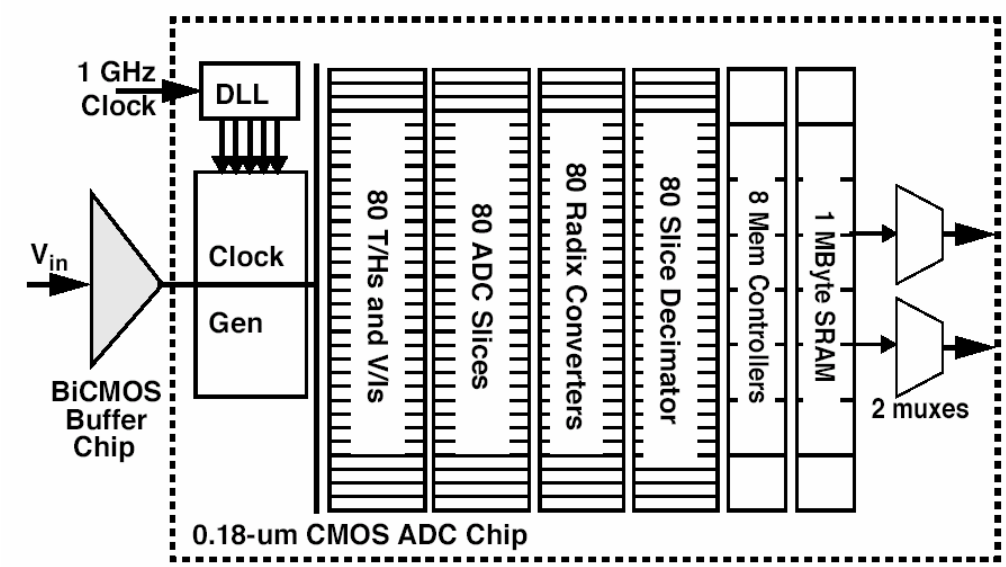




Issues:

1. **SHA bandwidth must be commensurate with input BW.**
2. **Mismatches: offset, gain error, timing**

Example: 20G 8b ADC [Poulton, ISSCC 03]



Sample Rate	20 GSa/s	
Resolution	8 bits	
INL Intrinsic With linearity correction	 ±1.7 LSBs ±0.4 LSBs	
DNL	±0.3 LSBs	
Bandwidth	6.6 GHz	
Accuracy @ 500 MHz input @ 6 GHz input	 6.5 effective bits 4.6 effective bits	
Jitter	0.7 ps rms	
Input Range	0.25 Vpk differential	
	Buffer Chip	**ADC Chip**
Input Capacitance	0.2 pF	4 pF
Power	1 W	9 W
Chip Size	1.2 x 2.6 mm	14 x 14 mm
Technology	40-GHz SiGe BiCMOS	0.18-mm CMOS
Transistors	1000	50M
Package	438-ball BGA	

Calibration is performed in software. Using a sawtooth calibration waveform, per-slice gain and offset values are measured and corrected with 160 on-chip DACs. Then gain coefficients for each stage of each pipeline are calculated and loaded into the radix converter, so that corrected 8b binary data comes out. Next, Fourier analysis of a pulse waveform is used to set the on-chip per-slice timing adjustments.