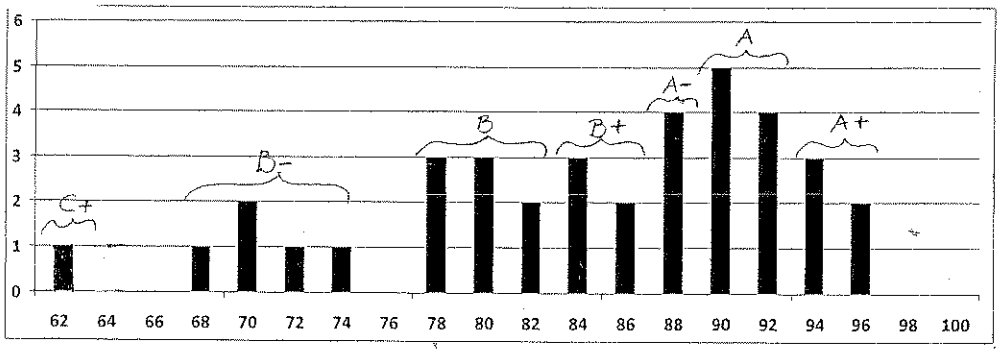
EE 215D

Final Exam

Spring 2012



Name: Solutions

Time Limit: 3 Hours

Open Book, Open Notes

1. 20
2. 20
3. 10
4. 20
5. 10

Total: 80

1. Assume a sinusoid of the form $V_{REF}\sin(2\pi f_0 t)$ is applied to the input of a pipelined ADC. Also, assume the clock frequency is about $20f_0$ and the input voltage range is from $-V_{REF}$ to $+V_{REF}$.

(a) Sketch the output of the first MDAC as a function of time for a 1-bit/stage architecture.

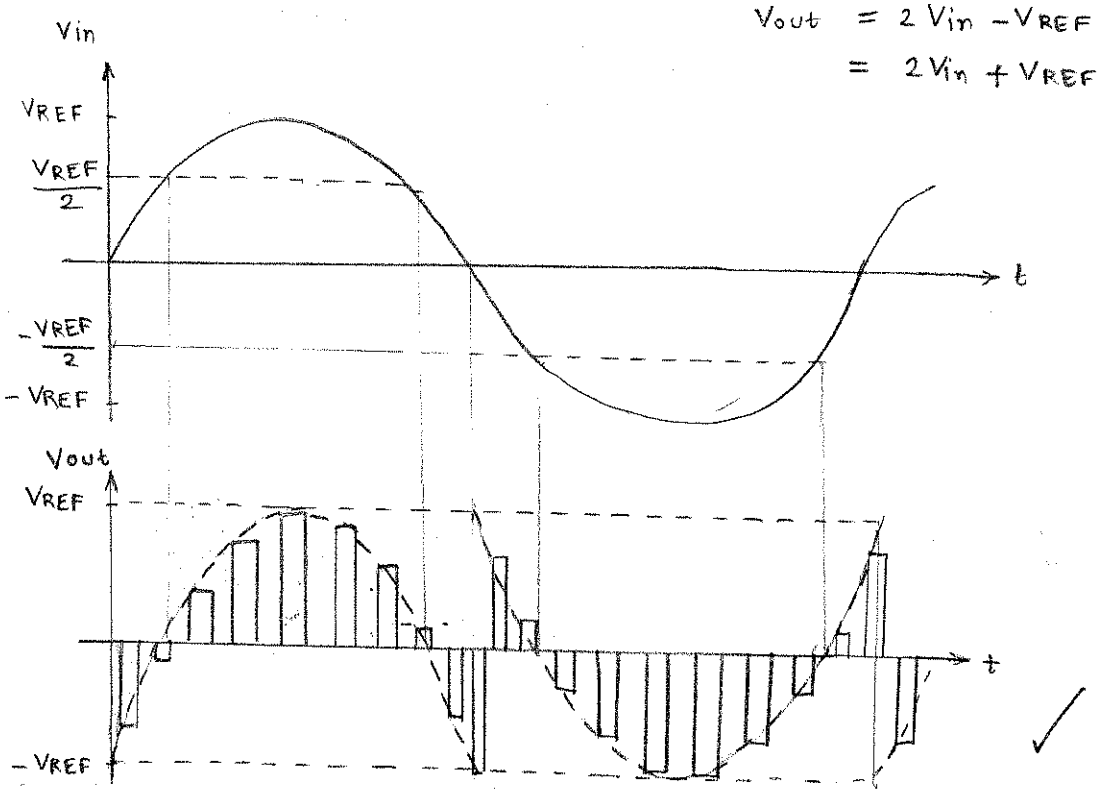
(b) Repeat (a) for a 1.5-bit/stage architecture.

For 1-bit/stage:

$V_{out} = 2V_{in} - V_{REF}$, $V_{in} > 0$

$= 2V_{in} + V_{REF}$, $V_{in} < 0$

(a)

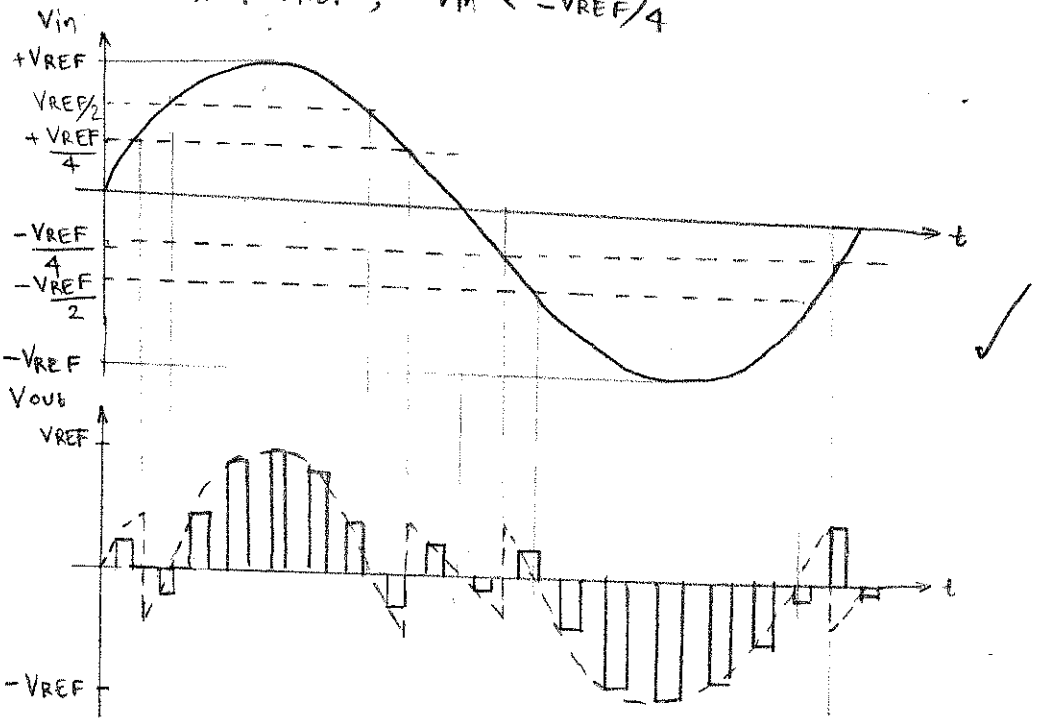


(b) For 1.5-bit/stage

$V_{out} = 2V_{in} - V_{REF}$, $V_{in} > V_{REF}/4$

$= 2V_{in}$, $-V_{REF}/4 < V_{in} < V_{REF}/4$

$= 2V_{in} + V_{REF}$, $V_{in} < -V_{REF}/4$



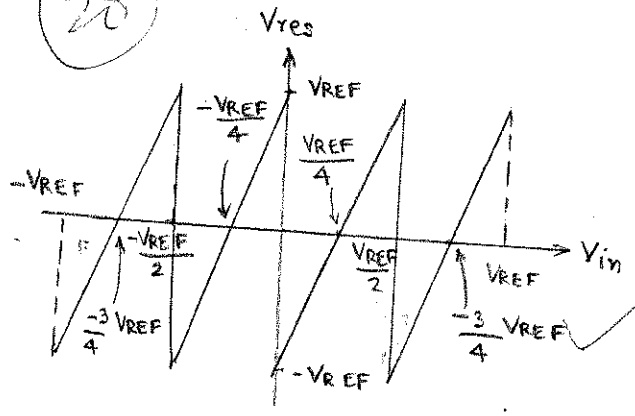
2. A pipelined ADC resolves 2 bits in the first stage. Assume an input voltage range from $-V_{REF}$ to $+V_{REF}$. Also, assume that fractions of $\pm V_{REF}$ are not available.

(a) If the residue must also range from $-V_{REF}$ to $+V_{REF}$, derive residue expressions similar to $V_{res} = 2V_{in} \pm V_{REF}$ for this architecture.

(b) Plot the residue as a function of V_{in}.

(c) Draw the circuit diagram of this stage, showing the comparators, their reference voltages, and the MDAC along with all of its capacitors. Clearly show between what voltages the left plates of the capacitors ar switched. Make sure your circuit satisfies your residue equations. You need not draw the internal circuits of the comparators or the op amp.

(a), (b) 20



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$$V_{res} = \begin{cases} 4V_{in} + 3V_{REF}, & V_{in} < -\frac{V_{REF}}{2} \\ 4V_{in} + V_{REF}, & -\frac{V_{REF}}{2} < V_{in} < 0 \\ 4V_{in} - V_{REF}, & 0 < V_{in} < \frac{V_{REF}}{2} \\ 4V_{in} - 3V_{REF}, & V_{in} > \frac{V_{REF}}{2} \end{cases}$$

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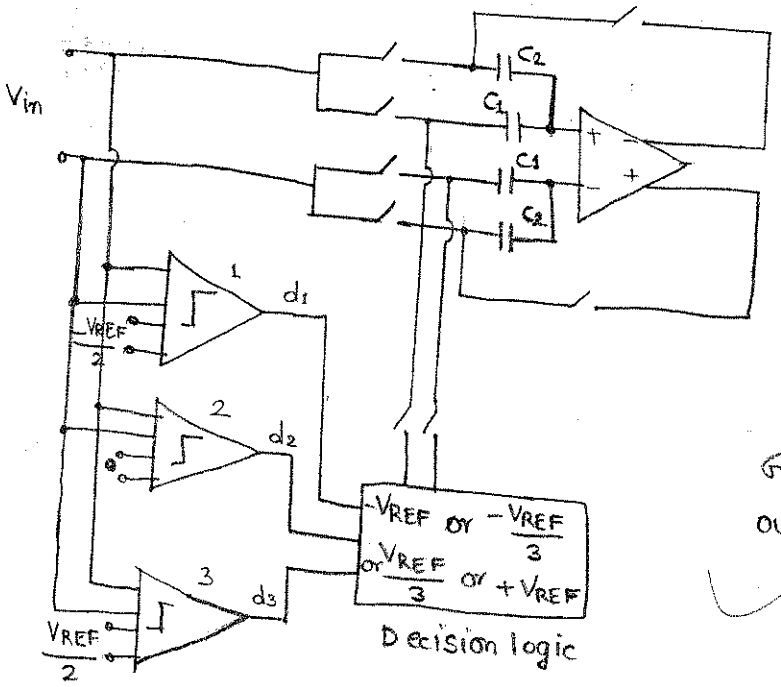
(c)



$C_1 = 3C_2 \Rightarrow$ Vin will appear at o/p with a gain of 4

Comparator 1 compares Vin with $-\frac{V_{REF}}{2}$ to give o/p d_1,

comparator 2 compares Vin with 0 to give o/p d_2 & comparator 3 compares Vin with $+\frac{V_{REF}}{2}$ to give o/p d_3.

Gain from left plate of C_1 to output $= -\frac{C_1}{C_2} = -3$.

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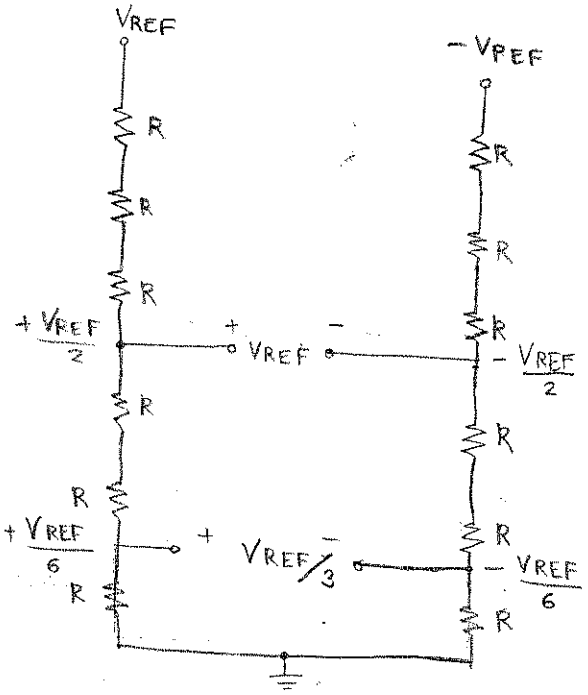
PTO

$d_1\ d_2\ d_3$	V_{in}	Left plate of C_1 switched to	V_{out}
0 0 0	$V_{in} < -\frac{V_{REF}}{2}$	$-V_{REF}$	$4V_{in} + 3V_{REF}$
1 0 0	$-\frac{V_{REF}}{2} < V_{in} < 0$	$-\frac{V_{REF}}{3}$	$4V_{in} + V_{REF}$
1 1 0	$0 < V_{in} < \frac{V_{REF}}{2}$	$+\frac{V_{REF}}{3}$	$4V_{in} - V_{REF}$
1 1 1	$V_{in} > \frac{V_{REF}}{2}$	$+V_{REF}$	$4V_{in} - 3V_{REF}$

Since fractions of $\pm V_{REF}$ is not available, they need to be generated using resistive divider.



Differentially, left plate of C_1 is switched to one of the 4 voltages

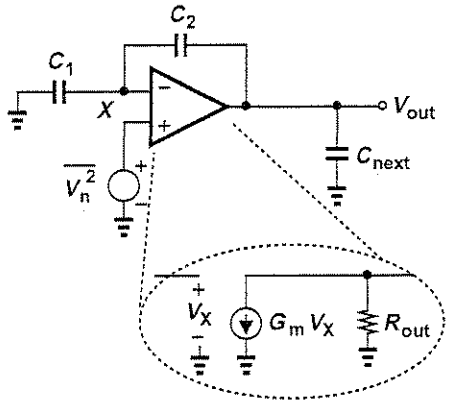
$$\frac{V_{REF}}{3} = +\frac{V_{REF}}{6} - \frac{-V_{REF}}{6}$$

$$-\frac{V_{REF}}{3} = -\frac{V_{REF}}{6} - \frac{V_{REF}}{6}$$

$$V_{REF} = \frac{V_{REF}}{2} - \frac{-V_{REF}}{2}$$

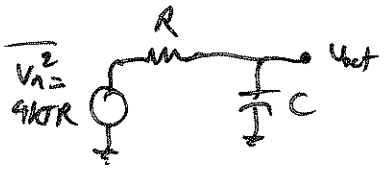
$$-V_{REF} = \frac{-V_{REF}}{2} - \frac{V_{REF}}{2}$$

3. Consider one MDAC stage of a pipelined ADC in the amplification mode. As shown below, the MDAC drives the input capacitor(s) of the next stage, denoted here by C_{next}. Modeling the op amp and its input-referred noise as shown below, determine the total noise measured across C_{next}. (Hint: the system is still of first order and lends itself to the equations covered in the first week.)



KCL @ output : $-G_m V_n = V_{out}\left[\underbrace{\frac{G_m C_2}{C_1+C_2} + \frac{1}{R_{out}}}_{\frac{1}{R_{eq}}} + s\underbrace{\left(C_{next} + \frac{C_1 C_2}{C_1+C_2}\right)}_{C_{eq}}\right]$

$\Rightarrow \frac{V_{out}}{V_n} = \frac{G_m R_{eq}}{1 + R_{eq} C_{eq} s}$ If we compare this with that of a simple RC circuit, we get:



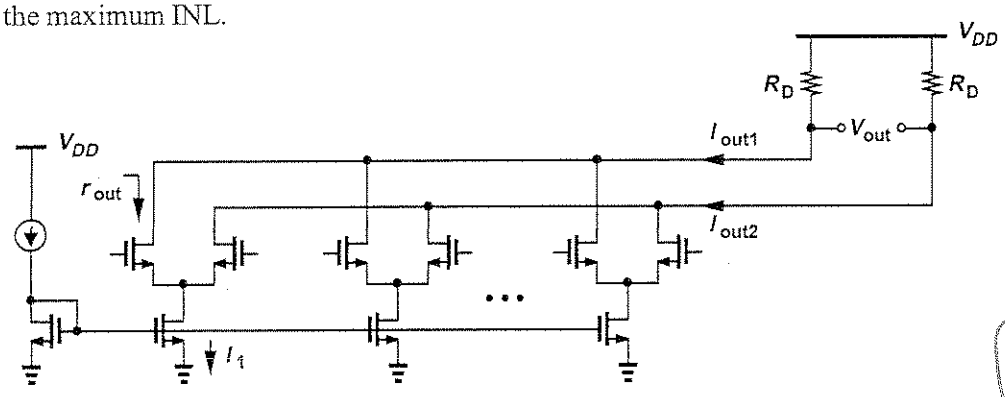
$\overline{V_n^2} = 4kTR$ $\quad \left|\frac{V_{out}}{V_n}\right| = \frac{1}{1+RCs}$

In our circuit we have $\overline{V_{out,n}^2} = V_n^2 \frac{G_m^2 R_{eq}^2}{4kT R_{eq}} \frac{kT}{C_{eq}} = V_n^2 \frac{G_m^2 R_{eq}}{4 C_{eq}}$

4. A current-steering DAC consists of 64 identical cells, each having a tail current of I_1 and an output impedance of r_{out}.

(a) Determine the INL profile for the *differential* output voltage, assuming that r_{out} is relatively large.

(b) Compute the maximum INL.



$N = 64$

a) $V_{out}(j) = j I_1 (R_D \| \frac{r_o}{j}) - (R_D \| (N-j) r_o) I_1$

$= I_1 R_D \left[j \frac{r_o/j}{r_o/j + R_D} - \frac{r_o}{r_o/(N-j) + R_D} \right] = V_{LSB} \left[j \frac{r_o/j}{r_o/j + R_D} - \frac{r_o}{r_o/(N-j) + R_D} \right]$

straight line $V_{ideal}(j) = (2N-j)(R_D \| \frac{r_o}{N})$

$INL(j) = V_{out}(j) - V_{ideal}(j) \approx \frac{R_D^2}{r_o^2} j (N/2 - j)(N-j) V_{LSB}$

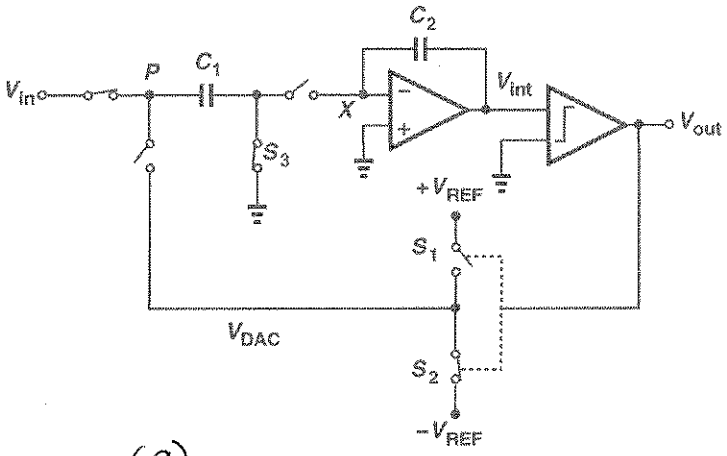
b) $\frac{\partial |INL(j)|}{\partial j} = 0 \Rightarrow j = (\frac{3 \pm \sqrt{3}}{6}) N$

and max $\approx \sqrt{3} (\frac{R_D}{r_o})^2 N^3/36$

5. Consider a first-order ΣΔ modulator. Using a continuous-time model, explain whether

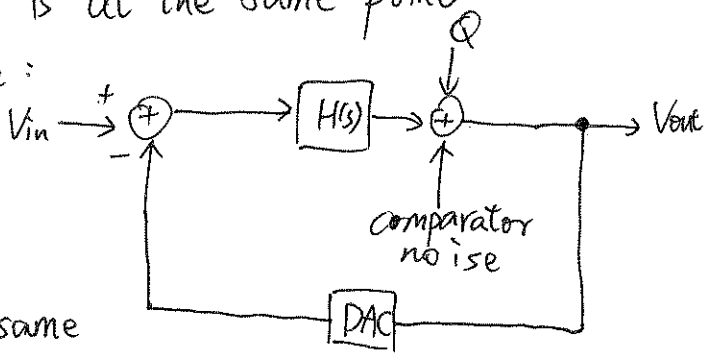
(a) The comparator noise is shaped.

(b) The noise in $\pm V_{REF}$ is shaped.



(a)

The comparator noise is at the same point as quantization noise:



Therefore, it has the same transfer function as quantization noise.

⇒ It is shaped.

(b)

The noise in DAC is added to V_{in}, so its transfer function is the same as V_{in}.

⇒ It is not shaped.