EE 215D
Spring 07

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HO #13

Homework #4

Due Mon. May 14, 2007

1. In this problem, we study the effect of nonidealities on the performance of a two-step 10-bit ADC (with 5 bits resolved in each stage). For each of the following errors, explain how the input/output characteristic of the ADC is affected and demonstrate using proper plots (e.g. residue plots, input/output plots, etc.).

(a) Comparator A_j in the first stage has an offset voltage of $+1.3$ LSB.

(b) The reference ladder of the first stage has an INL of $+0.7$ LSB at its midpoint.

(c) The DAC has an offset voltage of $+0.8$ LSB.

(d) The DAC has a gain error of $+0.04\%$.

(e) The DAC has a DNL of $+1.3$ LSB.

(f) The DAC has an INL of $+1.4$ LSB.

(g) The subtractor has an offset of $+1.7$ LSB.

(h) The subtractor has a gain error $+0.9\%$.

(i) The subtractor has an INL of $+1.5$ LSB.

(j) Suppose the subtractor has a nominal voltage gain of 8. What should the full-scale voltage of the second stage be (in LSB)? How much error can we tolerate in the gain of the subtractor or the full-scale voltage of the second stage if DNL is to remain below 0.2 LSB? How much comparator offset is allowed in the second stage?

2. Design an 8-bit folding and interpolating ADC. Consider two cases:

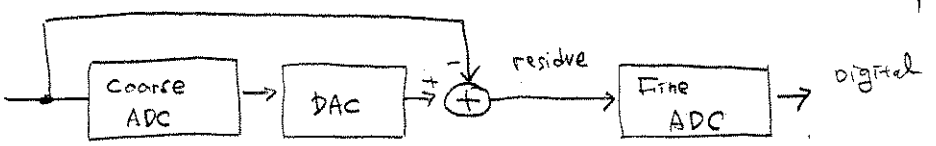
(a) The analog input can be loaded by at most 16 differential pairs.

(b) The analog input can be loaded by at most 32 differential pairs.

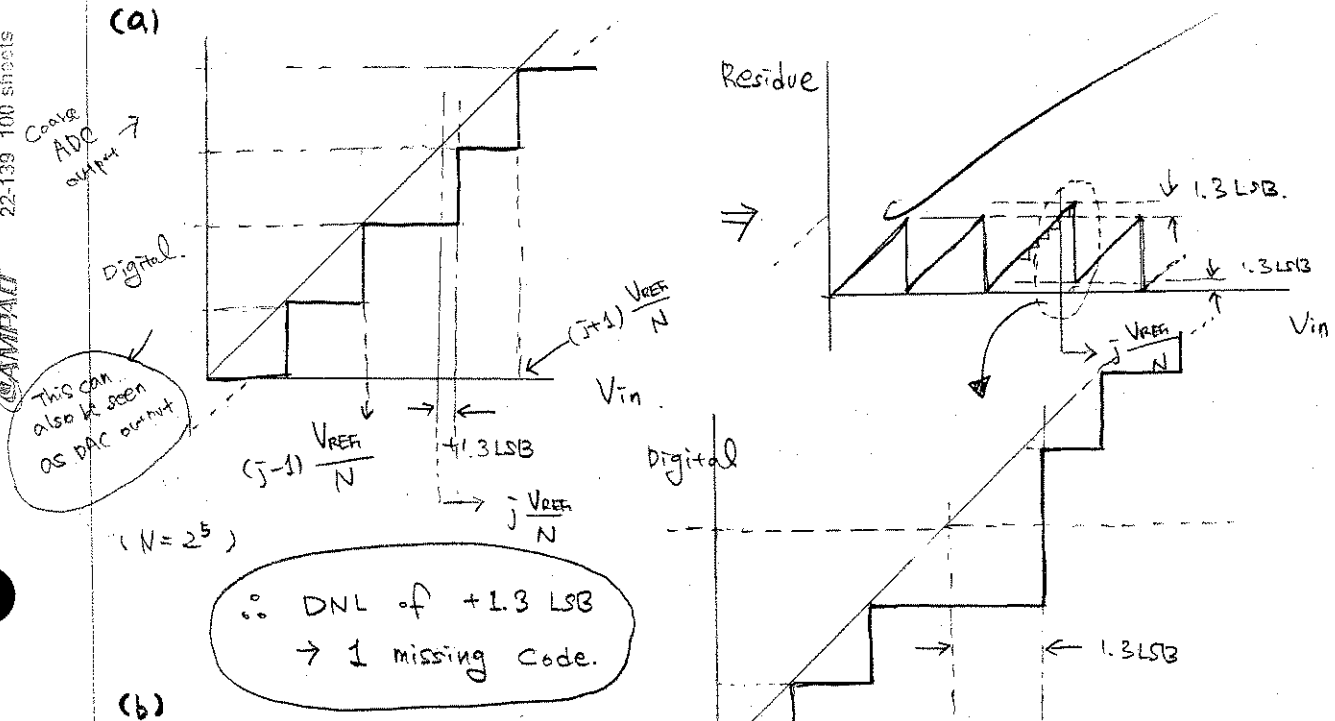
(Assume the input stage of each comparator requires a differential pair.) Provide a diagram similar to that of the 6-bit example in the lecture notes for each case, but also show the interpolation network in detail. Summarize the hardware requirements in two tables, showing the total number of differential pairs, comparators, and resistors for each case. (You need not count the load resistors used in the differential pairs.)

100/100

1. A two step 10 bit ADC. (5bits/5bits)

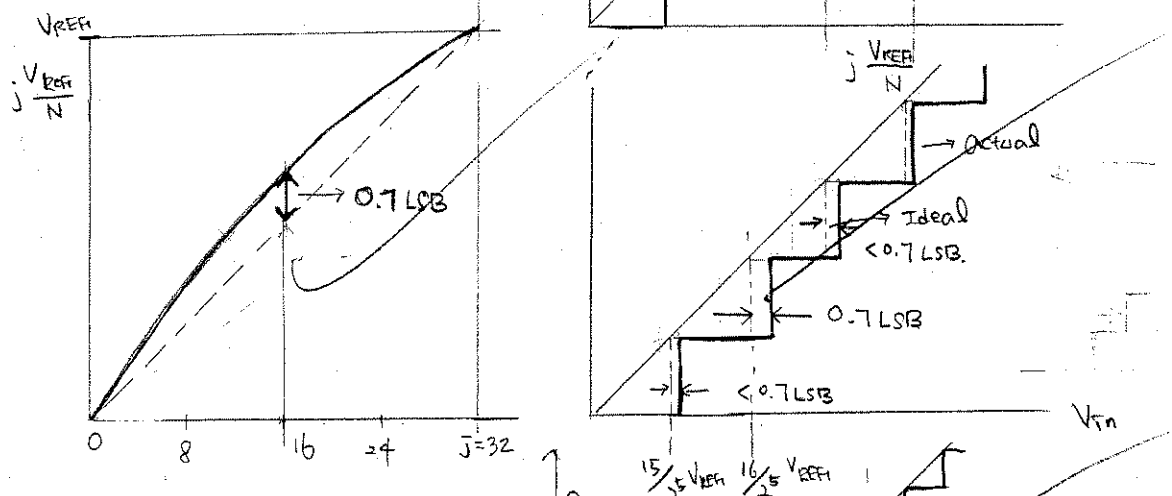


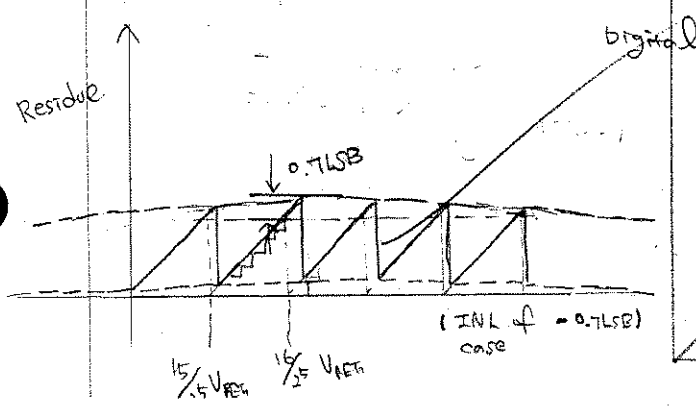
(a)

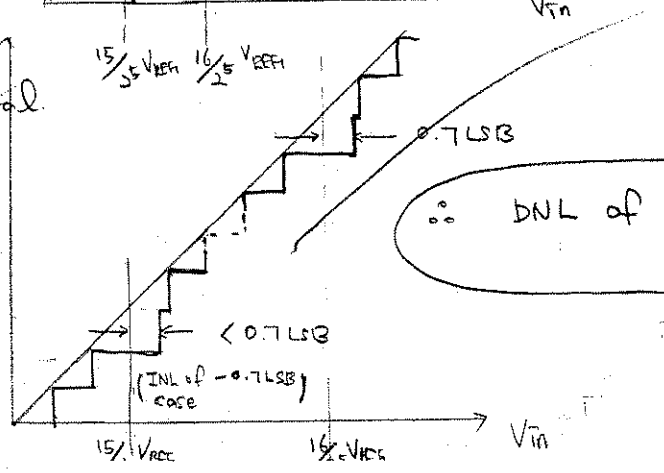


∴ DNL of +1.3 LSB → 1 missing code.

(b)

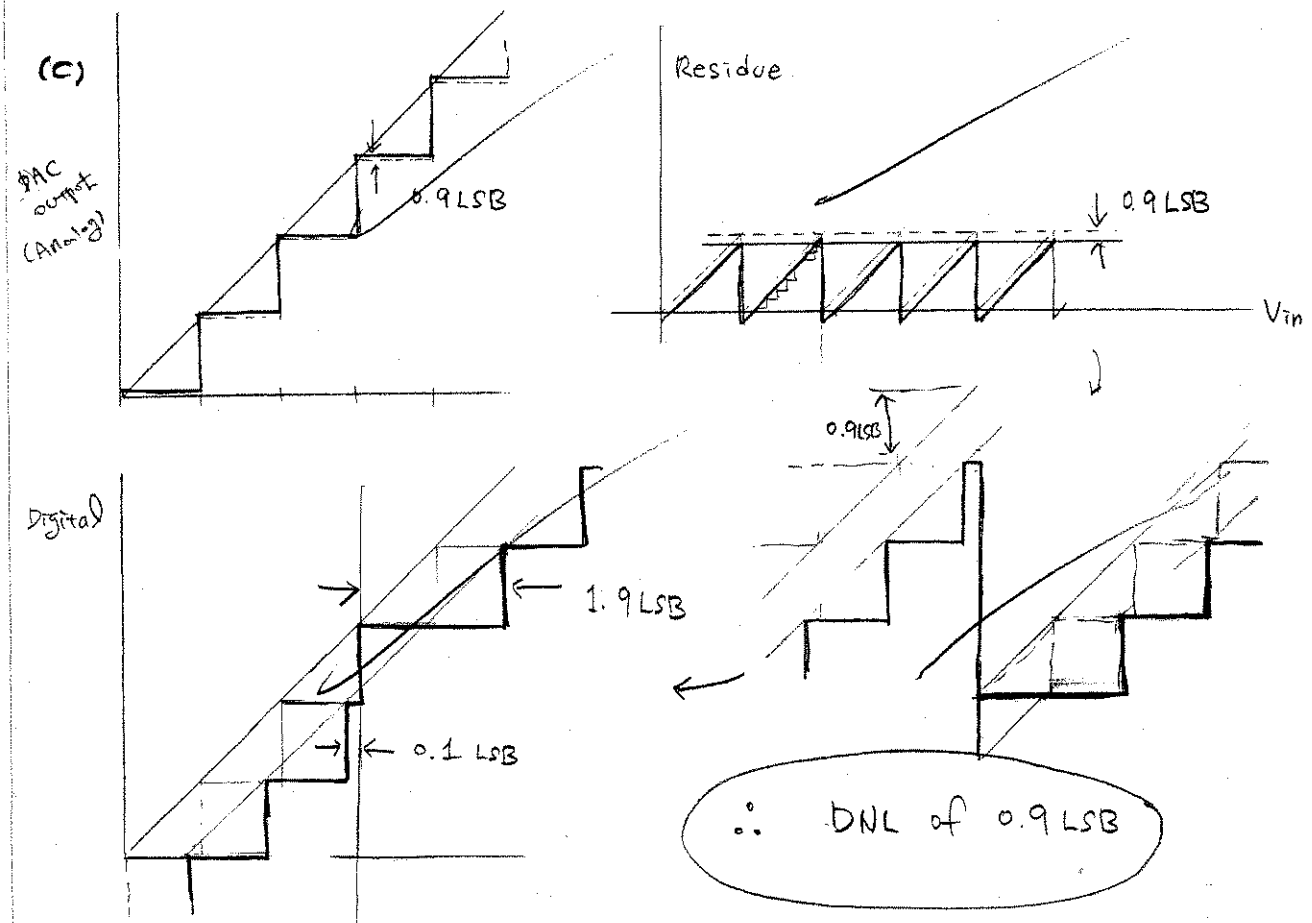






∴ DNL of +0.7 LSB

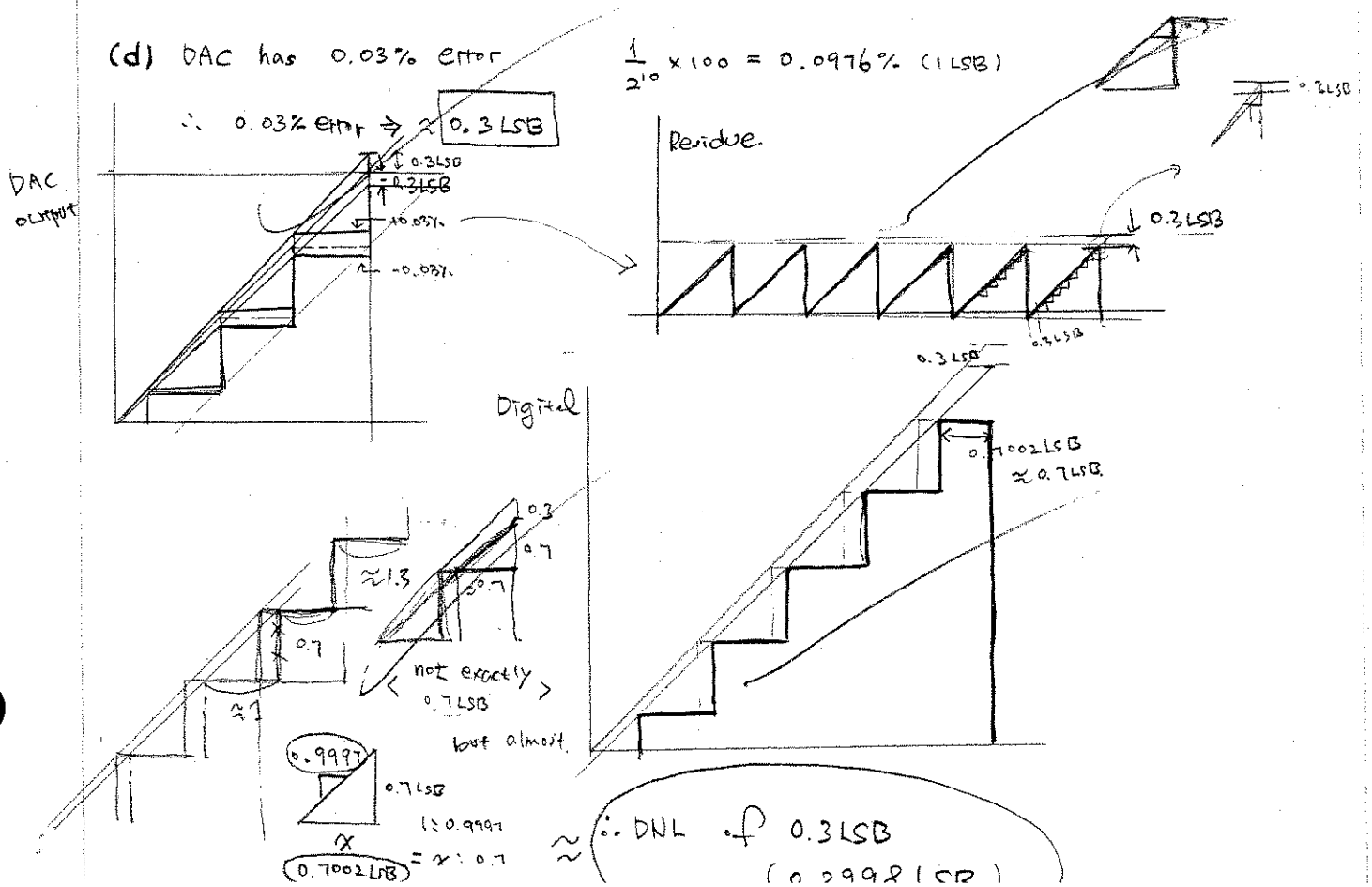
(c)



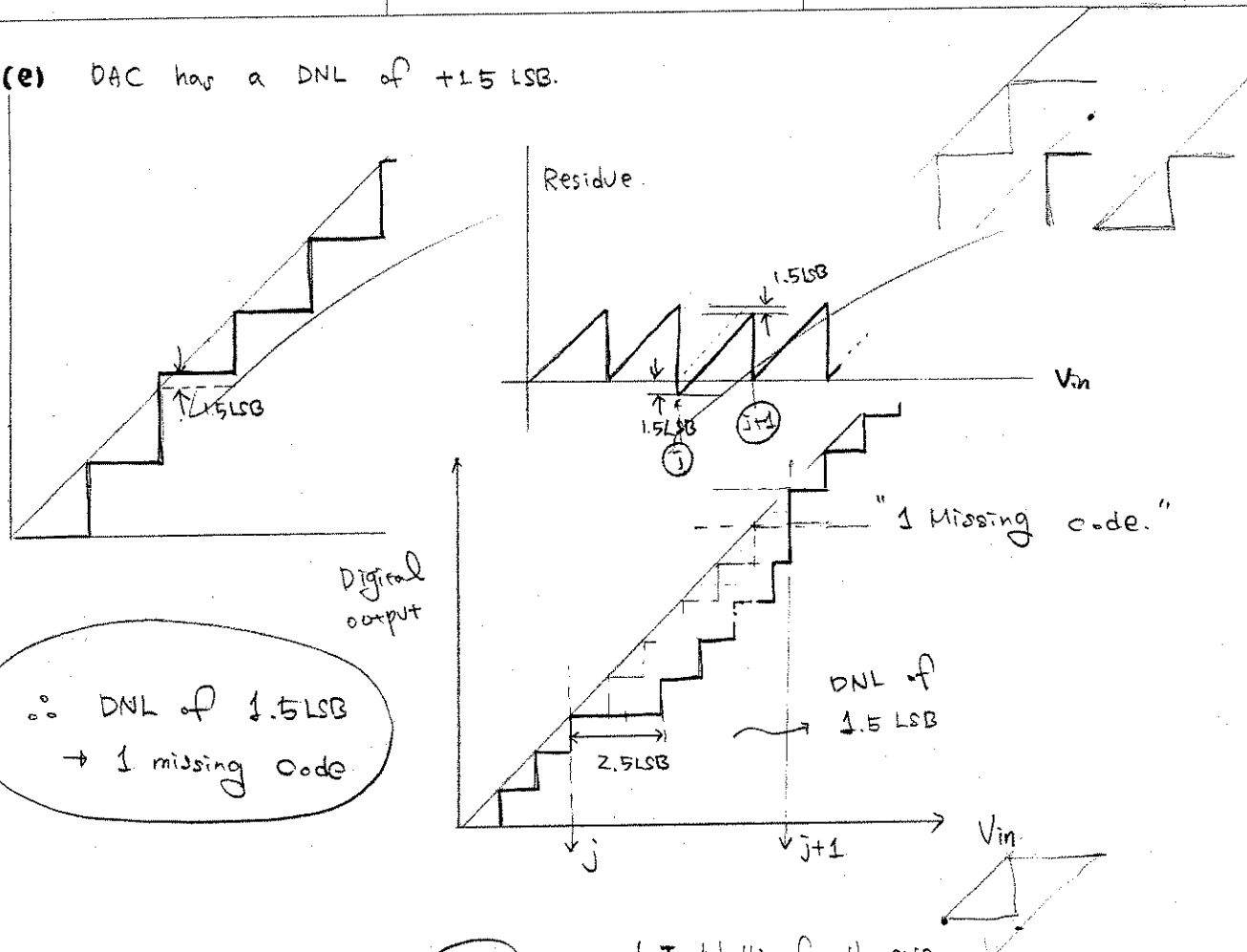
(d) DAC has 0.03% error

$\therefore$ 0.03% error $\Rightarrow \approx$ 0.3 LSB

$\frac{1}{2^{10}} \times 100 = 0.0976\%$ (1 LSB)

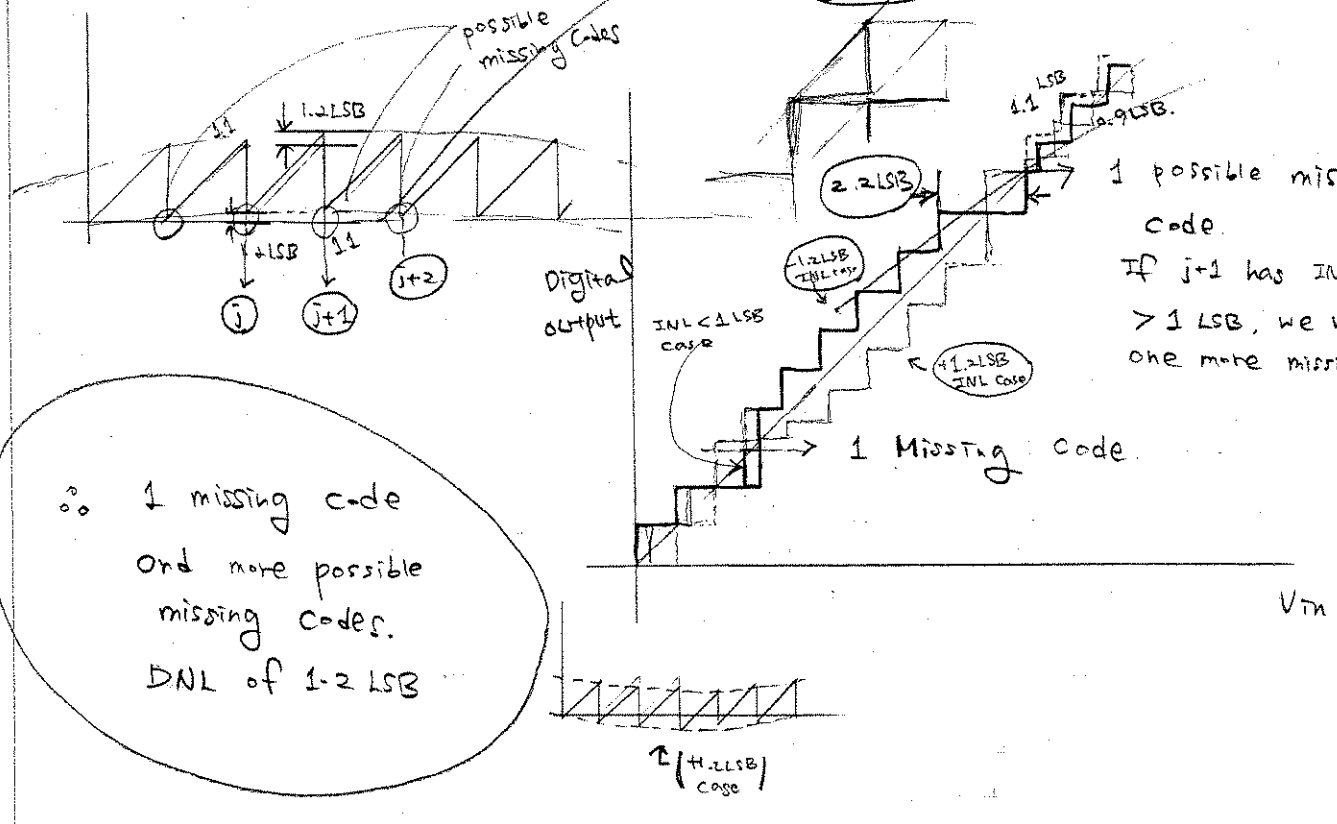


(e) DAC has a DNL of +1.5 LSB.



∴ DNL of 1.5LSB → 1 missing code

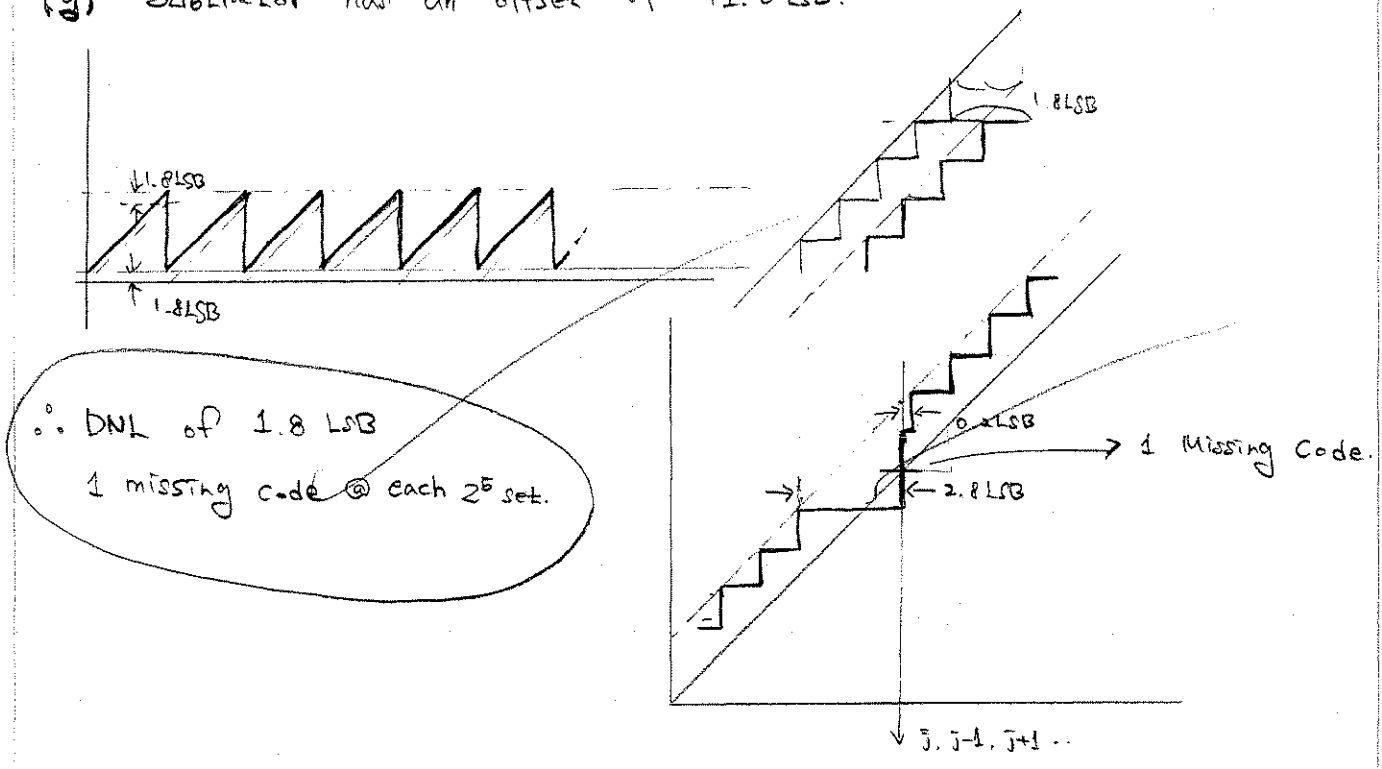
(f) DAC has a INL of ~~+1.2~~ −1.2 LSB. (I did this for the case of −1.2LSB INL, and the result will be very similar.)



If j+1 has INL of > 1 LSB, we will have one more missing code

∴ 1 missing code and more possible missing codes. DNL of 1.2 LSB

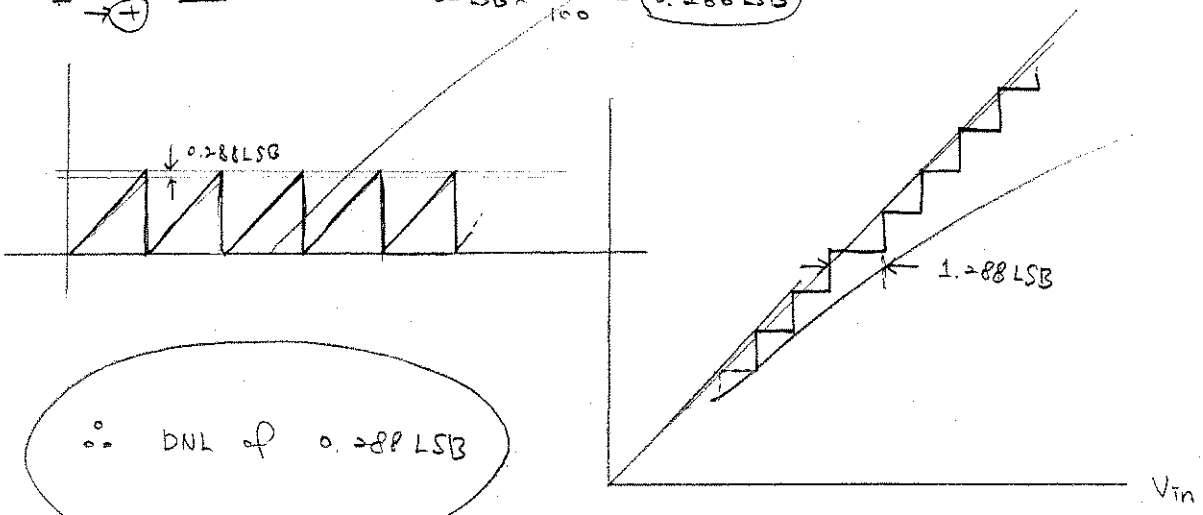
(g) Subtractor has an offset of +1.8 LSB.



∴ DNL of 1.8 LSB
1 missing code @ each 2^5 set.

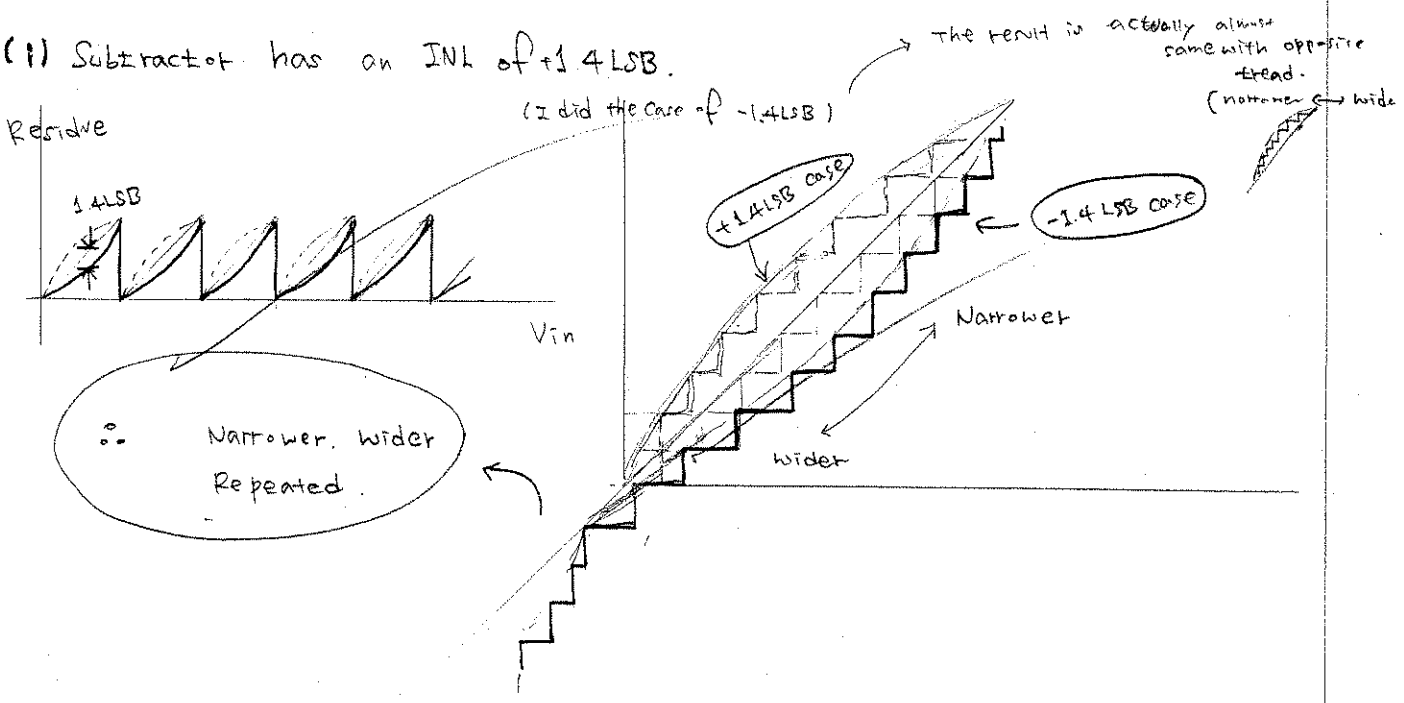
(h) Subtractor has a gain error +0.9%

$32\,LSB \times \frac{0.9}{100} = 0.288\,LSB$

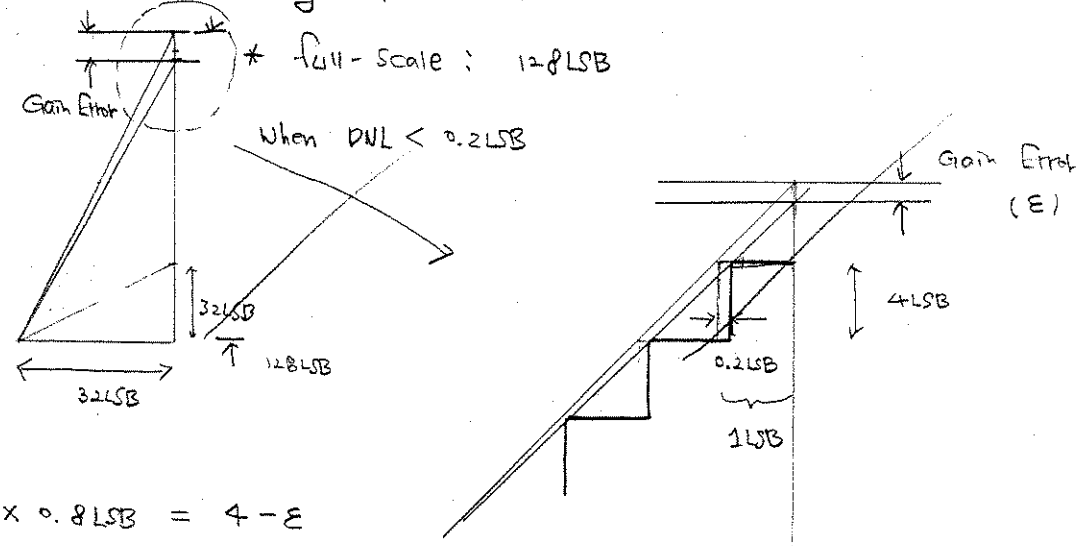


∴ DNL of 0.288 LSB

(i) Subtractor has an INL of ±1.4LSB.



(j) Subtractor : Nominal gain 4



$$\frac{128-\varepsilon}{32} \times 0.8\,\text{LSB} = 4-\varepsilon$$

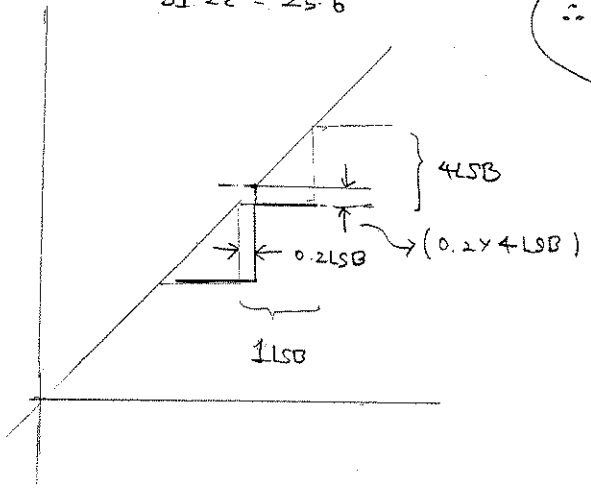
$$102.4 - 0.8\varepsilon = 128 - 32\varepsilon$$

$$31.2\varepsilon = 25.6$$

$$\varepsilon \simeq 0.82\ \text{LSB}$$

∴ Gain Error = $\frac{0.82\text{LSB}}{128\text{LSB}} \times 100 \simeq 0.64\,\%$

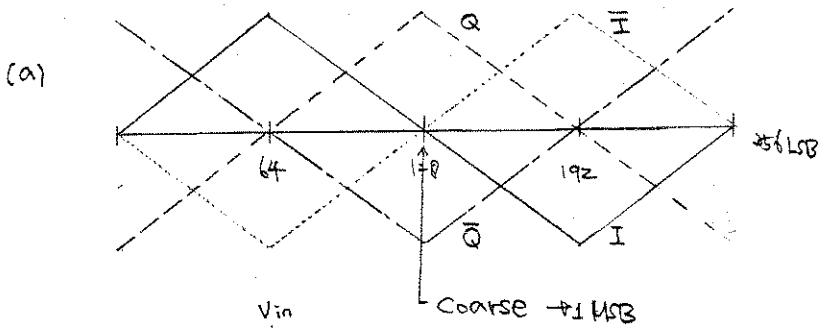
Full Scale = 127.18LSB



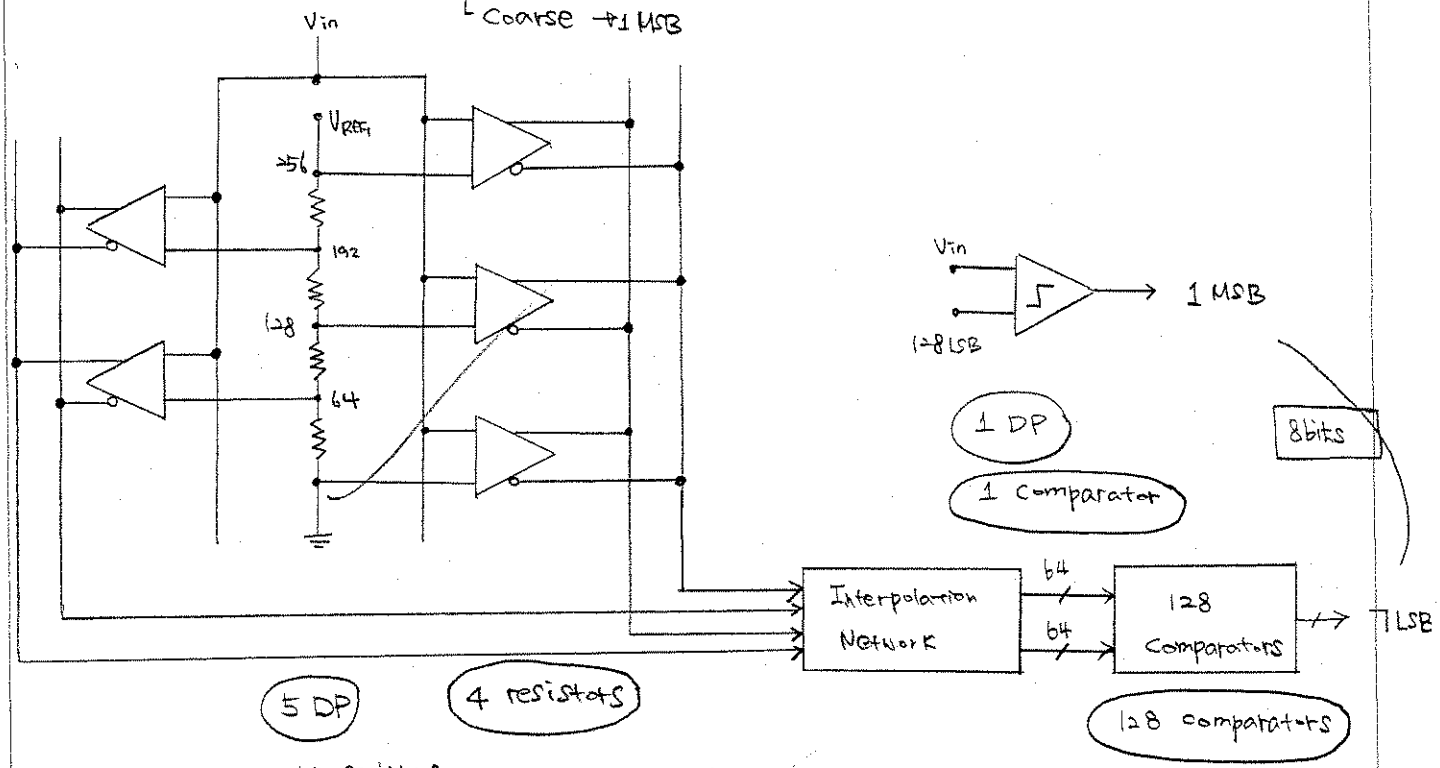
∴ 0.8 LSB offset is allowed.

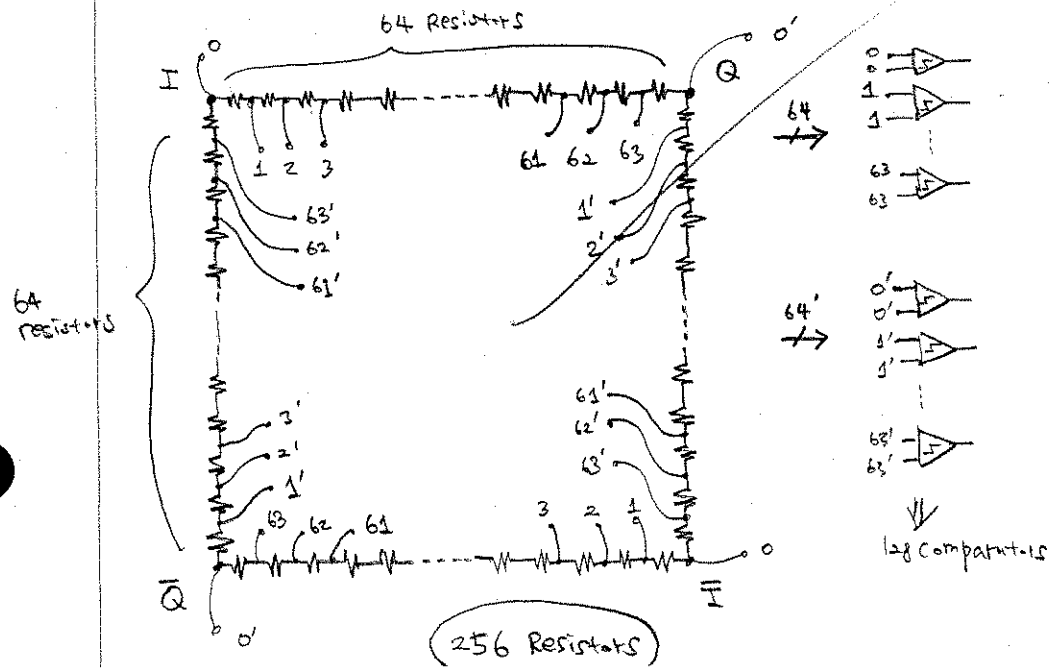
2. 8-bit folding and interpolating ADC.

(a) At most 8 differential pairs.



8bit → ±56 LSB.

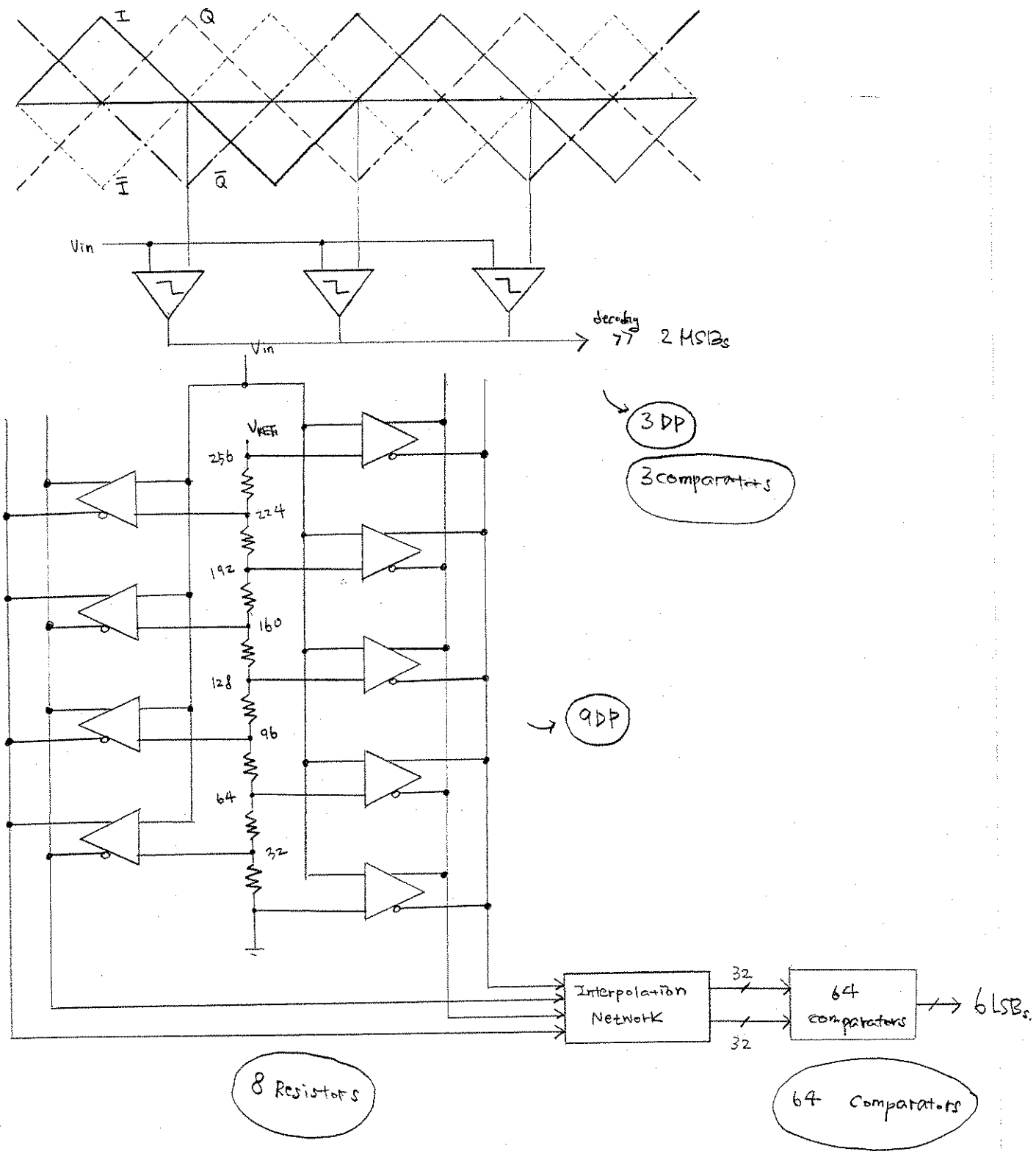


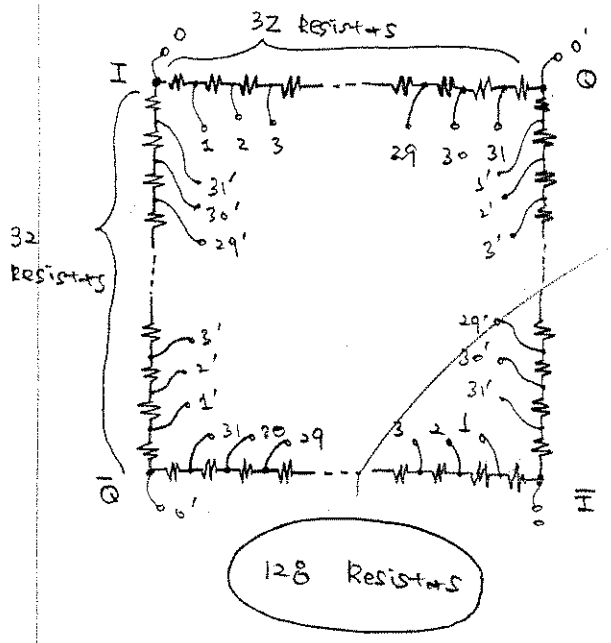


6 Differential Pairs
129 Comparators
260 Resistors

* Assumed the comparator for 1 MSB also has a differential pair.

(b) At most 16 differential pairs.





∴ 12 Differential Pairs

67 comparators

136 Resistors.

※ Summary

	DP	Comparators	Resistors
(a)	6	129	260
(b)	12	67	136