Introduction to Data Conversion

Why This Course?

- Data conversion is difficult;
- Data converters have a huge market;
- The demand for higher performance in data converters keeps growing;
- Cost issues make it desirable to build data converters in mainstream VLSI technologies rather than dedicated “analog” processes. This creates more difficulties in the design.

Why is data conversion difficult?

- Fundamental Trade-offs;
  
  Digital Circuits  Analog Circuits
  
- Data converters operate with “large” signals => traditional small-signal analysis techniques are not valid here;
- Data converters include both analog and digital circuits (and hence belong to the “mixed-signal” family). Thus, they must deal with noise coupling issues: supply coupling, line-to-line coupling, substrate coupling:

- Data converters are difficult to simulate. These circuits often have several thousand devices => their simulation with SPICE is extremely time consuming (hours or days), and sometimes impossible (convergence problems, etc.).

Applications of Data Converters

Any system where digital computing, processing, storage, or transmission of analog information is advantageous:

- consumer electronics (CD players, camcorders, etc.)
- medical imaging, speech processing, instrumentation, high-definition TV, communications, wireless, radar, neural recording.

Example: Neural Recording

Example: RF Receiver

The noise floor, linearity, speed, and power of the ADC become crucial here.

Example: Digital Camera
Examples of State of the Art

14-bit, 100-MHz CMOS ADC
Bogner, ISSCC 06
Power Diss.: 224 mW

5-bit, 22-GHz SiGe ADC
Schvan, ISSCC 06
Power Diss.: 3 W

Universal Figure of Merit for Data Converters:

Basic Concepts in Analog Design

- Linearity
  \[ x_1(t) \rightarrow y_1(t) \]
  \[ x_2(t) \rightarrow y_2(t) \]
  \[ \Rightarrow ax_1(t) + bx_2(t) \rightarrow ay_1(t) + by_2(t) \]

Is this system linear?

How about this?

Linear as long as input is defined as only 00, 01, 10, 11 digital inputs

I/O Characteristic:
Harmonic Distortion: If a sinusoidal waveform is corrupted by components that are harmonically related to it, we say it has harmonic distortion:

\[ x(t) = A \sin(\omega t) \Rightarrow y(t) = A_1 \sin(\omega t + \theta_1) + A_2 \sin(2\omega t + \theta_2) + \ldots \]

Nonlinearity introduces harmonic distortion:

Mathematically, if \[ y = a_1x + a_2 x^2 + \ldots \]

Then: \[ y(t) = a_1 A \sin(\omega t) + a_2 A^2 \sin^2(\omega t) + \ldots \]

\[ \sin^2(\omega t) = \frac{1 - \cos(2\omega t)}{2} \]

Does every kind of nonlinearity cause harmonic distortion?

- Differential vs. Single-Ended Operation

A single-ended signal is taken with respect to a fixed potential (usually ground):

A differential signal is taken between two modes that have equal and opposite signals with respect to a common-mode voltage and also equal impedances to a fixed potential (usually ground):

Advantages of Differential Operation:

- Rejection of common-mode effects such as supply and substrate noise;
- High immunity to coupling and feedthrough from other signals;
- Maximum voltage swing is twice that in single-ended operation (for a given supply voltage);
- Even-order harmonics are absent:

- A sin(\omega t) \Rightarrow a_1 A \sin(\omega t) + a_2 A^2 \sin^2(\omega t) + \ldots
- A \sin(\omega t) \Rightarrow -a_1 A \sin(\omega t) + a_2 A^2 \sin^2(\omega t) - a_3 A^3 \sin^3(\omega t) + \ldots

\[ \Rightarrow \text{Differential Output} = 2 a_1 A \sin(\omega t) + 2a_3 A^3 \sin^3(\omega t) + \ldots \]

- A given swing can be obtained at \sim \text{half the delay}:

- Biasing is easier.
Disadvantages:
- Random noise (thermal, shot,...) is due to more devices and is higher;
- Routing twice as many signals may be difficult;
- Testing may be more difficult;
- Current source consumes some voltage.

- Dynamic Range

Dynamic range is loosely defined as

\[
DR = \frac{\text{Maximum allowable signal}}{\text{Minimum resolvable signal}}
\]

The maximum allowable swing is limited by the supply voltage and the circuit topology. The minimum resolvable signal is limited by noise and/or offset.

- Precision & Accuracy

These two terms have been so overused that they have lost their true meaning. To avoid any confusion, we will not use either of these two. We define a set of self-sufficient and consistent parameters later that carries all the "precision" and "accuracy" information.

General Concepts

<table>
<thead>
<tr>
<th>Analog</th>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous – Amplitude</td>
<td>Discrete – Amplitude</td>
</tr>
<tr>
<td>Continuous – Time</td>
<td>Discrete – Time</td>
</tr>
</tbody>
</table>

A/D Conversion

LPF:

Sampling:

Quantization:

Decoding:

The ratio of \( f_s \) and the input signal bandwidth, \( BW_{in} \), determines the type of converter:
- “Nyquist Rate” ADCs employ \( f_s \geq 2BW_{in} \)
- “Oversampled” ADCs employ \( f_s \gg 2BW_{in} \)
  (typically, \( f_s = 8 BW_{in} \Rightarrow 64 BW_{in} \))

D/A Conversion
Basic Sampling Circuits

**Sampling Schemes**

- **Ideal**
  - Difficult to generate impulses;
  - Following circuits require nonzero duration.

- **Zero-Order Hold**
  - This waveform too has a sinc envelope in the frequency domain.
  - How can a track-and-hold provide discrete-time data?

**Important conclusion:** The above combination operates as an ideal sampler. The sinc envelope is inconsequential here.

**Simple Sampling Circuit**

- Draws transient currents from input;
- Is susceptible to currents drawn at output.
Performance Metrics

- Acquisition Time, $t_{acq}$, is the time after the sampling command required for the SHA output to experience a full-scale transition and settle within a specified error band around its final value.

- Hold Settling Time, $t_{hs}$, is the time after the hold command required for the SHA output to settle within a specified error band around its final value.

- Pedestal Error is the error introduced at the SHA output during the transition from sample to hold.

- Droop Rate is the rate of discharge of the capacitor during the hold mode.

- Hold-Mode Feedthrough is the percentage of the input signal that appears at the output during the hold mode.

- Signal-to-(Noise + Distortion) Ratio (SNDR)

$$\text{SNDR} = \frac{\text{Signal Power at output}}{\text{Noise Power + Dist. Power at output}}$$

- Clock jitter is the random variation in the zero crossings (or period) of the clock.