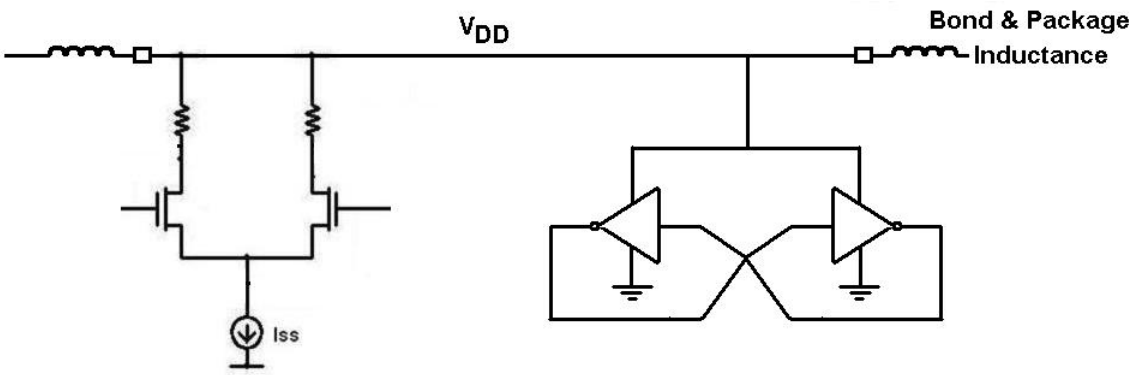
# Layout Considerations

## Basic Issues

- **Analog vs. Digital Supplies**

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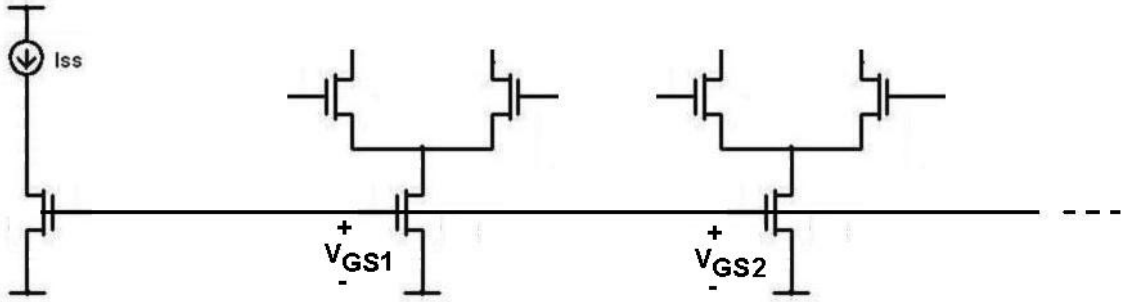
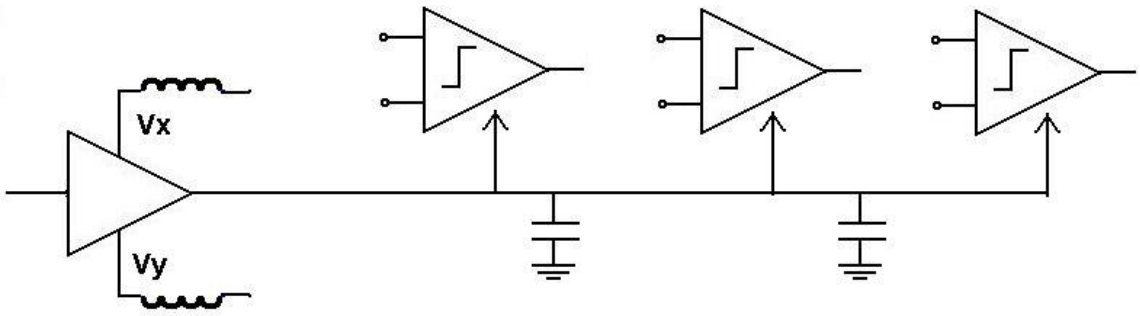
- **DC Voltage Drops**

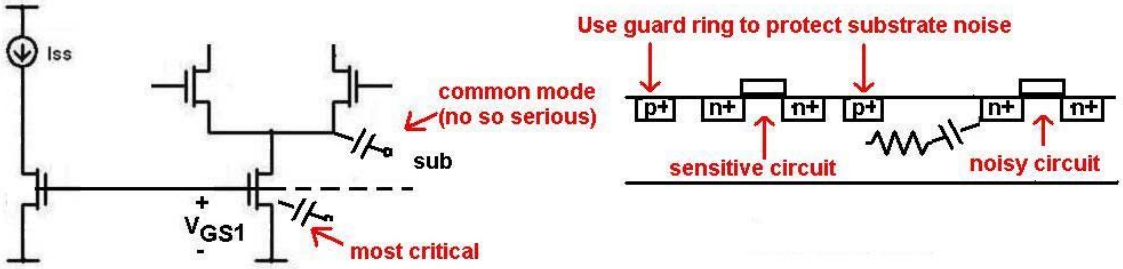



**e.g. for 1mm long wire (i.e. 100 sq) and 50mΩ/sq,**
**this corresponds to: Resistance = 5Ω**

- **- Bond Wires & Device Capacitances**

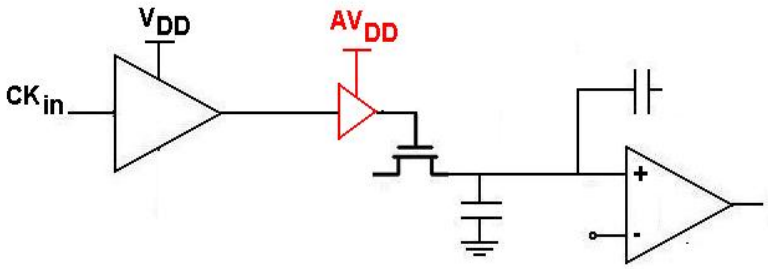


**-Substrate Coupling**




**Different arguments for connecting substrate to analog ground and digital ground. Not clear. But the best way is to have a low-inductance connection to substrate.**

- **Clock Noise Coupling**




**Local buffer (AVdd)**

**Need a clean buffer.**

## Layout of MOS Devices

- **Multi-Finger Structures**

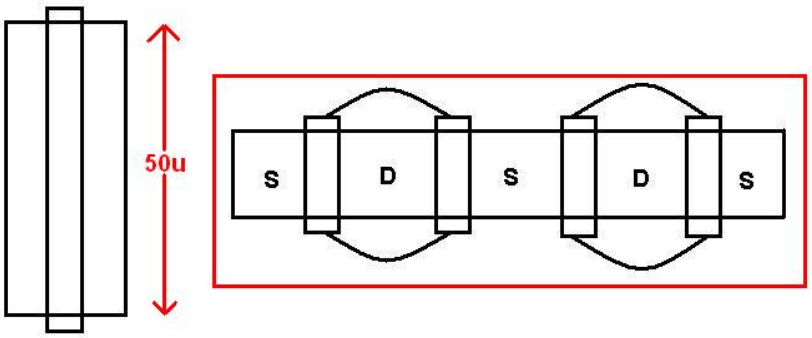
**Slicided poly**

**RD = 8~10Ω**

**e.g. with 0.13-umtech,**

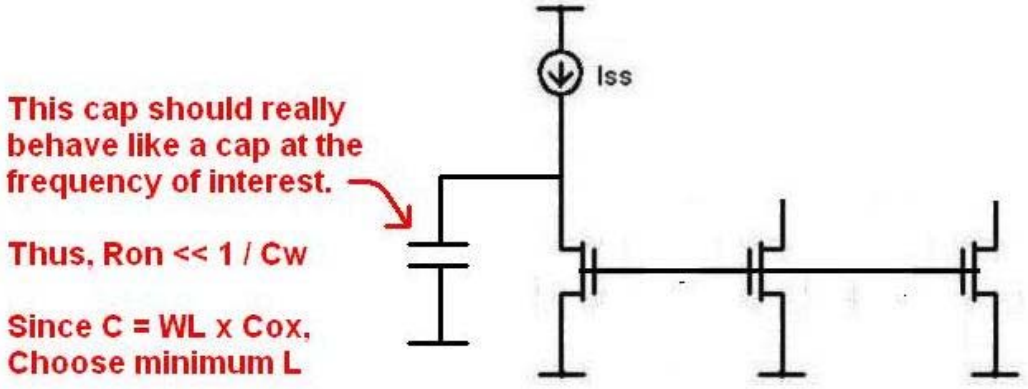
**gate = 360□ x 10**

**= 3.6k**



- **MOS Devices Used as Capacitors**

**Do not use if linearity of capacitor is important. Good for bypassing:**

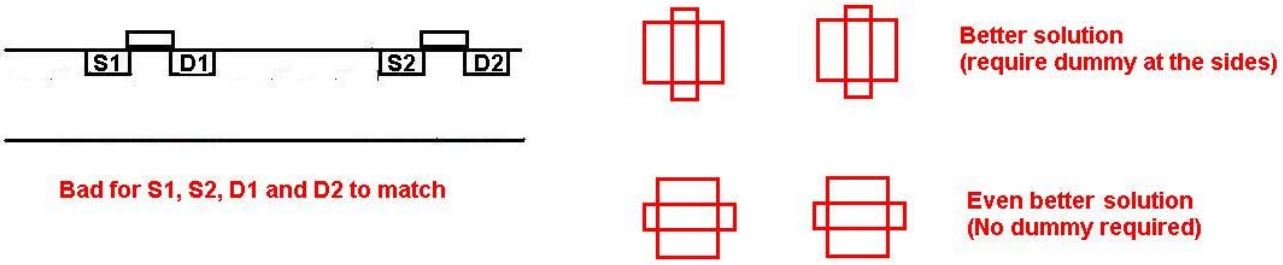



**But must make sure on-resistance is sufficiently small (Q is high.)**

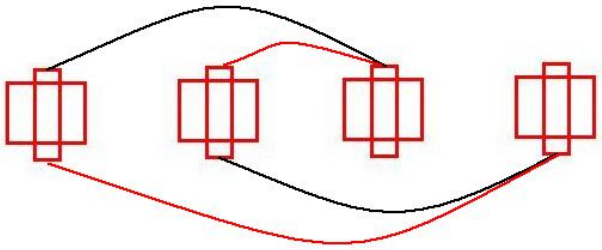
- **Measure on-resistance for given gate voltage.**
- **Divide the value by 12.**

**Sometimes deliberately choose a low Q to dampen ringing due to bond wire inductance.**

- **Matched MOS structures**
  - **Use same orientation**
  - **Account for asymmetries due to nonvertical implants:**



- **Make the surroundings of transistors the same.**
- **Cross connect to cancel gradients.**



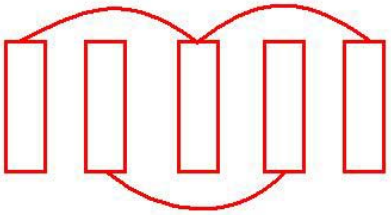
**Which connection (red or black) is less sensitive to mismatch?**

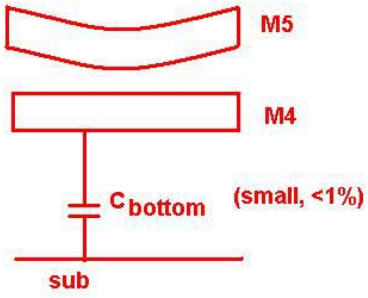
## Capacitors

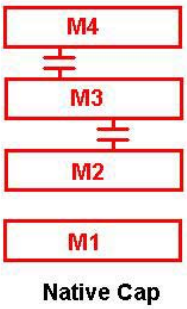
**Poly-Diffusion**

**Metal-Poly**

**"Native Caps"**



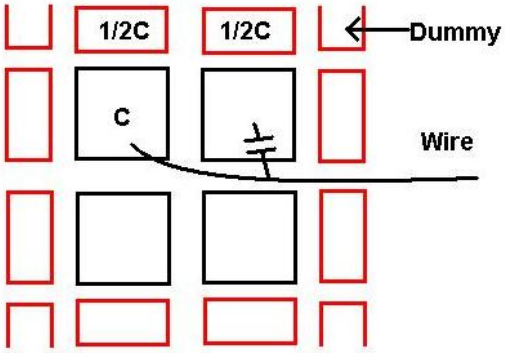



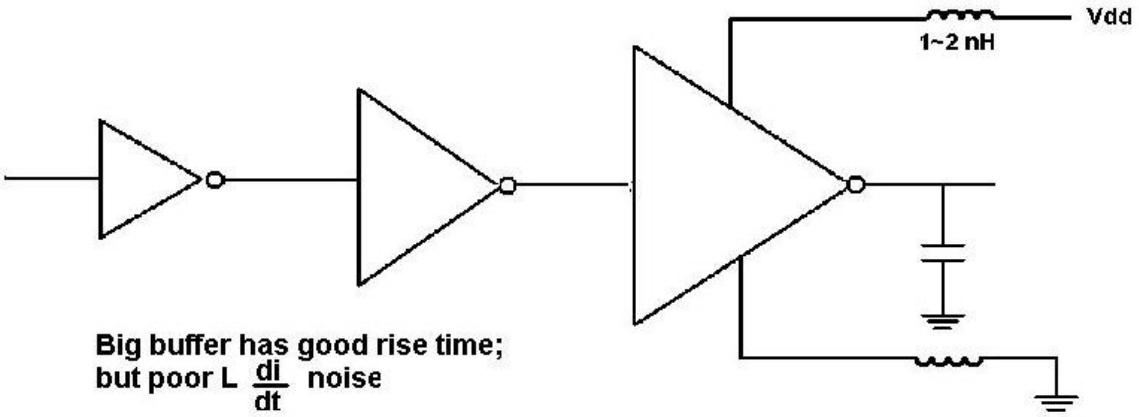

**Issues:**

**Nonlinearity, matching, temp. coefficient, bottom- and top-plate parasitics, series resistance, contact placement**

## Matched Caps



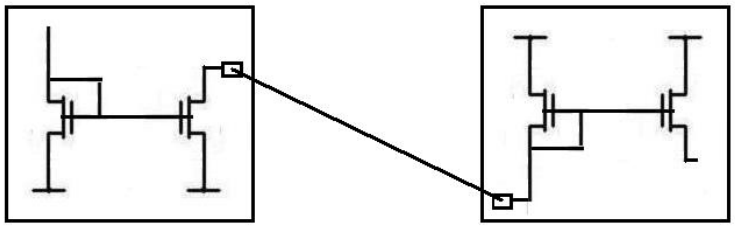
## Output Drivers & Clock Buffers



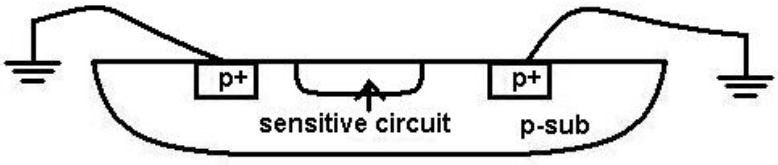

Need to simulate with bond wire inductance to Vdd

- **Don't make the driver too large!**
- **If possible, make the driver differential.**
- **If possible, reduce the output swing.**

**In a fully custom-designed system, we can try to route currents rather than voltages.**



## Guard Rings



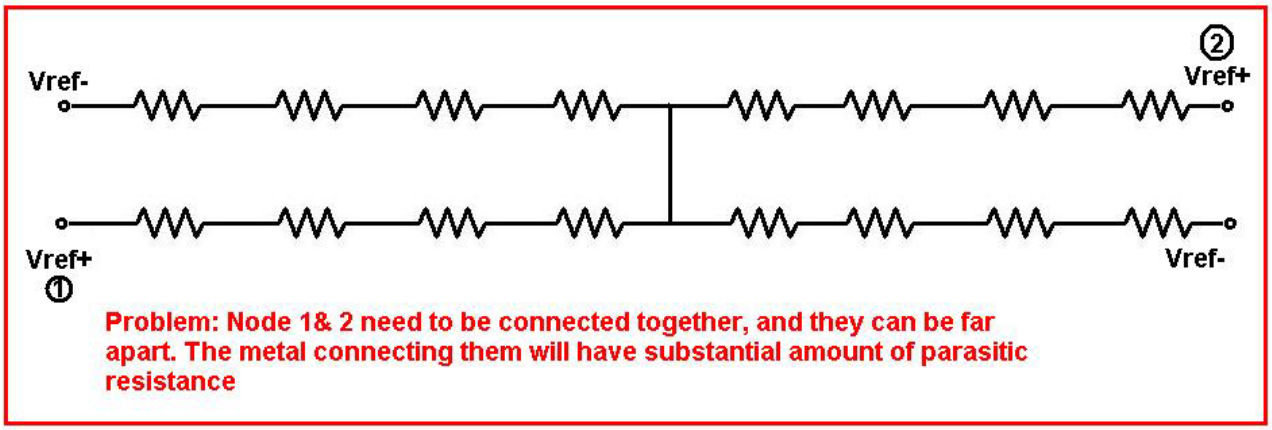

**Guard ring can be N+, P+ or N-well**

**Can do the same in n-well. It is also believed that guard rings improve matching as well.**

**In most modern CMOS technologies, the substrate has a low resisitivity. As a result, the distance between analog and digital blocks has little effect on the amount of coupled noise.**

## Miscellaneous

- **Resistor Ladder Layout**




- **Coupling through Bias Line**