EE 215D

Final Exam

Spring 2007

Name: Solutions

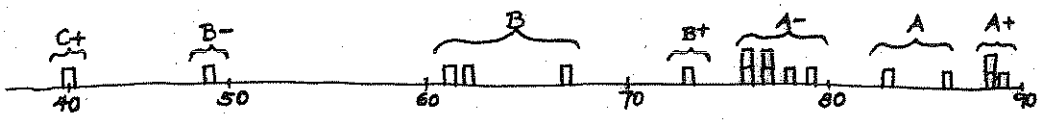
Time Limit: 3 Hours

Open Book, Open Notes

1. 10
2. 10
3. 15
4. 15
5. 10

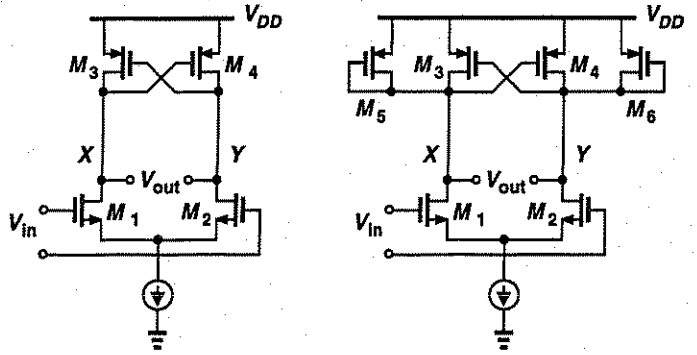
Total: 60

Course Grade Distribution

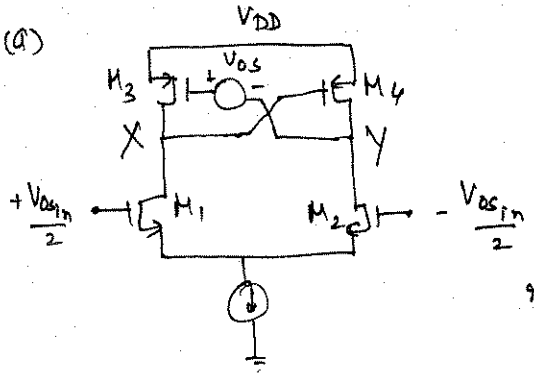


1. (a) Consider the circuit shown on the left and assume M_3 and M_4 exhibit an offset voltage of V_{OS1}. Determine the input-referred offset voltage of the circuit. Assume $\lambda \neq 0$. What happens if $\lambda \to 0$?

(b) Repeat part (a) for the circuit shown on the right and denote the mismatch between M_5 and M_6 by V_{OS2}. Assume $\lambda = 0$.

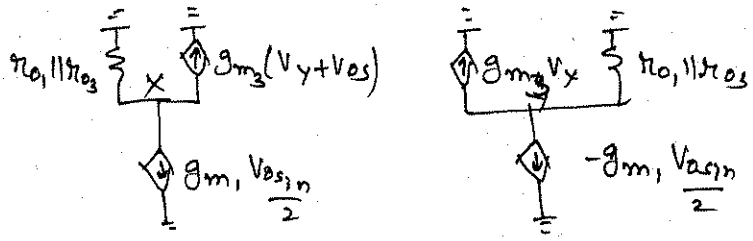


(a)



For zero offset $V_x = V_y$

Small signal mode



* $\frac{V_{os_{in}}}{2}$ → Input referred offset

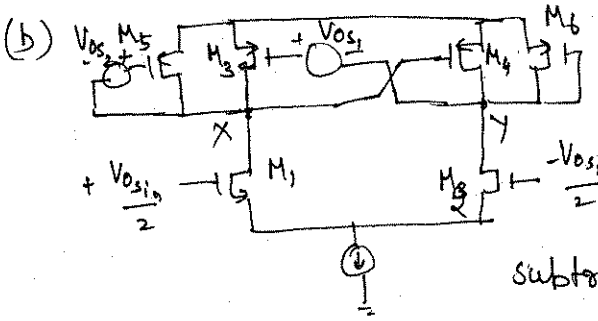
Apply KCL at X and Y.

$$g_{m_1}\frac{V_{os_{in}}}{2} + \frac{V_x}{r_{o_1}\|r_{o_3}} + g_{m_3}(V_y+V_{os}) = 0 \quad -(1)$$

$$-g_{m_1}\frac{V_{os_{in}}}{2} + \frac{V_x}{r_{o_1}\|r_{o_3}} + g_{m_3}V_x = 0 \quad -(2)$$

Subtracting (2) from (1) $\Rightarrow$ $V_{os_{in}} = \left|\frac{g_{m_3}V_{os}}{g_{m_1}}\right|$ (independent of λ)

(b)



In a similar fashion, apply KCL at x and y

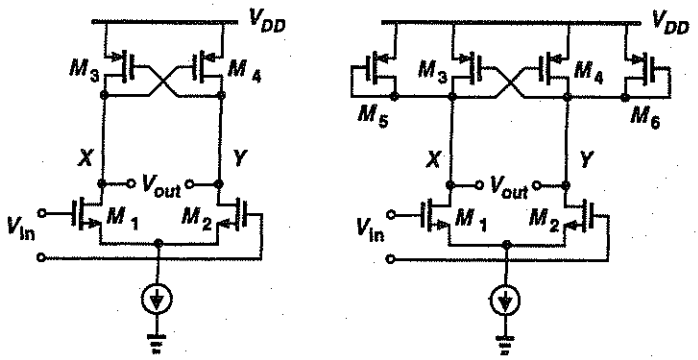
$$g_{m_1}\frac{V_{os_{in}}}{2} + g_{m_5}(V_x+V_{os_2}) + g_{m_3}(V_x+V_{os_1}) = 0 \quad -(1)$$

$$-g_m\frac{V_{os_{in}}}{2} + g_{m_5}V_x + g_{m_3}V_x = 0 \quad -(2)$$

Subtracting (2) from (1)

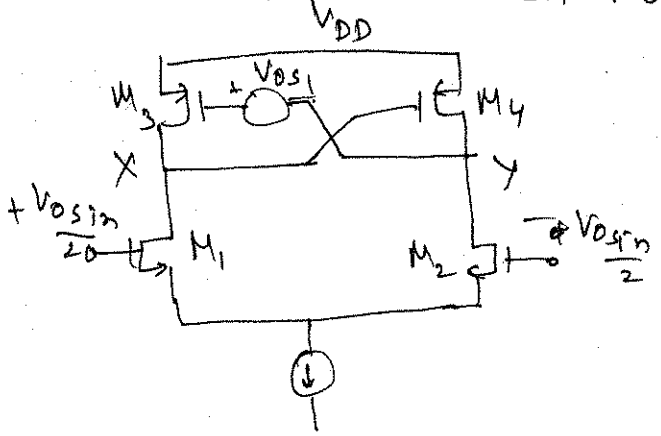
$$V_{os_{in}} = \frac{g_{m_5}V_{os_2} + g_{m_3}V_{os_1}}{g_m}$$

1. (a) Consider the circuit shown on the left and assume M_3 and M_4 exhibit an offset voltage of V_{OS1}. Determine the input-referred offset voltage of the circuit. Assume $\lambda \neq 0$. What happens if $\lambda \to 0$?
(b) Repeat part (a) for the circuit shown on the right and denote the mismatch between M_5 and M_6 by V_{OS2}. Assume $\lambda = 0$.



Alternative solution for (a):

Since the circuit regenerates, the offset voltage referred to input is such that M_3 and M_4 carry equal current



i.e Find $V_{OS_{in}}$ such that

$$V_X = V_Y + V_{OS_1}$$

Applying KCL at X and Y

$$g_{m_1}\frac{V_{OSin}}{2} + \frac{V_X}{R_o} + g_{m_3}(V_Y + V_{OS_1}) = 0 \quad -(1)$$

$$-g_{m_1}\frac{V_{OSin}}{2} + \frac{V_Y}{R_o} + g_{m_3}\cdot V_X = 0 \quad -(2)$$

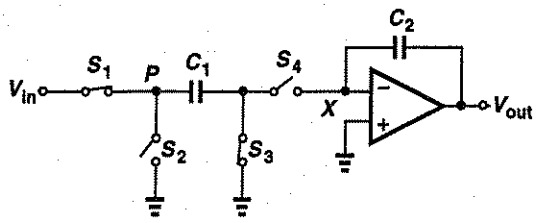
where $R_o = r_{o_1} \| r_{o_3}$

Subtracting (2) from (1) and since $V_X = V_Y + V_{OS_1}$

$$g_{m_1} V_{OSin} = -\frac{V_{OS_1}}{R_o}$$

$$\Rightarrow \boxed{V_{OSin} = \left|\frac{V_{OS_1}}{g_m R_o}\right|}$$

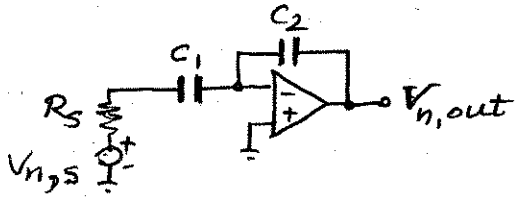
2. We wish to study the kT/C noise behavior of the integrator shown below. Assume the circuit begins with a zero initial condition across C_2. Calculate the total kT/C noise at the output in the integration mode. Assume the op amp is ideal.



- In the sampling mode : $\sqrt{\frac{kT}{C_1}}$ is sampled on C_1.

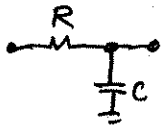
- In the integration mode, $\sqrt{\frac{kT}{C_1}}$ is amplified by a factor of $\frac{C_1}{C_2}$.

Also,



$$\frac{V_{n,out}}{V_{n,s}} = \frac{-\frac{1}{C_2 s}}{R_s + \frac{1}{C_1 s}}$$

$$= \frac{-\frac{C_1}{C_2}}{R_s C_1 s + 1}.$$

Since this network  with $H(s) = \frac{1}{RCs+1}$ exhibits a noise output equal to $\frac{kT}{C}$, we can say $\overline{V_{n,out}^2} = \left(\frac{C_1}{C_2}\right)^2 \cdot \frac{kT}{C_1}$.

Adding the amplified component from the sampling mode and this component, we have

$$\overline{V_{n,tot}^2} = \left(\frac{C_1}{C_2}\right)^2 \frac{kT}{C_1} + \left(\frac{C_1}{C_2}\right)^2 \frac{kT}{C_1}$$

$$= 2\left(\frac{C_1}{C_2}\right)^2 \frac{kT}{C_1}$$

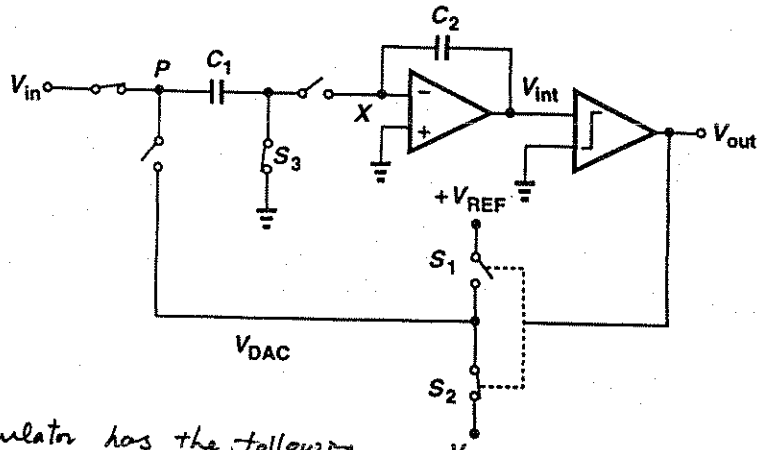
3. Consider the first-order ΣΔ modulator shown below. If $V_{int} < 0$, then the comparator produces $V_{out} = -1$ V and S_2 turns on, producing $V_{DAC} = -V_{REF}$. If $V_{int} > 0$, the reverse occurs. Assume $C_1 = C_2 = C$.

(a) Suppose $V_{in} = V_{REF}/4$ and the initial value of V_{int} is slightly less than zero. Plot V_{int}, V_{out}, and V_{DAC} as a function of time. What is the average value of V_{out}?

(b) Repeat part (a) if $V_{in} = 0.9V_{REF}$.

(c) Repeat parts (a) and (b) if the comparator has a small postive offset voltage, e.g., 5 mV. The positive polarity means V_{int} must be *above* zero by more than 5 mV to switch the comparator.

(d) Repeat parts (a) and (b) if the op amp has a small postive offset voltage, e.g., 5 mV. The postive polarity means that the noninverting input of the op amp is 5 mV above zero.



This Σ-Δ modulator has the following characteristics

$V_{int}[n] = V_{int}[n-1] + (V_{in}[n-1] - V_{DAC}[n-1])$

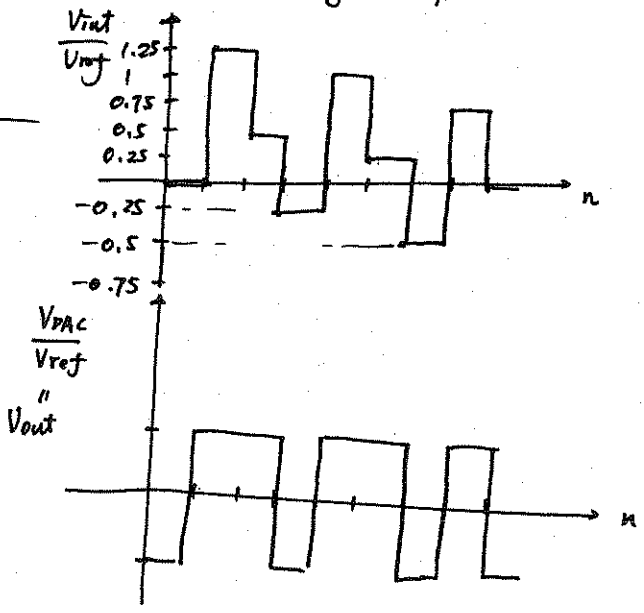
$V_{out}[n] = Sgn(V_{int}[n])$

$V_{DAC}[n] = V_{ref} \cdot V_{out}[n]$

(a) $V_{int}(n=0) = 0^-$, $V_{in} = 0.25\, V_{ref}$

n	V_{in}/V_{ref}	V_{DAC}/V_{ref}	V_{int}/V_{ref}	V_{out}
0	0.25	−1	0^-	−1
1	0.25	1	1.25	1
2	0.25	1	0.5	1
3	0.25	−1	−0.25	−1
4	0.25	1	1	1
5	0.25	1	0.25	1
6	0.25	−1	−0.5	−1
7	0.25	1	0.75	1
8	0.25	−1	0^-	−1

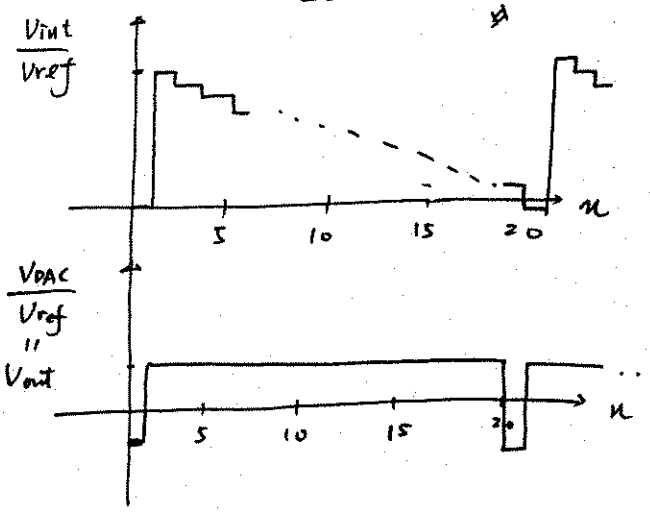
$E[V_{out}] = \frac{5-3}{8} = \frac{1}{4}$



(b) $V_{int}(n=0) = 0^-$, $V_{in} = 0.9\,V_{ref}$

n	V_{in}/V_{ref}	V_{DAC}/V_{ref}	V_{int}/V_{ref}	V_{out}
0	0.9	−1	0−	−1
1	0.9	1	1.9	1
2	0.9	1	1.8	1
⋮	⋮	⋮	⋮	⋮
19	0.9	1	0.1	1
20	0.9	−1	0−	−1

$E[V_{out}] = \frac{19-1}{20} = 0.9$



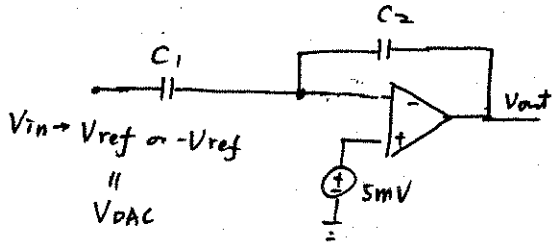
(c)

If the comparator has positive offset 5mV ⇒ the equation associated with the comparator can be written as

$V_{out}[n] = \text{sgn}(V_{int}[n] - 0.005)$

Since $0.1\,V_{ref} >> 0.005$ ⇒ All of the plots in part (a) & (b) don't change

(d) If the OP has positive offset 5mV



$0 = C_2(5mV - V_{o1} - 5mV + V_{o2}) + C_1(5mV - V_{in} - 5mV + V_{DAC})$

$C_2 = C_1 \Rightarrow V_{o2} - V_{o1} = \Delta V_o = V_{in} - V_{DAC}$

Thus, 5mV offset doesn't accumulate.

⇒ All of the plots in part (a) & (b) are the same except V_{int}, which is shifted by >5mV (since the initial value of V_{int} <5mV)

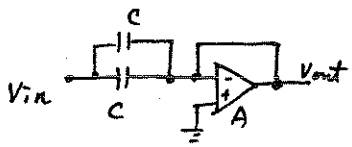
4. Consider the one-bit-per-stage pipelined ADC architecture.

(a) If each op amp has an open-loop gain $A \gg 1$ and an input capacitance C_{in}, calculate the output of the first stage in the pipeline and express it as $(2V_{in} - V_{REF})(1 - \alpha)$, where α denotes the gain error.

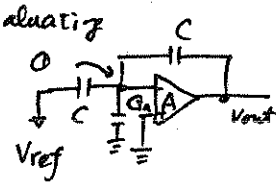
(b) If V_{in} is in the vicinity of $V_{REF}-0.5$ LSB, we expect all stages in the pipeline to produce positive outputs so that the digital output is equal to $11\cdots1$. For this case, derive an expression for the output of the nth stage in the pipeline in terms of V_{in}, V_{REF}, α, and n. [Hint: $1 + x + x^2 + \cdots + x^m = (x^{m+1} - 1)/(x - 1)$.]

(c) Assuming an 8-bit system, determine the output of the eighth stage if $V_{REF} = 1024$ mV, $V_{in} = 1022$ mV, and $\alpha = (256 \times 4)^{-1}$.

(a) Sampling



Evaluating



The total charge change @ Node ① = 0 . Also . $V_1 = -\frac{V_{out}}{A}$

$$\therefore\ C\left(V_{out} - V_{in} + \frac{V_{out}}{A}\right) + C\left(V_{ref} - V_{in} + \frac{V_{out}}{A}\right) + C_{in}\cdot\frac{V_{out}}{A} = 0$$

$$V_{out} = (2V_{in} - V_{ref}) \Big/ \left(1 + \frac{2 + \frac{C_{in}}{C}}{A}\right) \approx (2V_{in} - V_{ref})\left(1 - \frac{2 + \frac{C_{in}}{C}}{A}\right)$$

$$\therefore\ \alpha = \frac{2 + \frac{C_{in}}{C}}{A}$$

(b) The output of 1st stage $= (2V_{in} - V_{ref})(1-\alpha) = 2V_{in}(1-\alpha) - V_{ref}(1-\alpha)$

2nd stage $= [2(2V_{in} - V_{ref})(1-\alpha) - V_{ref}](1-\alpha) = 2^2 V_{in}(1-\alpha)^2 - 2V_{ref}(1-\alpha)^2 - V_{ref}(1-\alpha)$

$\vdots$

$$n^{th}\ \text{stage} = 2^n V_{in}(1-\alpha)^n - 2^{n-1} V_{ref}(1-\alpha)^n - 2^{n-2} V_{ref}(1-\alpha)^{n-1} \cdots - 2^0 \cdot V_{ref}(1-\alpha)$$

$$= V_{in}\cdot 2^n (1-\alpha)^n - \frac{V_{ref}\cdot\left[2^n(1-\alpha)^N - 1\right]\cdot(1-\alpha)}{1 - 2\alpha}$$

(c) $V_{in} = 1022$mV, $V_{ref} = 1024$mV, $n = 8$, $\alpha = \frac{1}{1024}$

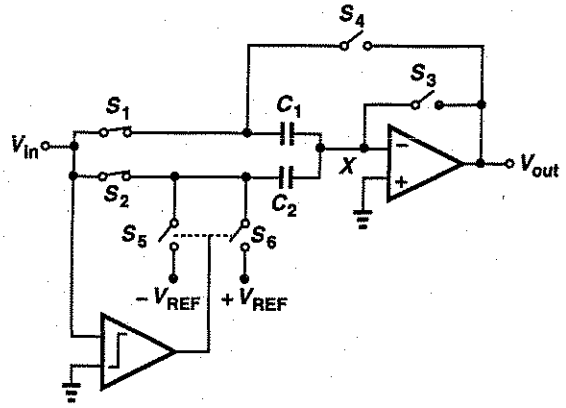
$$V_{out}\ (8^{th}\ \text{stage}) = 1022\cdot\left[2\left(1 - \frac{1}{1024}\right)\right]^8 - \frac{1024\cdot\left[2^8\left(1 - \frac{1}{1024}\right)^8 - 1\right]}{1 - \frac{1}{512}}\cdot\left(1 - \frac{1}{1024}\right)$$

$$= 262.484\ \text{mV}$$

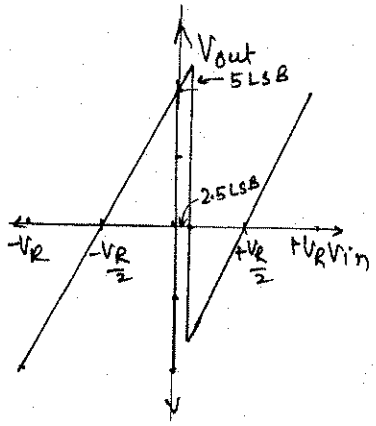
5. Shown below is the first stage of a one-bit-per-stage pipelined ADC. The comparator connects the left plate of C_2 to $-V_{REF}$ if $V_{in} < 0$ and to $+V_{REF}$ if $V_{in} > 0$. Assume $C_1 = C_2$ and the op amp is ideal.

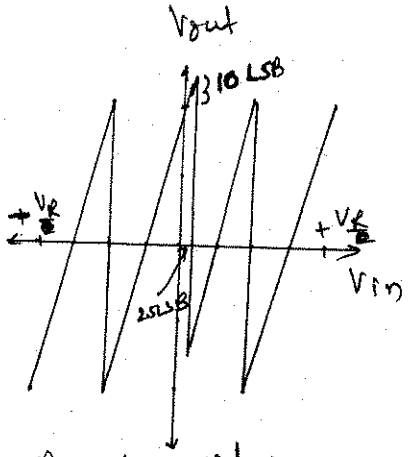
(a) Suppose the comparator has an offset of +2.5 LSB (i.e., V_{in} must exceed +2.5 LSB for the comparator to change its output state). Plot the residue at the output of this stage and at the output of the second stage in the pipeline. Also, show the effect of this offset on the input/output characteristic of the overall ADC.

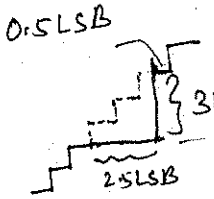
(b) Suppose the comparator in the second stage of the pipeline has an offset of +2.5 LSB (i.e., V_{in} must exceed +2.5 LSB for the comparator to change its output state). Plot the residue at the output of the second stage. Also, show the effect of this offset on the input/output characteristic of the overall ADC.



(a)



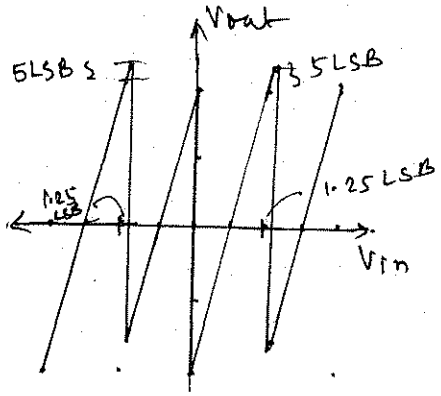


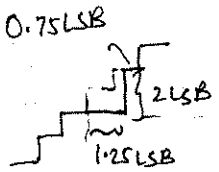


Midcode −1

Residue 1st stage

Residue 2nd stage





$\frac{FS}{4} - 1$ or $\frac{3}{4}FS - 1$

EE 215D

Final Exam

Spring 2009

Name: Solutions

Time Limit: 3 Hours

Open Book, Open Notes

1. 10
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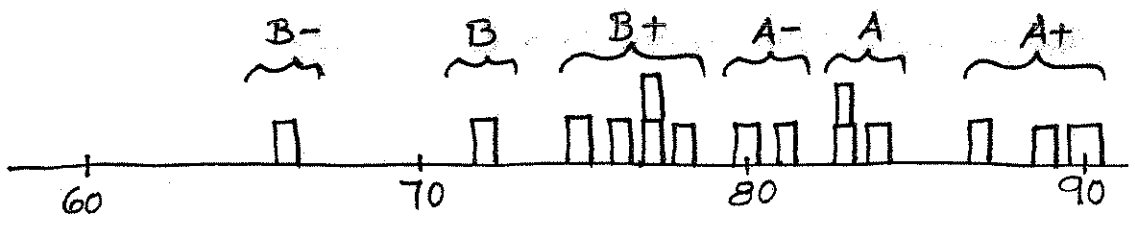
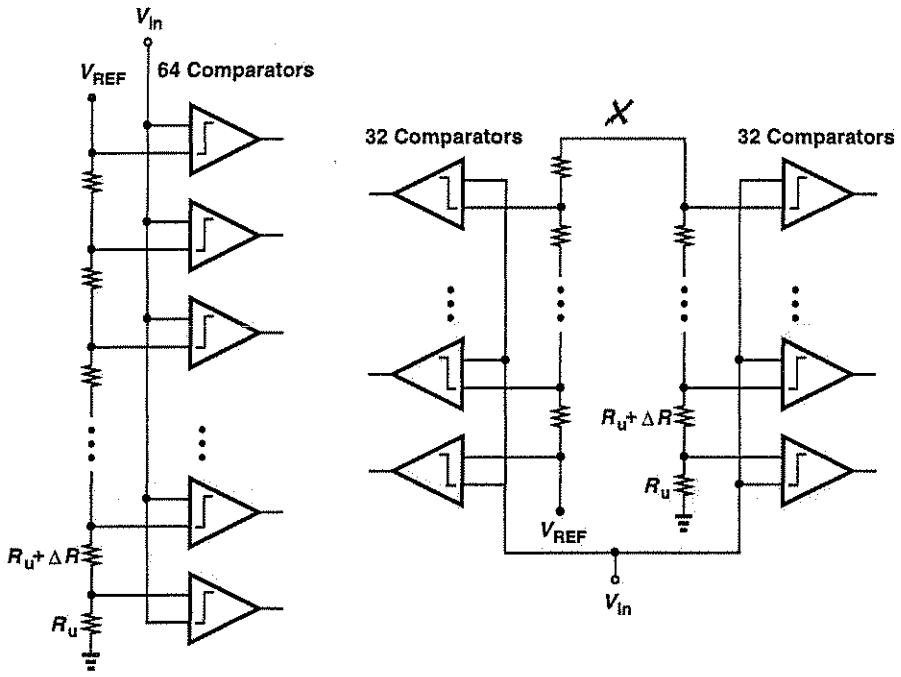
Total: 50



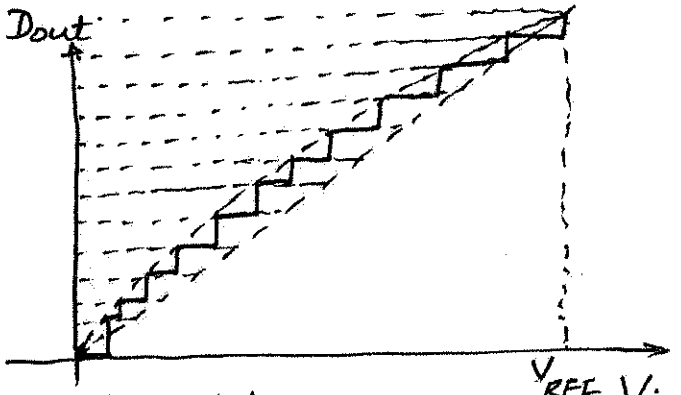
1. A 6-bit flash ADC employs a reference ladder that suffers from a linear gradient. We consider the two ladder topologies shown below. Determine the maximum INL in each case and sketch the input/output characteristic of each ADC, highlighting the differeneces between them. (10)



(a) $INL_{max} = N\, V_{REF}\, \frac{\Delta R}{8R_u}$

$\frac{INL_{max}}{V_{REF}} = \frac{8\Delta R}{R_u}$ %.

(at $V_{in} = \frac{V_{REF}}{2}$).

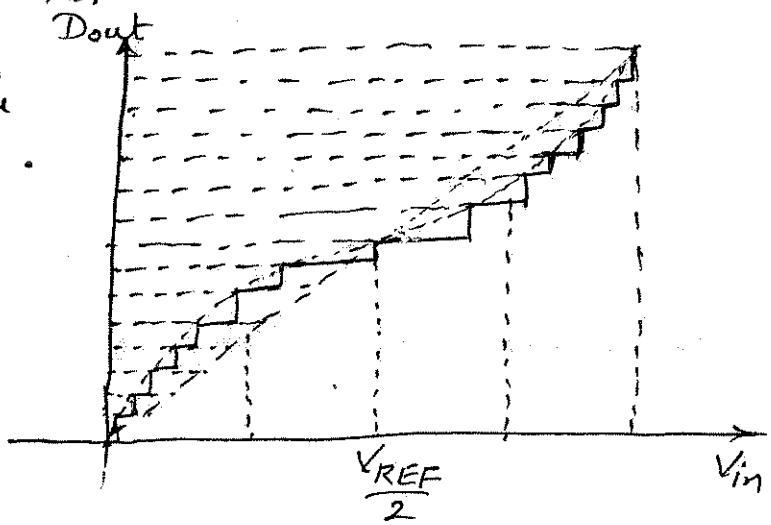


(b) The error now accumulates only to $N/4 = 16$ because the midpoint, V_x, is equal to $V_{REF}/2$.

$INL_{max} = \frac{N}{4} V_{REF} \frac{\Delta R}{8R_u}$

$\frac{INL_{max}}{V_{REF}} = \frac{2\Delta R}{R_u}$ %.

(at $V_{in} = \frac{V_{REF}}{4}$ and $\frac{3V_{REF}}{4}$).

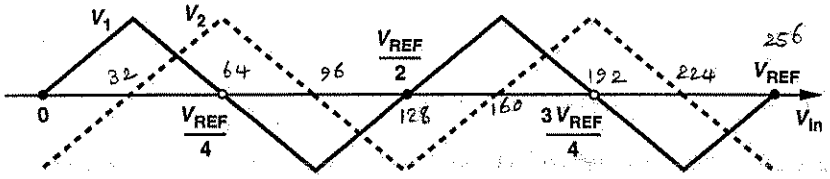


2. We wish to design an 8-bit folding and interpolating ADC. Assume the folding characteristics shown below.

(a) Construct the coarse flash ADC (the comparators and their reference voltages). 2

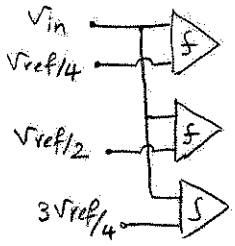
(b) Construct the folding blocks to generate V_1 and V_2. If the analog input has a frequency of f_{in}, what is the frequency of the signal in V_1 and V_2? 4 2

(c) Constuct the interpolation network. How many comparators are required following the interpolation? 2

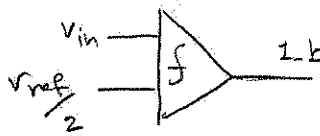


8-bit ⇒ 256 LSB

(a) Three comparators in coarse ADC are needed:

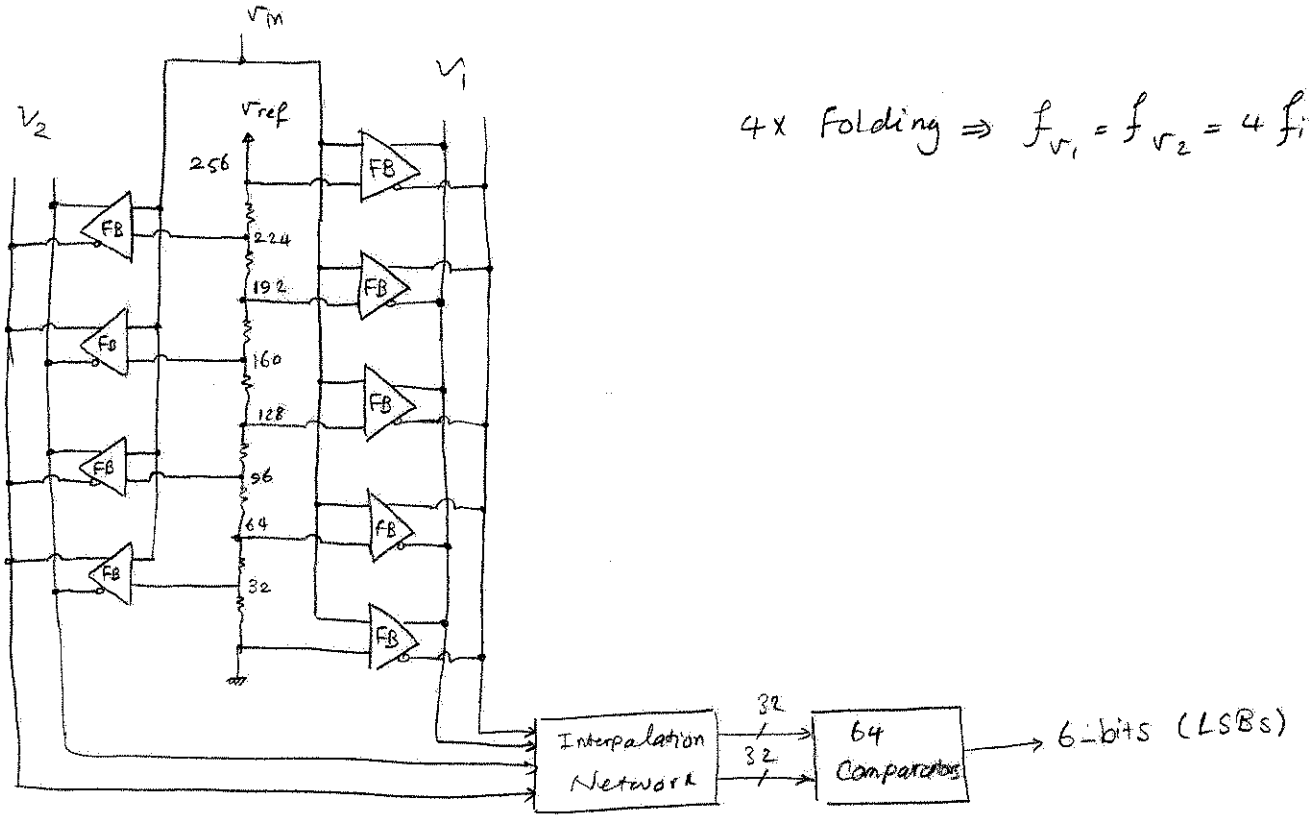


⇒ 2-bits (MSBs) or



1-bit MSB

(b)



4x Folding ⇒ $f_{V_1} = f_{V_2} = 4 f_{in}$

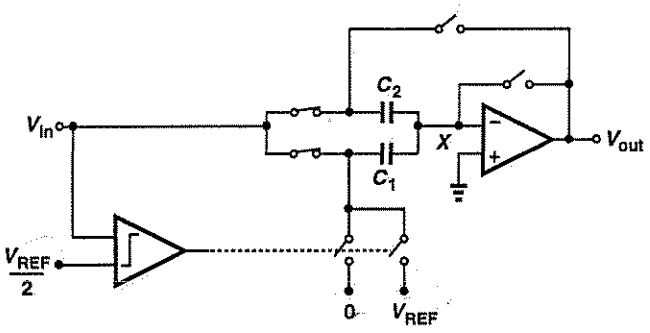
6-bits (LSBs)

3. Consider a 1-bit/stage pipelined ADC. Shown below is the first stage, where C_2 is accidentally chosen equal to $2C_1$ rather than C_1. The other stages in the pipeline operate properly.

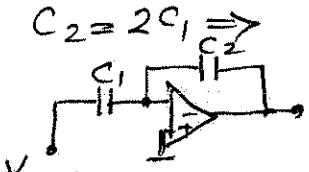
(10)

(a) Plot the residue at the output of the first stage and show significant breakpoints.

(b) Sketch the input/output characteristic and show significant breakpoints.



$C_2 = 2C_1 \Rightarrow$

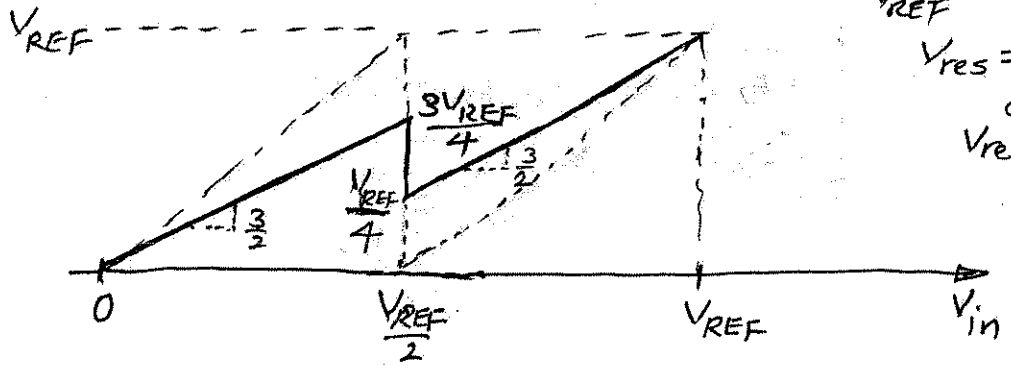


$V_{res} = \frac{3}{2} V_{in} - \frac{1}{2} V_{REF}$

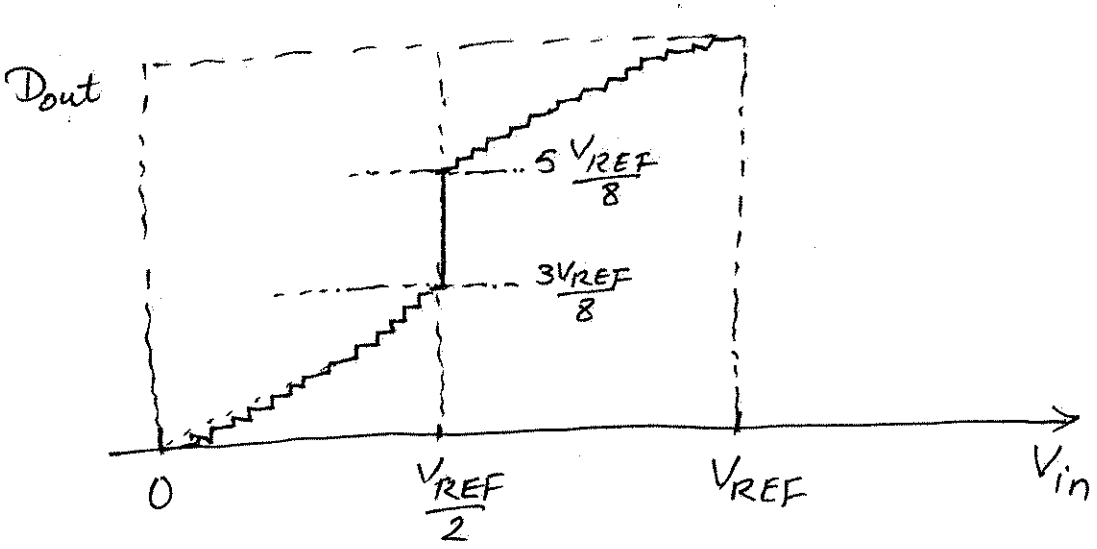
or

$V_{res} = \frac{3}{2} V_{in}$

(a)



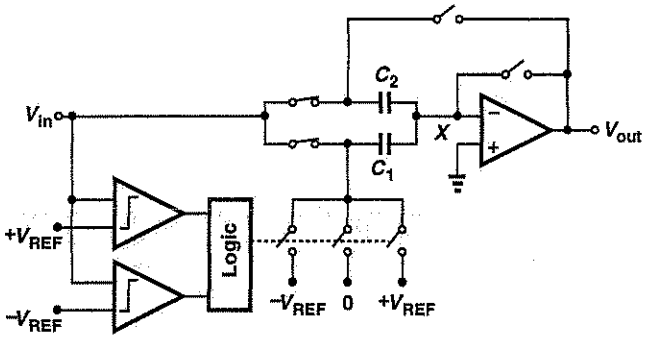
(b)



4. Consider the 1.5-bit/stage pipelined ADC shown below.

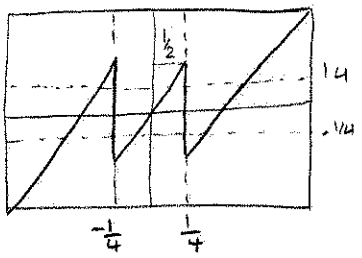
5 (a) Due to a layout error, the $-V_{REF}$ and $+V_{REF}$ connections going to the left plate of C_1 are swapped in the first stage of the pipeline. The other stages operate properly. Plot the residue at the output of the first stage and the overall input/output characteristic.

5 (b) Repeat part (a) if the error has occurred only in the second stage.

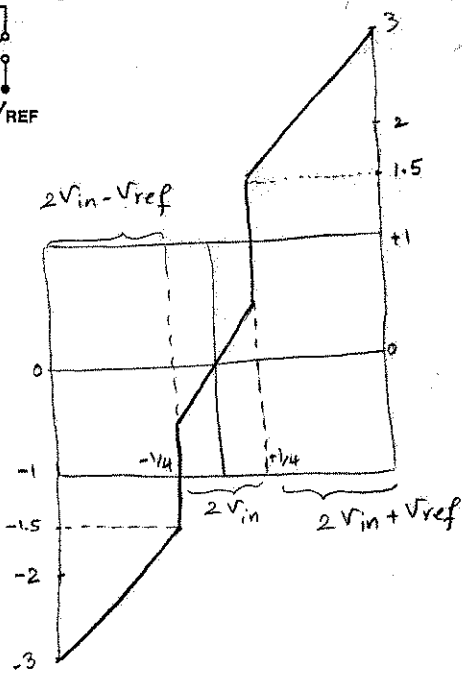


Call values are normalized to V_{ref})

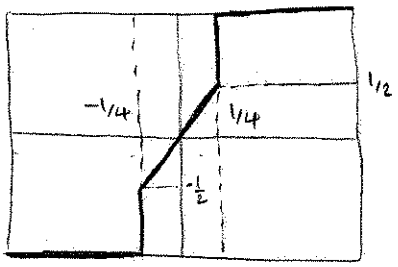
(a) ideal case



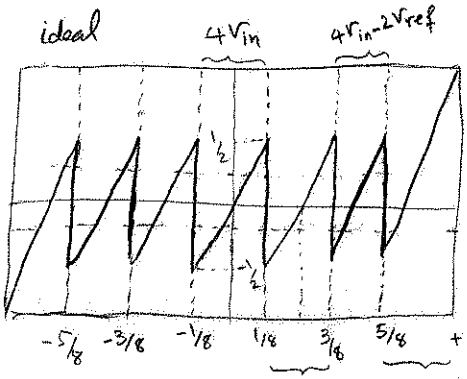
⇒ with error



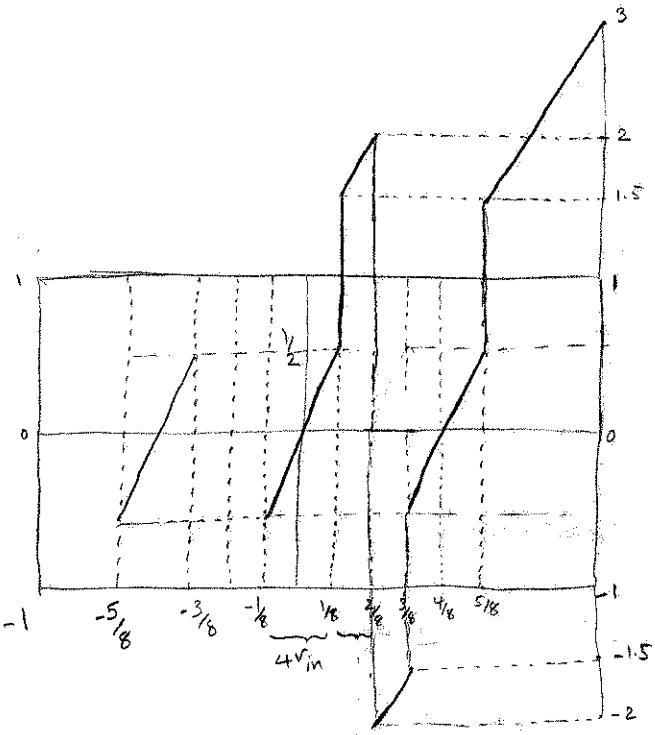
In/out



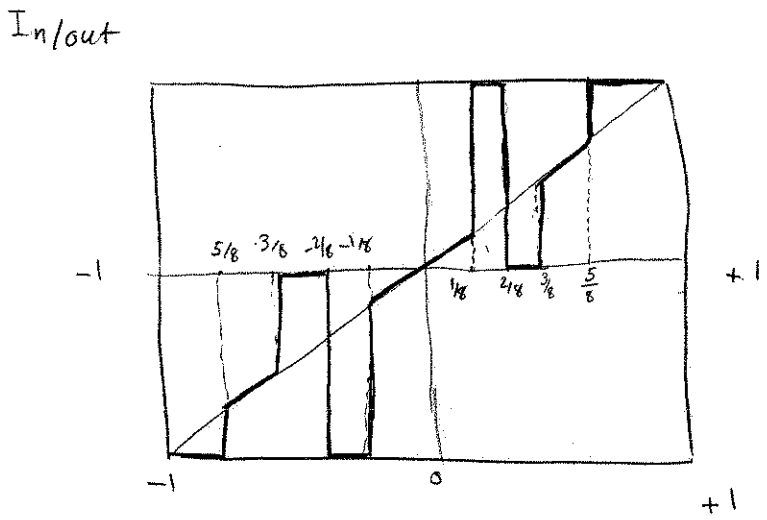
(b) ideal



⇒ error



4) b)

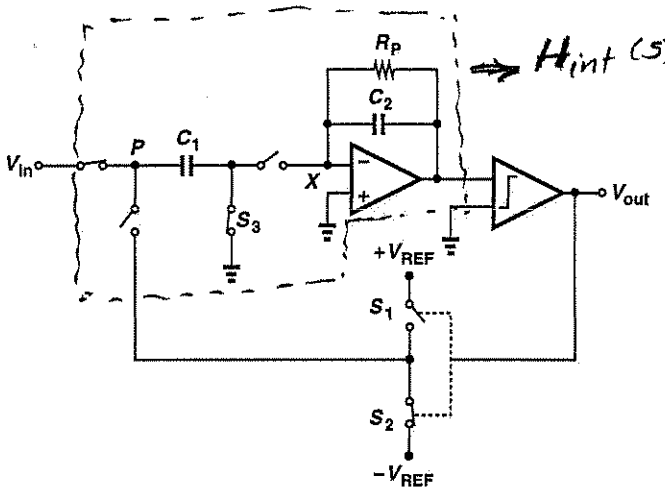


(10)

5. Due to a manufacturing error, a parasitic resistance, R_P, has appeared in parallel with the feedback capacitor in a first-order Σ-Δ modulator's integrator.

(a) Using a continuous-time approximation, determine the spectrum of the quantization noise at the modulator output.

(b) Integrate the noise from $-f_B$ to $+f_B$. What is the minimum tolerable value of R_P if this total noise power must not exceed the ideal value by 10%?



$$H_{int}(s) = -\frac{R_P \| \frac{1}{C_2 s}}{\frac{1}{f_s \cdot C_1}} = -\frac{R_P C_1 f_s}{R_P C_2 s + 1}$$

(a) The transfer function of this integrator is similar to that of the leaky integrator (with a finite op amp gain). From lecture notes,

$$\frac{Y}{Q} = \frac{1}{1 + H_{int}(s)} = \frac{R_P C_2 s + 1}{R_P C_2 s + R_P C_1 f_s + 1}$$

$$S_Y(f) = S_Q(f) \frac{R_P^2 C_2^2 \omega^2 + 1}{R_P^2 C_2^2 \omega^2 + (R_P C_1 f_s + 1)^2} \qquad S_Q(f) = \frac{\Delta^2}{12 f_s}$$

(b) Neglecting the first term in the denominator, we have

$$P_{tot} = \int_{-f_B}^{+f_B} S_Y(f)\,df \cong \int_{-f_B}^{+f_B} \frac{R_P^2 C_2^2 \omega^2 + 1}{(1 + R_P C_1 f_s)^2} \cdot \frac{\Delta^2}{12 f_s}\,df$$

$$\cong \frac{2\Delta^2}{12 f_s (1 + R_P C_1 f_s)^2} \left[f_B + \frac{R_P^2 C_2^2}{3} (2\pi)^2 f_B^3 \right]$$

$$P_{tot,ideal} = \frac{\pi^2}{3} \frac{\Delta^2}{12} \left(\frac{2 f_B}{f_s} \right)^3.$$

If R_P is large, $R_P C_1 f_s \gg 1$. Also, assume $C_1 = C_2 = C$

1.1 $$\frac{\pi^2}{3} \frac{\Delta^2}{12} \left(\frac{2 f_B}{f_s} \right)^3 = \frac{2\Delta^2}{12} \frac{1}{f_s^3 R_P^2 C_1^2} \left[f_B + \frac{R_P^2 C_2^2}{3} (2\pi)^2 f_B^3 \right] \Rightarrow R_P \geq \frac{1}{\sqrt{\frac{0.4}{3}}\, \pi f_B C}$$